



ALPHA & OMEGA
SEMICONDUCTOR

AOW7S60/AOWF7S60
600V 7A α MOS™ Power Transistor

General Description

The AOW7S60 & AOWF7S60 have been fabricated using the advanced α MOS™ high voltage process that is designed to deliver high levels of performance and robustness in switching applications. By providing low $R_{DS(on)}$, Q_g and E_{OSS} along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

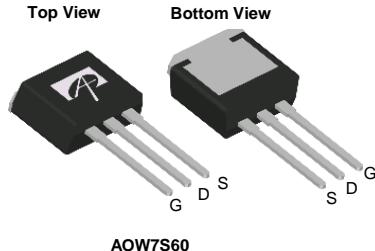
Product Summary

V_{DS} @ $T_{j,max}$	700V
I_{DM}	33A
$R_{DS(ON),max}$	0.6Ω
$Q_{g,typ}$	8.2nC
E_{OSS} @ 400V	1.9μJ

100% UIS Tested
100% R_g Tested

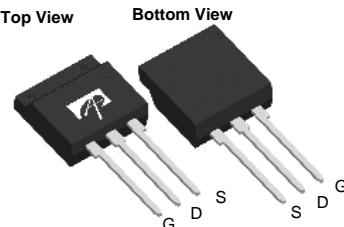


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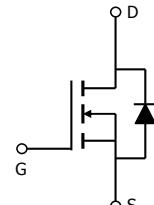


AOW7S60

TO-262F



AOWF7S60



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	AOW7S60	AOWF7S60	Units
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	± 30		V
Continuous Drain Current	I_D $T_c=25^\circ\text{C}$	7	7*	A
	I_D $T_c=100^\circ\text{C}$	5	5*	
Pulsed Drain Current ^C	I_{DM}	33		
Avalanche Current ^C	I_{AR}	1.7		A
Repetitive avalanche energy ^C	E_{AR}	43		mJ
Single pulsed avalanche energy ^G	E_{AS}	86		mJ
Power Dissipation ^B	P_D $T_c=25^\circ\text{C}$	104	25	W
	P_D Derate above 25°C	0.8	0.2	W/ $^\circ\text{C}$
MOSFET dv/dt ruggedness	dv/dt	100		V/ns
Peak diode recovery dv/dt ^H		20		
Junction and Storage Temperature Range	T_J , T_{STG}	-55 to 150		°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds ^J	T_L	300		°C

Thermal Characteristics

Parameter	Symbol	AOW7S60	AOWF7S60	Units
Maximum Junction-to-Ambient ^{A,D}	$R_{\theta JA}$	65	65	°C/W
Maximum Case-to-sink ^A	$R_{\theta CS}$	0.5	--	°C/W
Maximum Junction-to-Case	$R_{\theta JC}$	1.2	5	°C/W

* Drain current limited by maximum junction temperature.

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	600	-	-	V
		I _D =250μA, V _{GS} =0V, T _J =150°C	650	700	-	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =600V, V _{GS} =0V	-	-	1	μA
		V _{DS} =480V, T _J =150°C	-	10	-	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V	-	-	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	2.7	3.3	3.9	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =3.5A, T _J =25°C	-	0.54	0.60	Ω
		V _{GS} =10V, I _D =3.5A, T _J =150°C	-	1.48	1.64	Ω
V _{SD}	Diode Forward Voltage	I _S =3.5A, V _{GS} =0V, T _J =25°C	-	0.82	-	V
I _S	Maximum Body-Diode Continuous Current		-	-	7	A
I _{SM}	Maximum Body-Diode Pulsed Current ^C		-	-	33	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	-	372	-	pF
C _{oss}	Output Capacitance		-	28	-	pF
C _{o(er)}	Effective output capacitance, energy related ^H	V _{GS} =0V, V _{DS} =0 to 480V, f=1MHz	-	22	-	pF
C _{o(tr)}	Effective output capacitance, time related ^I		-	65	-	pF
C _{rss}	Reverse Transfer Capacitance	V _{GS} =0V, V _{DS} =100V, f=1MHz	-	1.2	-	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	17.5	-	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =480V, I _D =3.5A	-	8.2	-	nC
Q _{gs}	Gate Source Charge		-	2.0	-	nC
Q _{gd}	Gate Drain Charge		-	2.8	-	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =400V, I _D =3.5A, R _G =25Ω	-	19	-	ns
t _r	Turn-On Rise Time		-	13	-	ns
t _{D(off)}	Turn-Off DelayTime		-	50	-	ns
t _f	Turn-Off Fall Time		-	15	-	ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =3.5A, dI/dt=100A/μs, V _{DS} =400V	-	198	-	ns
I _{rm}	Peak Reverse Recovery Current	I _F =3.5A, dI/dt=100A/μs, V _{DS} =400V	-	18	-	A
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3.5A, dI/dt=100A/μs, V _{DS} =400V	-	2.4	-	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.

B. The power dissipation P_D is based on T_{J(MAX)=150°C}, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)=150°C}, Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)=150°C}. The SOA curve provides a single pulse rating.

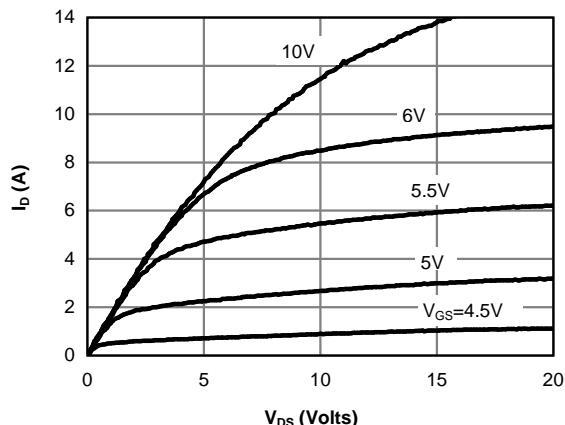
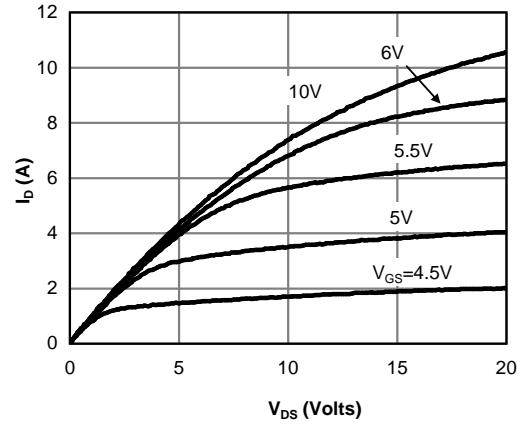
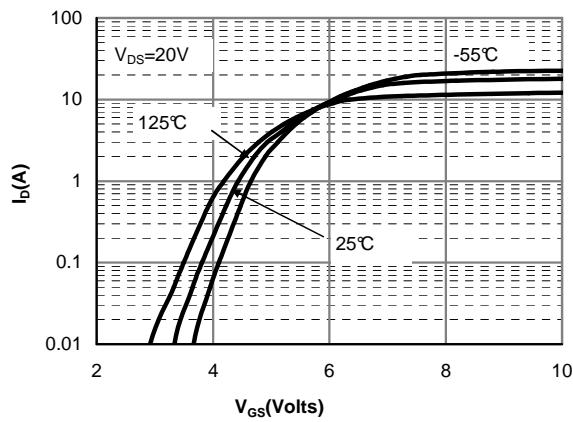
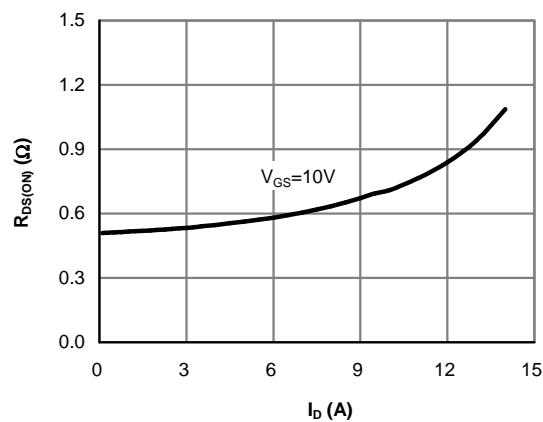
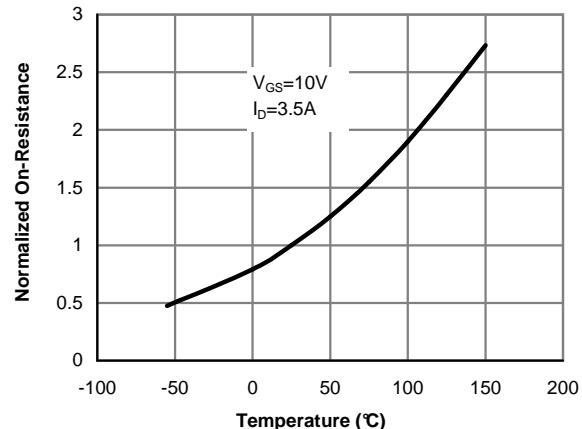
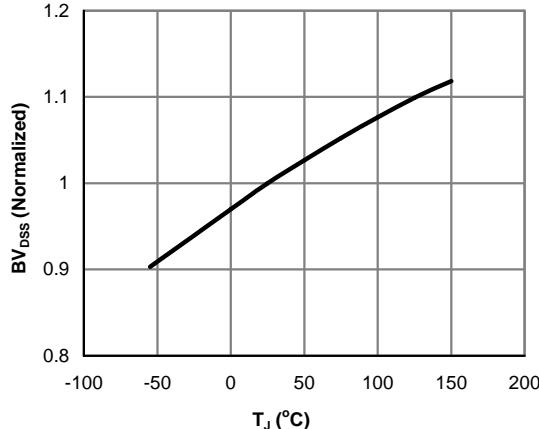
G. L=60mH, I_{AS}=1.7A, V_{DD}=150V, Starting T_J=25°C

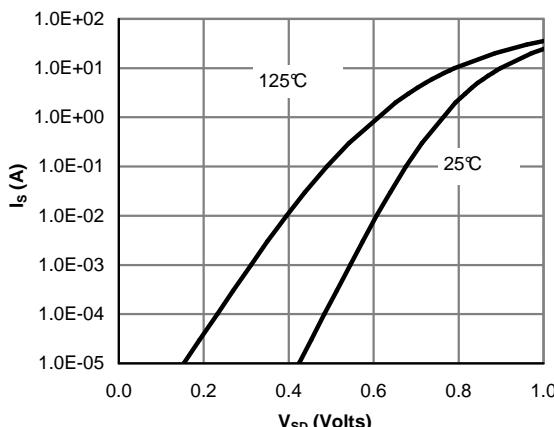
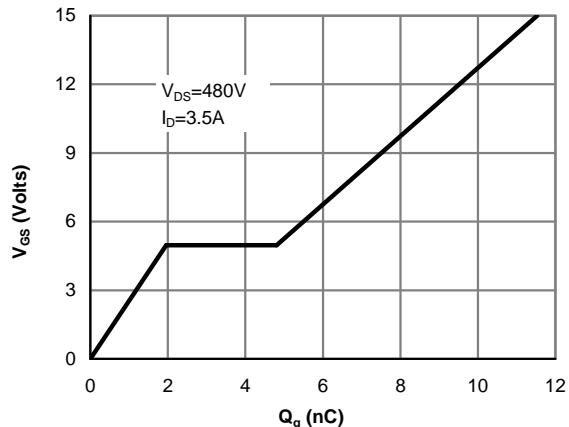
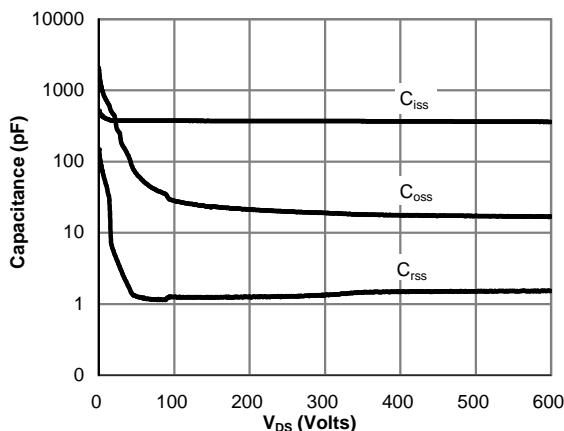
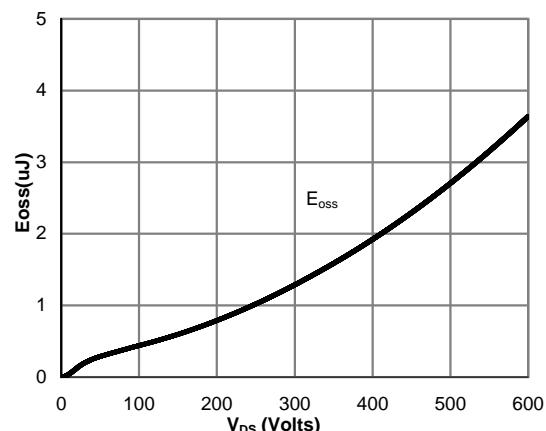
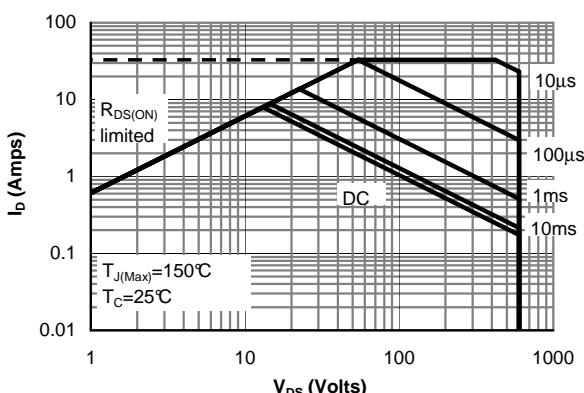
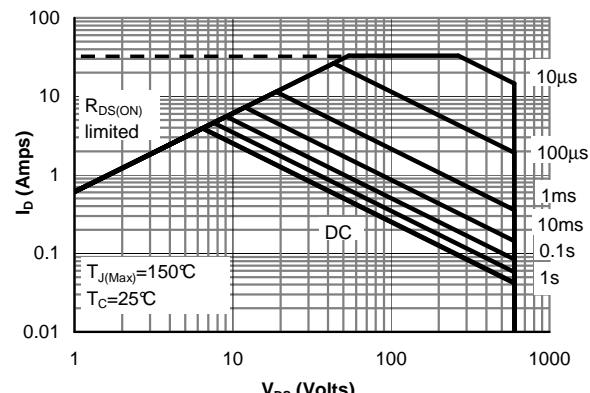
H. C_{o(er)} is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

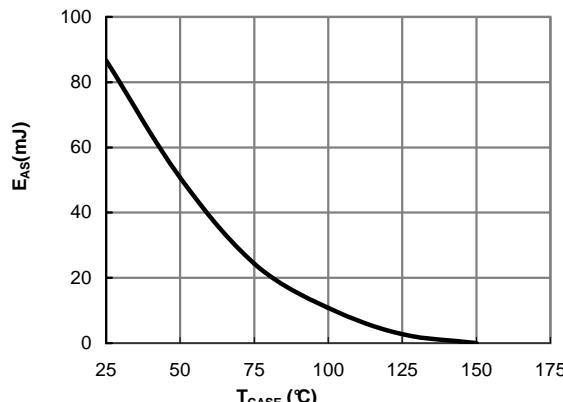
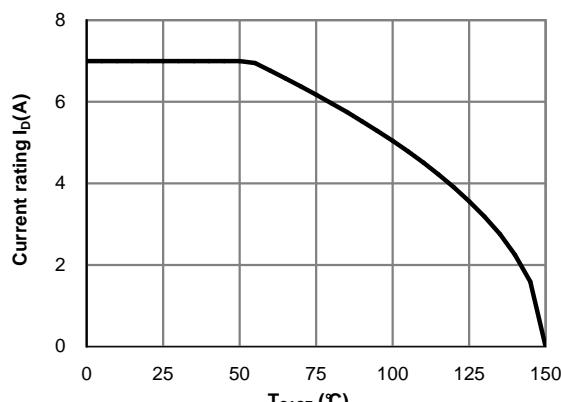
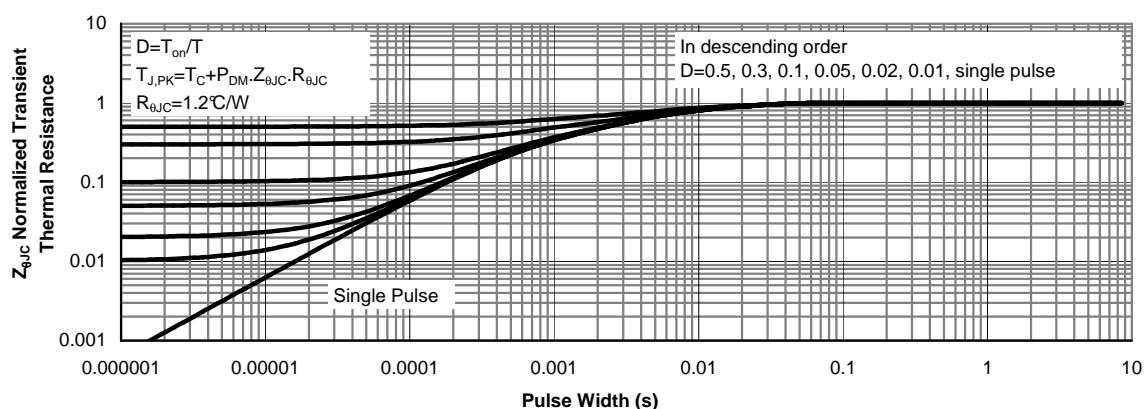
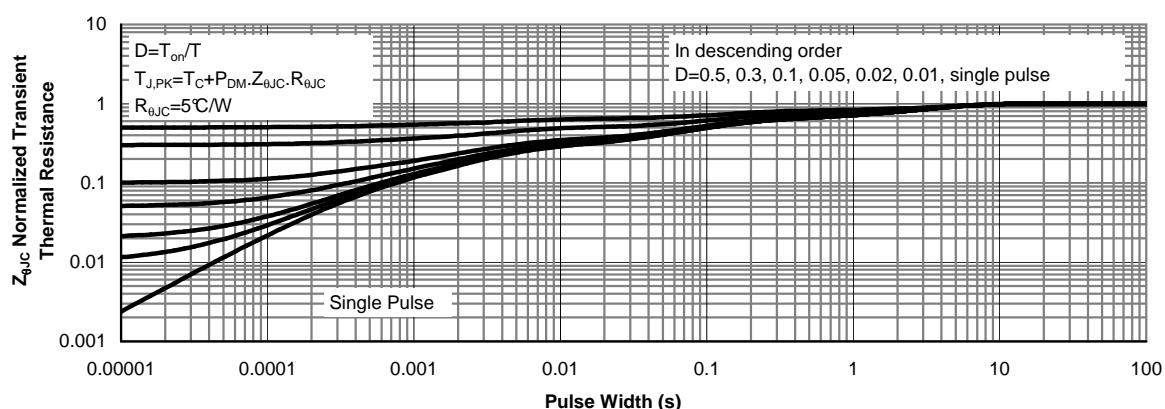
I. C_{o(tr)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{(BR)DSS}.

J. Wavesoldering only allowed at leads.

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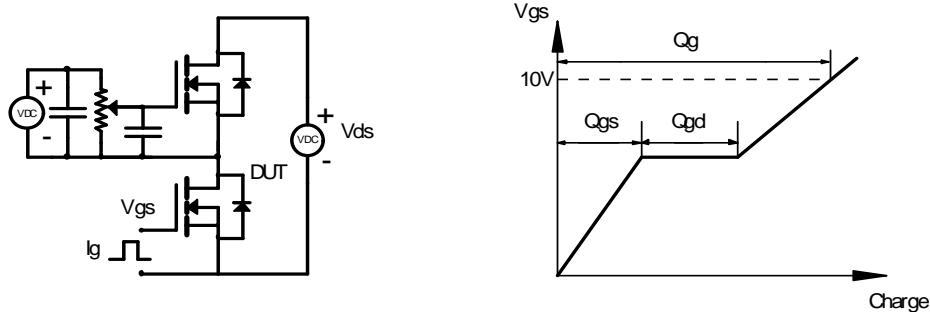
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics@25°C

Figure 2: On-Region Characteristics@125°C

Figure 3: Transfer Characteristics

Figure 4: On-Resistance vs. Drain Current and Gate Voltage

Figure 5: On-Resistance vs. Junction Temperature

Figure 6: Break Down vs. Junction Temperature

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 7: Body-Diode Characteristics (Note E)

Figure 8: Gate-Charge Characteristics

Figure 9: Capacitance Characteristics

Figure 10: Coss stroed Energy

Figure 11: Maximum Forward Biased Safe Operating Area for AOW7S60 (Note F)

Figure 12: Maximum Forward Biased Safe Operating Area for AOWF7S60 (Note F)

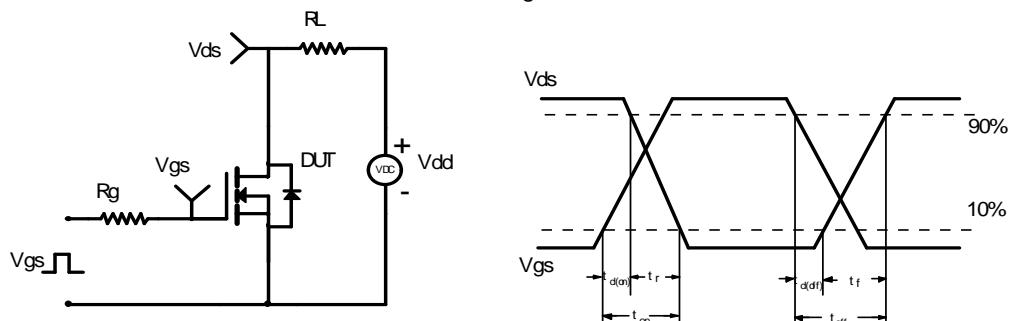
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 13: Avalanche energy

Figure 14: Current De-rating (Note B)

Figure 15: Normalized Maximum Transient Thermal Impedance for AOW7S60 (Note F)

Figure 16: Normalized Maximum Transient Thermal Impedance for AOWF7S60 (Note F)



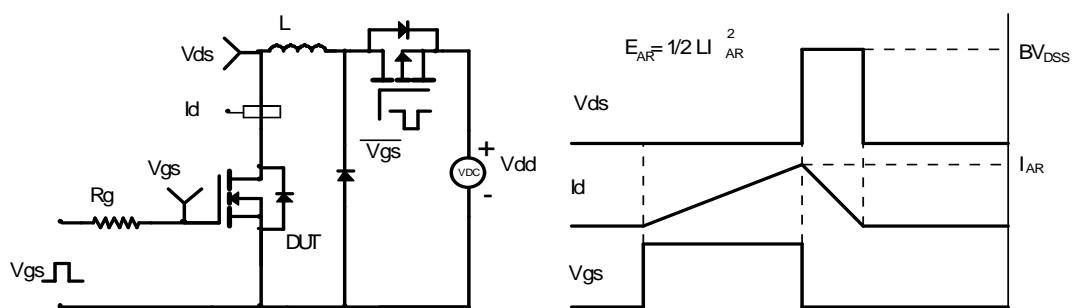
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

