Texas Instruments

TPS40009-Based, 5-A Converter in Less Than One Square Inch

User's Guide

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TPS40009-Based 5-A Converter in Less Than One Square Inch

Mark Dennis *Systems Power*

Contents

1 Introduction

The TPS40009 is a voltage-mode, synchronous buck PWM controller that uses TI's proprietary Predictive Gate Drive™ technology to wring maximum efficiency from step-down converters. This controller provides a bootstrap charging circuit to allow the use of an N-channel MOSFET as the topside buck switch to reduce conduction losses and increase silicon device utilization. Predictive Gate Drive™ technology controls the delay from main switch turn-off to synchronous rectifier turn-on and also the delay from rectifier turn-off to main switch turn-on. This allows minimization of the losses in the MOSFET body diodes by reducing conduction and reverse recovery time. This user's guide provides details on a 5-A buck converter that converts 3.3 V down to a 1.2-V level using the TPS40009 controller, with less than one square inch board area.

A schematic for the board is shown in Figure 1. A list of material is provided in the final section.

2 Features

The specification for this board is as follows:

- V_{IN} = 3.0 V to 3.6 V
- V_{OUT} = 1.2 V ± 3%
- 0 A ≤ I_{OUT} ≤ 5 A
- Efficiency > 90% with a load of 2 A
- Output voltage ripple < 2% V_{OUT}
- Physical size < 1 square inch circuit area

3 Schematic

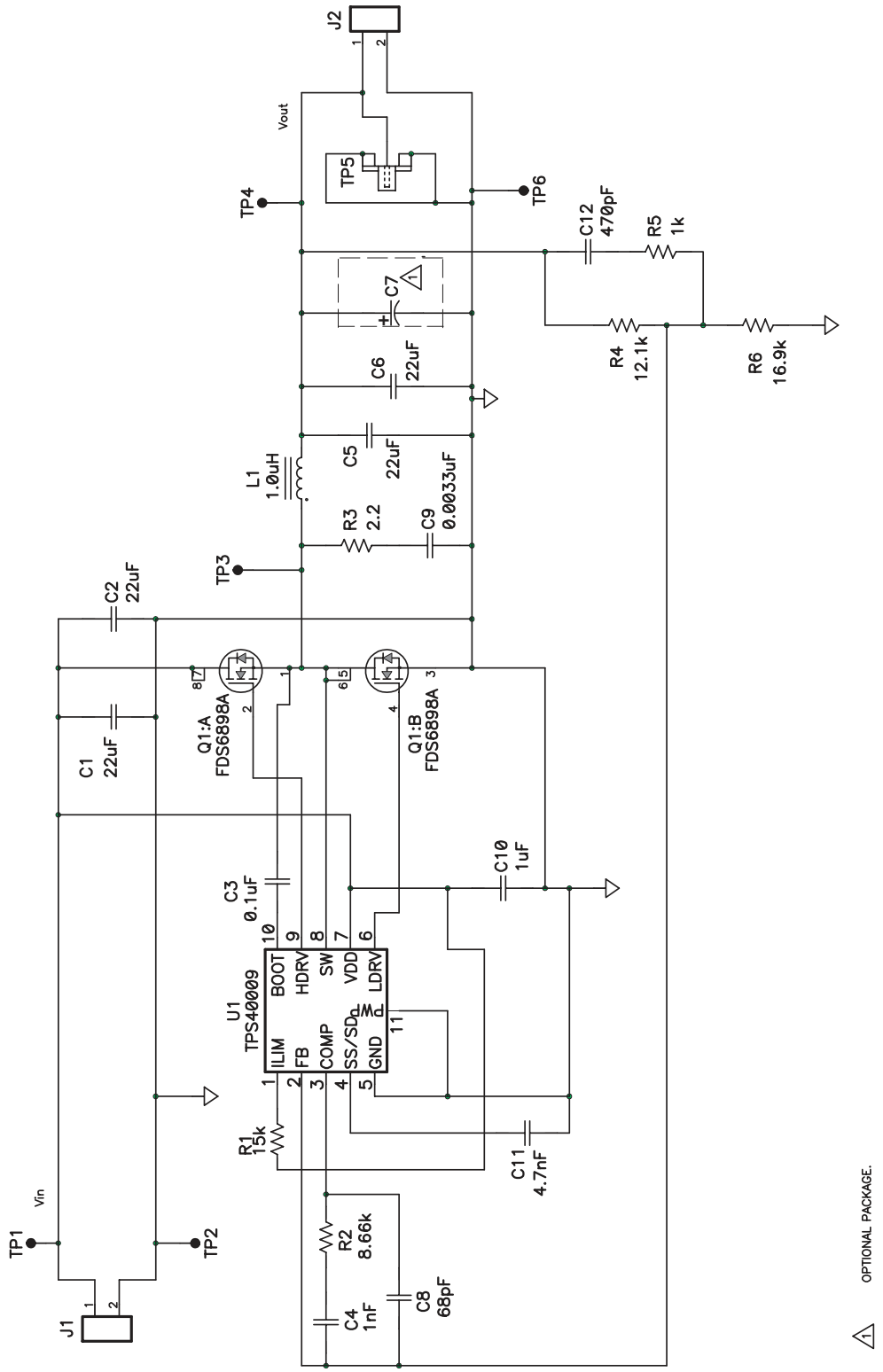


Figure 1. Application Diagram for the TPS40009

4 Design Procedure

4.1 Controller Selection

The TPS40009 synchronous buck controller is selected for this small size application because the 600-kHz switching frequency enables the selection of minimally sized filter components. The TPS40007 is available for applications needing 300-kHz operation for designs where efficiency is to be optimized.

4.2 Inductance Value

The output inductor value is selected to set the ripple current to a value most suited to overall circuit functionality. The inductor value is calculated in equation (1).

$$L = \frac{V_{OUT}}{f \times I_{RIPPLE}}\left(1 - \frac{V_{OUT}}{V_{IN(max)}}\right) = \frac{1.2\ V}{600\ kHz \times 1.25\ A} \times \left(1 - \frac{1.2\ V}{3.6\ V}\right) = 1.07\ \mu H \quad (1)$$

where I_{RIPPLE} is chosen to be 25% of I_{OUT}, or 1.25 A. A common value of 1 μH is selected.

4.3 Input Capacitor Selection

Bulk input capacitor selection is based on allowable input voltage ripple and required RMS current carrying capability. In typical buck converter applications, the converter is fed from an upstream power converter with its own output capacitance. In this converter, onboard capacitance is provided to supply the current required during the top MOSFET on-time while keeping ripple within acceptable limits. For this power level, input voltage ripple of 150 mV is reasonable, and a conservative minimum value of capacitance is calculated in equation (2).

$$C = \frac{I \times \Delta t}{\Delta V} = \frac{5\ A \times 606\ ns}{0.15\ V} = 20\ \mu F \quad (2)$$

To meet this requirement with the lowest size and cost, a single 22 μF, X5R ceramic capacitor might be considered. Although these capacitors have an extremely small resistance a typical datasheet indicates that the part undergoes a 30°C temperature rise with 2 A_{RMS} current at 500 kHz. With V_{IN} = 3.0 V our circuit requires nearly 2 A_{RMS} of current, so for a conservative design two capacitors are selected to allow for conservative current derating. These capacitors function as power bypass components and should be located near the MOSFET package, to keep the high frequency current flow in a tight loop. The low impedance characteristics of the dual ceramic capacitors help to reduce noise on the V_{DD} supply of the device. Specifically, the high side MOSFET current sense is referenced to this point, so noise at the device must be kept to a low level.

4.4 Output Capacitor Selection

Selection of the output capacitor is based on many application variables, including function, cost, size, and availability. The minimum allowable output capacitance is determined by the amount of inductor ripple current and the allowable output ripple in equation (3).

$$C_{OUT(min)} = \frac{I_{RIPPLE}}{8 \times f \times V_{RIPPLE}} = \frac{1.25\ A}{8 \times 600\ kHz \times 12\ mV} = 22\ \mu F \quad (3)$$

In this design, $C_{OUT(min)}$ is 22 µF with V_{RIPPLE} = 12 mV to allow for some margin. However, this only affects the capacitive component of the ripple voltage. In addition, the voltage component due to the capacitor ESR must be considered in equation (4).

$$ESR_{Cout} \leq \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{0.012\ V}{1.25\ A} = 9.6\ m\Omega \quad (4)$$

For compactness while maintaining transient response capability, two 22-µF ceramic capacitors are fitted in parallel. The total ESR of these capacitors is below 3 mΩ, and contributes only a few mV to the output voltage ripple.

4.5 MOSFET Selection

The small physical size of this design requires the use of a single SO-8 package which contains dual N-channel MOSFETs. MOSFETs with an $R_{DS(on)}$ of 18 mΩ are selected to keep the conduction losses to a manageable amount at full load.

4.6 Short Circuit Protection

The TPS40009 implements short circuit protection by comparing the voltage across the topside MOSFET while it is on to a voltage dropped from VDD by R_{LIM} due to an internal current source of 15 µA inside pin 1. Due to tolerances in the current source and variations in the power MOSFET on-voltage versus temperature, the short circuit level can protect against gross overcurrent conditions only, and should be set higher than rated load. In this particular case, R_{LIM} is selected as:

$$R_{LIM} = R1 = \frac{2.5 \times I_{OUT} \times 0.018\ \Omega}{15\ \mu A} = 15\ k\Omega \quad (5)$$

For this design, R_{LIM} = 15 kΩ, and the factor of 2.5 in the equation accounts for the variations in component tolerances over temperature and output current ripple.

4.7 Compensation Design

The TPS40009 uses voltage mode control in conjunction with a high frequency error amplifier. For the fastest transient response, the loop crossover frequency is set at 1/10 f_S, or 60 kHz. The power circuit L-C double pole corner frequency f_C is situated at 24 kHz, and the output capacitor ESR zero is far higher at approximately 1MHz. The feedback compensation network is implemented to provide two zeroes and three poles. The first pole is placed at the origin to improve dc regulation.

The first zero is placed at approximately 2/3 f_C, 18 kHz,

$$f_{z1} = \frac{1}{2 \times \pi \times R_2 \times C_4} \tag{6}$$

The second zero is selected at f_C,

$$f_{z2} = \frac{1}{2 \times \pi \times \left(R_4 + R_5\right) \times C_{12}} \tag{7}$$

The two poles are placed at approximately 300 kHz, which is one-half the switching frequency,

$$f_{p1} = \frac{1}{2 \times \pi \times R_2 \times \left(\frac{C_4 \times C_8}{C_4 + C_8}\right)} \tag{8}$$

and

$$f_{p2} = \frac{1}{2 \times \pi \times R_5 \times C_{12}} \tag{9}$$

Figure 2 shows the plots for the closed loop gain and phase with V_{IN} = 3.3 V and I_{OUT} = 4.4 A. At the crossover frequency of 60 kHz the phase margin is approximately 51 degrees.

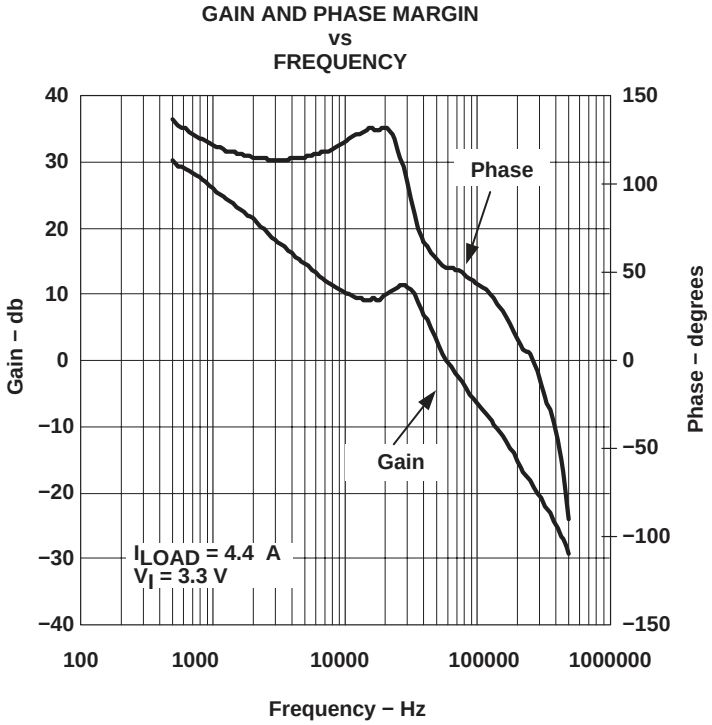


Figure 2.

4.8 Snubber Component Selection

The switch node where Q1 and L1 come together is very noisy. An R−C network fitted between this node and ground can help reduce ringing and voltage overshoot on Q1:B. This ringing noise should be minimized to prevent it from confusing the control circuitry which is monitoring this node for current limit and Predictive Gate Drive™.

As a starting point, the snubber capacitor, C9, is generally chosen to be 5 to 8 times larger than the parasitic capacitance at the node, which is primarily C_{OS} of Q1:B. Since C_{OS} is 440 pF for Q1:B, C9 is chosen to be 3.3 nF. R3 is empirically determined to be 2.2 Ω, which minimizes the ringing and overshoot at the switch node. With low input voltages the power loss, $1/2 \times C \times V^2 \times f$, is relatively small at 24 mW.

5 PowerPAD™ Packaging

The TPS4000X family is available in the DGQ version of TI's PowerPAD™ thermally enhanced package. In the PowerPAD™, a thermally conductive epoxy is used to attach the integrated circuit die to the leadframe die pad, which is exposed on the bottom of the completed package. The leadframe die pad can be soldered to the PCB using standard solder flow techniques when maximum heat dissipation is required. However, depending on power dissipation requirements, the PowerPAD™ may not need to soldered to the PCB.

The PowerPAD™ package helps to keep the junction temperature rise relatively low even with the power dissipation inherent in the onboard MOSFET drivers. This power loss is proportional to switching frequency, drive voltage, and the gate charge needed to enhance the N-channel MOSFETs. Effective heat removal allows the use of ultra small packaging while maintaining high component reliability.

To effectively remove heat from the PowerPAD™ package, a thermal land should be provided directly underneath the package whether the package needs to be soldered or not. This thermal land usually has vias that help to spread heat to internal copper layers and/or the opposite side of the PCB. The vias should not have thermal reliefs that are often used on ground planes, because this reduces the copper area which transfers heat. Additionally, the vias should be small enough so that the holes are effectively plugged when plated. This prevents the solder from wicking away from the connection between the PCB surface and the bottom of the part. A typical construction uses a few vias of 0.013" diameter plated with 1 ounce copper in the land under the TPS40009. A typical layout pattern is shown in Figure 2, but does not show the copper land which would encompass the vias above and below the device.

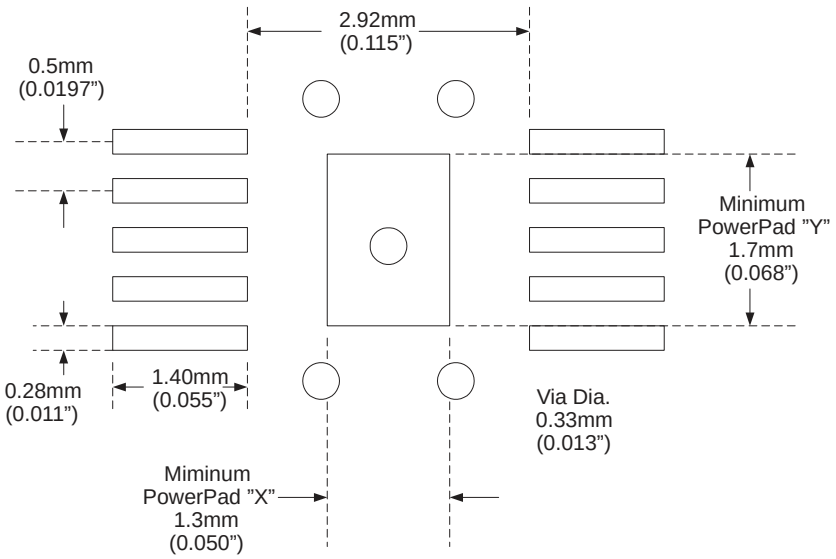


Figure 3. PowerPAD PCB Layout Guidelines

The Texas Instrument document, PowerPAD™ Thermally Enhanced Package Application Report (SLMA002) should be consulted for more information on the PowerPAD™ package. This report offers in-depth information on the package, assembly and rework techniques, and illustrative examples of the thermal performance of the PowerPAD™ package.

6 Test Results/Performance Data

The test setup is shown in figure 4

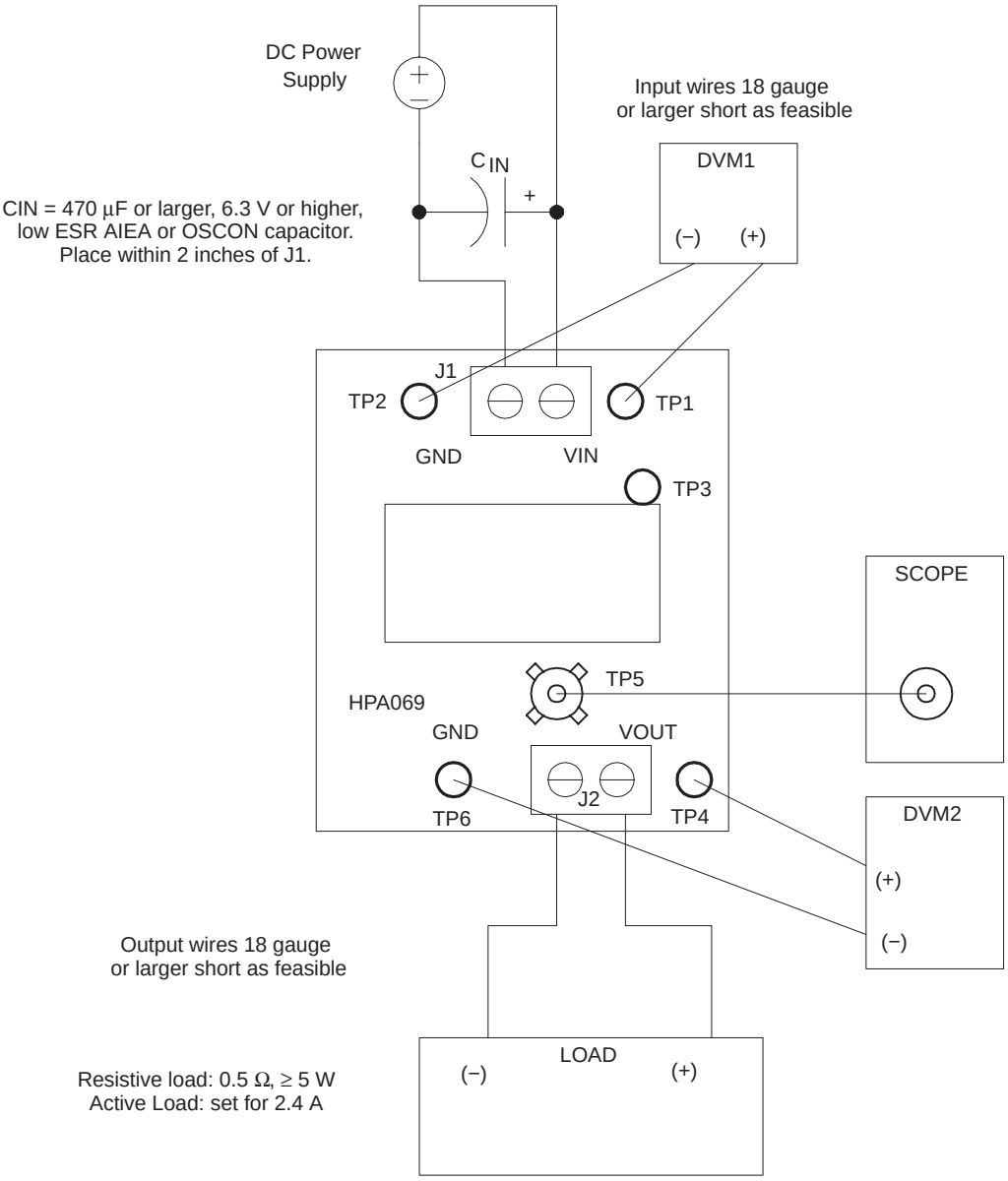


Figure 4.

Typical efficiency curves are shown in Figure 5 for an input of 3.3 V.

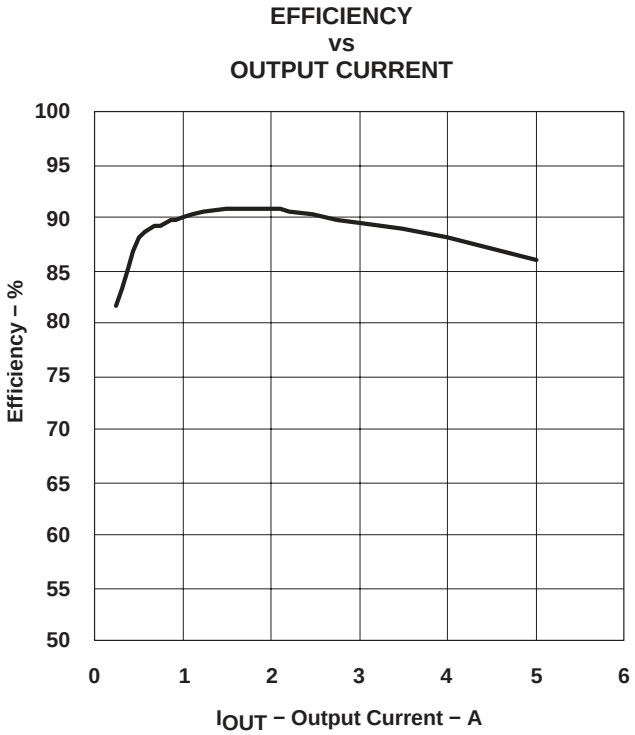


Figure 5.

Figure 6 shows the switch node during typical operation at full load. Note that there is very minimal body diode conduction in the bottom MOSFET. This is a result of using the predictive delay control implementation. This technique is able to dynamically change the delays in the MOSFET drive circuit to account for variations in line, load, and between devices.

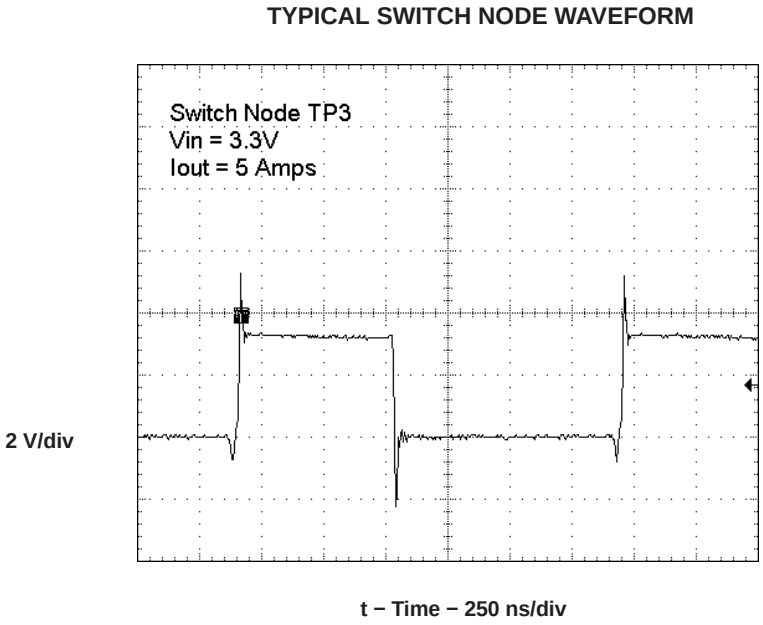


Figure 6.

Circuit operation with an output short circuit is shown in Figure 7. After each restart into a short circuit the pulses terminate for a period of approximately 6 ms. This causes the input power to collapse to minuscule levels, and the circuit is protected.

SHORT CIRCUIT OPERATION

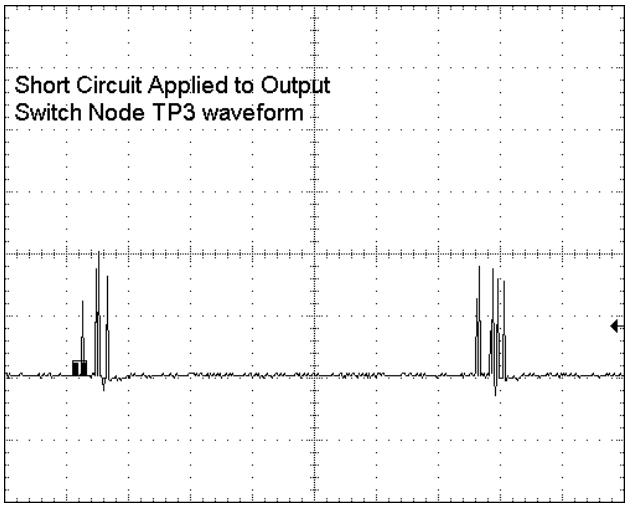


Figure 7.

Figure 8 shows the output voltage ripple which is approximately half the 24-mV limit.

OUTPUT VOLTAGE RIPPLE

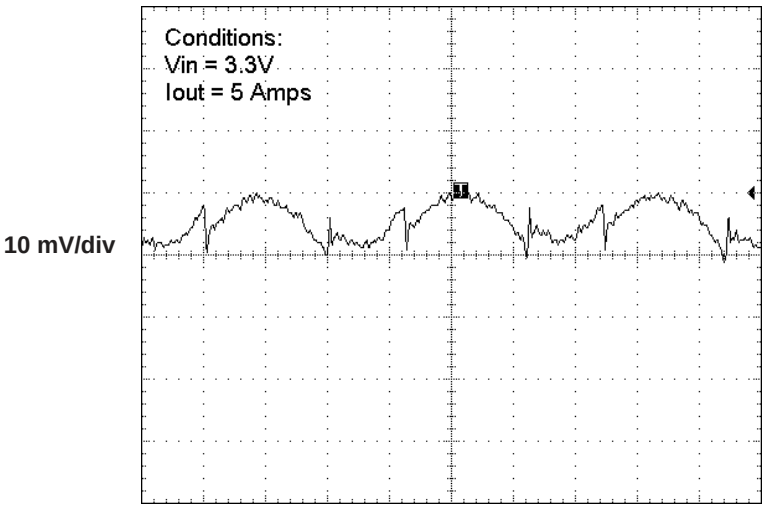
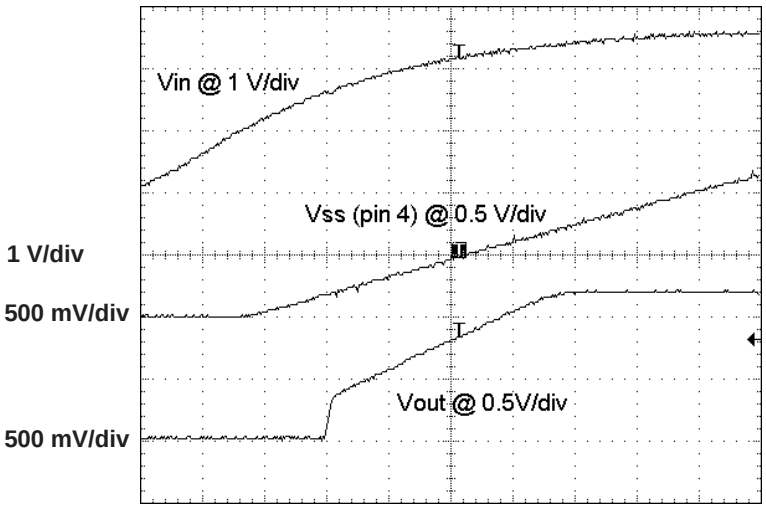


Figure 8.

Figure 9 shows the startup waveforms with an input voltage of 3.3 V and a load of 0.3 Ω. Note that the output is held low until V_{SS} (pin 4) goes above 0.12 V, and then the output comes up smoothly under closed loop softstart control.

STARTUP WAVEFORM

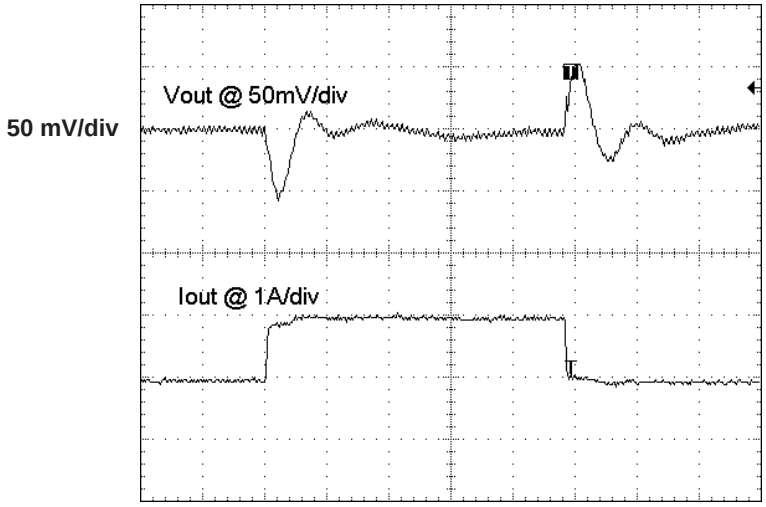


t − Time − 200 μs/div

Figure 9.

Figure 10 shows the transient response for a fast load step from 1 A to 2 A.

TRANSIENT RESPONSE



t − Time − 20 μs/div

Figure 10.

7 PCB Layout

Figures 11 through13 show the top copper layer, the bottom copper layer, and top assembly layer, of HPA069.

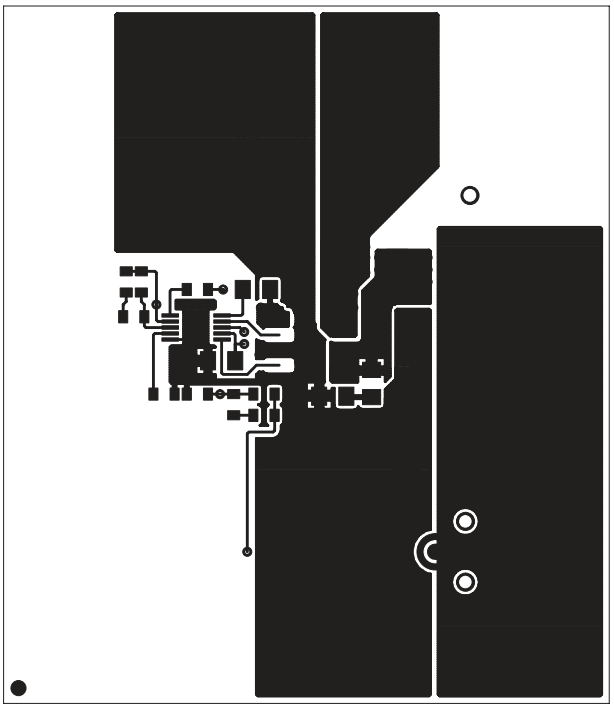


Figure 11

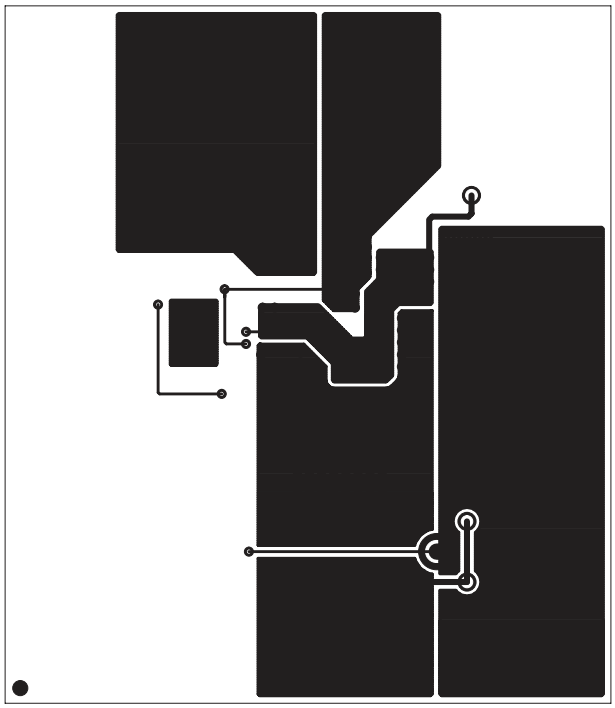
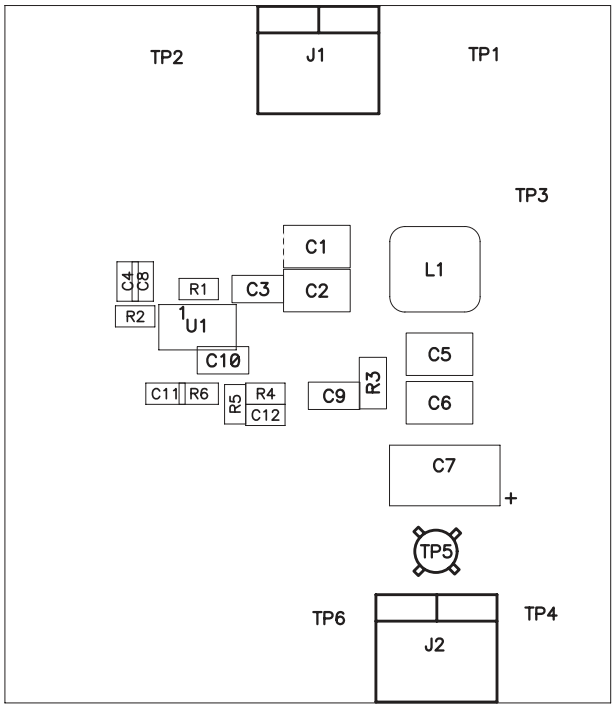
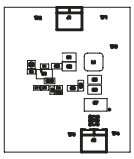


Figure 12





actual size

Figure 13

8 List of Material

Table 1 lists the components used in this design. With minor component tweaks this design could be modified to meet a wide range of applications.

	Reference	Qty	Description	Manufacturer	Part Number
Capacitor	C1, C2, C5, C6	4	Ceramic, 22 μF, 6.3 V, X5R, 20%, 1210	Panasonic	ECJ−4YB0J226M
	C10	1	Ceramic, 0.001 μF, 10 V, X5R, 10%, 805	Panasonic	ECJ−2YB1A105K
	C11	1	Ceramic, 0.0047 μF, 50 V, X7R, 10%	Vishay	VJ0603Y472KXAAT
	C12	1	Ceramic, 470 pF, 50 V, X7R, 10%	Vishay	VJ0603Y471KXAAT
	C3	1	Ceramic, 0.1 μF, 50 V, X5R, 10%	Vishay	VJ0805Y104KXAAT
	C4	1	Ceramic, 0.001 μF, 50 V, X7R, 10%	Vishay	VJ0603Y102KXAAT
	C8	1	Ceramic, 68 pF, 50 V, NPO, 10%	Vishay	VJ0603A680KXAAT
	C9	1	Ceramic, 0.0033 μF, 50 V, X7R, 10%	Vishay	VJ0805Y332KXAAT
Terminal Block	J1, J2	2	2 pin, 15 A, 5.1 mm	OST	ED1609
Inductor	L1	1	SMT, 1.0 μH, 8.5 A, 10 mΩ	Vishay	IHLP−2525CZ−01
MOSFET	Q1	1	Dual N−channel, 20 V, 9.4 A, 18 mΩ	Fairchild	FDS6898A
Resistor	R1	1	Chip, 15 kΩ, 1/16W, 1%	Std	Std
	R2	1	Chip, 8.66 kΩ, 1/16 W, 1%	Std	Std
	R3	1	Chip, 2.2 Ω, 1/10 W, 5%	Std	Std
	R4	1	Chip, 12.1 kΩ, 1/16 W, 1%	Std	Std
	R5	1	Chip, 1 kΩ, 1/16 W, 1%	Std	Std
	R6	1	Chip, 16.9 Ω, 1/16 W, 1%	Std	Std
JACK	TP1, TP3, TP4,	5	Test point, red	Farnell	240−345
JACK	TP2, TP6	2	Test point, black	Farnell	240−333
Adaptor	TP5	1	3.5-mm probe clip (or 131−5031−00)	Tektronix	131−4244−00
Device	U1	1	Syncronous buck controller, 600 kHz	TI	TPS40009DGQ

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