FEATURES:

- **256 x 256 channel non-blocking switch**
- **Automatic signal identification (ST-BUS®, GCI)**
- **8 RX inputs — 32 channels at 64 Kbit/s per serial line**
- **8 TX outputs — 32 channels at 64 Kbit/s per serial line**
- **Three-state serial outputs**
- **Microprocessor Interface (8-bit data bus)**
- **Frame Integrity for data applications**
- **5V Power Supply**
- **Operating Temperature Range -40°C to +85°C**
- **Available in 44-pin Plastic Leaded Chip Carrier (PLCC), 44-pin Plastic Quad Flatpack (PQFP) and 40-pin Plastic Dip (P-DIP)**

DESCRIPTION:

The IDT728985 is a ST-BUS®/GCI compatible digital switch controlled by a microprocessor. The IDT728985 can handle as many as 256, 64 Kbit/s input and output channels. Those 256 channels are divided into 8 serial inputs and outputs, each of which consists of 32 channels. The IDT728985 provides per-channel variable or constant throughput delay modes and microprocessor read

and write access to individual channels. As an important function of a digital switch is to maintain sequence integrity and minimize throughput delay, the IDT728985 is an ideal solution for most switching needs.

FUNCTIONAL DESCRIPTION

Frame sequence, constant throughput delay, and guaranteed minimum delay are high priority requirements in today's integrated data and multimedia networks. The IDT728985 provides these functions on a per-channel basis using a standard microprocessor control interface. Each of the eight serial lines is designed to switch 64 Kbit/s PCM or N x 64 Kbit/s data.

In Processor Mode, the microprocessor can access the input and output time slots to control other devices such as ISDN transceivers and trunk interfaces. Supporting both GCI and ST-BUS® formats, IDT728985 has incorporated an internal circuit to automatically identify the polarity and format of the frame synchronization.

A functional block diagram of the IDT728985 device is shown on page 1. The serial streams operate continuously at 2.048 Mb/s and are arranged in 125μs wide frames each containing 32, 8-bit channels. Eight input (RX0-7) and
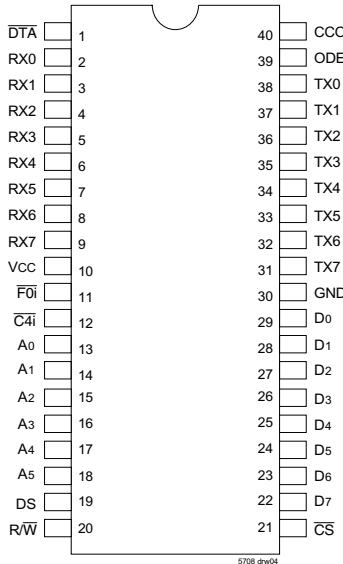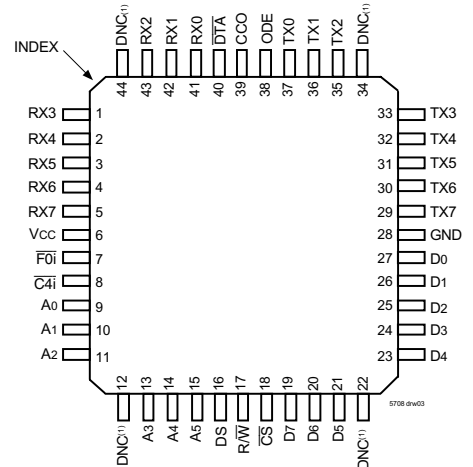
FUNCTIONAL BLOCK DIAGRAM

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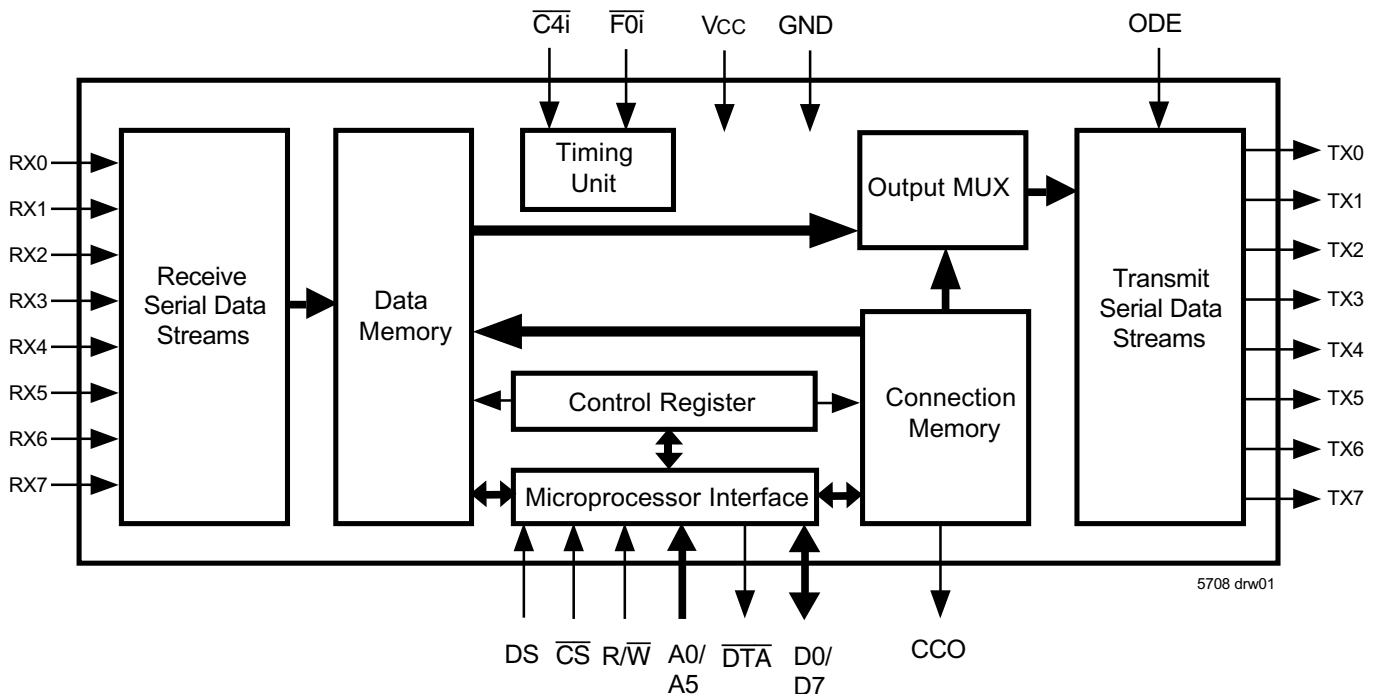
PIN CONFIGURATION
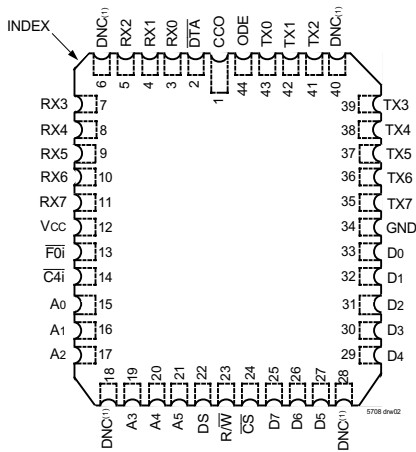
**PLCC: 0.05in. pitch, 0.65in. x 0.65in.
(J44-1, order code: J)
TOP VIEW**

**PLASTIC DIP: 0.10in. pitch, 2.05in. x 0.60in.
(P40-1, order code: P)
TOP VIEW**

**PQFP: 0.80mm pitch, 10mm x 10mm
(DB44-1, order code: DB)
TOP VIEW**

NOTE:
1. DNC - Do Not Connect

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
GND	Ground.		Ground Rail.
Vcc	Vcc		+5.0 Volt Power Supply.
$\overline{DTA}$	Data Acknowledgment (Open Drain)	O	This active LOW output indicates that a data bus transfer is complete. A pull-up resistor is required at this output.
RX0-7	RX Input 0 to 7	I	Serial data input streams. These streams have 32 channels at data rates of 2.048 Mb/s.
$\overline{F0i}$	Frame Pulse	I	This input accepts and automatically identifies frame synchronization signals formatted according to different backplane specifications such as ST-BUS® and GCI.
$\overline{C4i}$	Clock	I	4.096 MHz serial clock for shifting data in and out of the data streams.
A0-A5	Address 0 to 5	I	These lines provide the address to IDT728985 internal registers.
DS	Data Strobe	I	This is the input for the active HIGH data strobe on the microprocessor interface. This input operates with $\overline{CS}$ to enable the internal read and write generation.
R/$\overline{W}$	Read/Write	I	This input controls the direction of the data bus lines (D0-D7) during a microprocessor access.
$\overline{CS}$	Chip Select	I	Active LOW input enabling a microprocessor read or write of control register or internal memories.
D0-D7	Data Bus 0 to 7	I/O	These pins provide microprocessor access to data in the internal control register. Connection Memory HIGH, Connection Memory LOW and data memory.
TX0-7	TX Outputs 0 to 7 (Three-state Outputs)	O	Serial data output streams. These streams are composed of 32, 64 Kbit/s channels at data rates of 2.048 Mb/s.
ODE	Output Drive Enable	I	This is an output enable for the TX0-7 serial outputs. If this input is LOW, TX0-7 are high-impedance. If this is HIGH, each channel may still be put into high-impedance by software control.
CCO	Control Channel Output	O	This output is a 2.048 Mb/s line which contains 256 bits per frame. The level of each bit is controlled by the contents of the CCO bit in the Connection Memory HIGH locations.

FUNCTIONAL DESCRIPTION (Cont'd)

eight output (TX0-7) serial streams are provided in the IDT728985 device allowing a complete 256 x 256 channel non-blocking switch matrix to be constructed. The serial interface clock for the device is 4.096 MHz, as required in ST-BUS® and GCI specifications.

The received serial data is internally converted to parallel by the on chip serial-to-parallel converters and stored sequentially in a 256-position Data Memory. By using an internal counter that is reset by the input 8 KHz frame pulse, $\overline{F0i}$, the incoming serial data streams can be framed and sequentially addressed.

Depending on the type of information to be switched, the IDT728985 device can be programmed to perform time slot interchange functions with different throughput delay capabilities on a per-channel basis. The Variable Delay mode, most commonly used for voice applications, can be selected ensuring minimum throughput delay between input and output data. In Constant Delay mode, used in multiple or grouped channel data applications, the integrity of the information through the switch is maintained.

CONNECTION MEMORY

Data to be output on the serial streams may come from two sources: Data Memory or Connection Memory. The Connection Memory is split into HIGH and LOW parts and is associated with particular TX output streams. In Processor Mode, data output on the TX streams is taken from the Connection Memory Low and originates from the microprocessor (Figure 2). Where as in Connection Mode (Figure 1), data is read from Data Memory and originated from the incoming RX streams. Data destined for a particular channel on the serial output stream is read internally during the previous channel time slot to allow time for memory access and internal parallel-to-serial conversion.

CONNECTION MODE

In Connection Mode, the addresses of input source for all output channels are stored in the Connection Memory Low. The Connection Memory Low locations are mapped to corresponding 8-bit x 32-channel outputs. The contents of the Data Memory at the selected address are then transferred to the parallel-to-serial converters before being output. By having the output channel to specify the input channel through the Connection Memory, the same input channel can be broadcast to several output channels.

PROCESSOR MODE

In Processor Mode the CPU writes data to the Connection Memory Low locations which correspond to the output link and channel number. The contents of the Connection Memory Low are transferred to the parallel-to-serial converter one channel before it is to be output and are transmitted each frame to the output until it is changed by the CPU.

CONTROL

The Connection Memory High bits (Table 4) control the per-channel functions available in the IDT728985. Output channels are selected into specific modes such as: Processor Mode or Connection mode, Variable or Constant throughput delay modes, Output Drivers Enabled or in three-state condition. There is also one bit to control the state of the CCO output pin.

OUTPUT DRIVE ENABLE (ODE)

The ODE pin is the master output three-state control pin. If the ODE input is held LOW all TDM (Time Division Multiplexed) outputs will be placed in high impedance regardless Connection Memory High programming. However, if ODE is HIGH, the contents of Connection Memory High control the output state on a per-channel basis.

SERIAL INTERFACE TIMING

The IDT728985 master clock ($\overline{C4i}$) is 4.096 MHz signal allowing serial data link configuration at 2.048 Mb/s to be implemented. The IDT728985 can automatically detect the presence of an input frame pulse, identify the type of backplane present on the serial interface, and format the synchronization pulse according to ST-BUS® or GCI interface specifications (active HIGH in GCI or active LOW in ST-BUS®). Upon determining the correct interface Connected to the serial port, the internal timing unit establishes the appropriate serial data bit transmit and sampling edges. In ST-BUS® mode, every second falling edge of the 4.096 MHz clock marks a boundary and the input data is clocked in by the rising edge, three quarters of the way into the bit cell. In GCI mode every second rising edge of the 4.096 MHz clock marks the bit boundary while data sampling is performed during the falling edge, at three quarters of the bit boundaries.

DELAY THROUGH THE IDT728985

The transfer of information from the input serial streams to the output serial streams results in a delay through the device. The delay through the IDT728985 device varies according to the mode selected in the $\overline{V}$/C bit of the Connection Memory High.

VARIABLE DELAY MODE

The delay in Variable Delay Mode is dependent only on the combination of source and destination on the input and output streams. The minimum delay achievable in the IDT728985 device is three time slots. In the IDT728985 device, the information that is to be output in the same channel position as the information is input (position n), relative to frame pulse, will be output in the following frame (channel n, frame n+1). The same occurs if the input channels succeeding (n+1, n+2) the channel position as the information is input.

The information switched to the third time slot after the input has entered the device (for instance, input channel 0 to output channel 3 or input channel 30 to output channel 1), is always output three channels later.

Any switching configuration that provides three or more time slots between input and output channels, will have a throughput delay equal to the difference
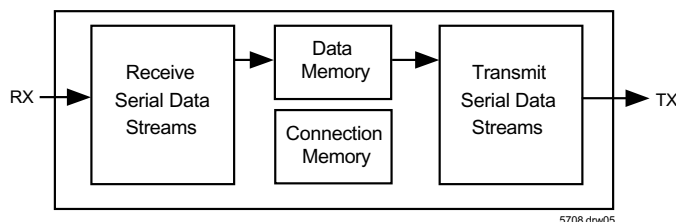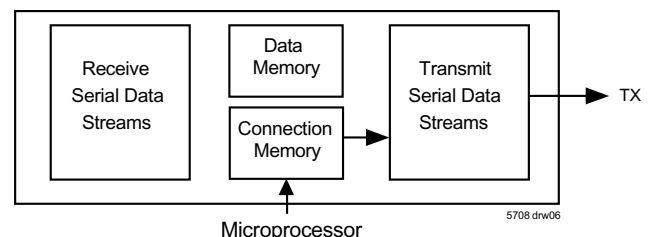

Figure 1. Connection Mode

Figure 2. Processor Mode

between the output and input channels; i.e., the throughput delay will be less than one frame. Table 1 shows the possible delays for the IDT728985 device in Variable Delay Mode. An example is shown in Figure 3.

CONSTANT DELAY MODE

In this mode frame integrity is maintained in all switching configurations by making use of a multiple Data Memory buffer technique where input channels written in any of the buffers during frame N will be read out during frame N+2. In the IDT728985, the minimum throughput delay achievable in Constant Delay mode will be 32 time slots; for example, when input time slot 32 (channel 31) is switched to output time slot 1 (channel 0). Likewise, the maximum delay is achieved when the first time slot in a frame (channel 0) is switched to the last time slot in the frame (channel 31), resulting in 94 time slots of delay (see Figure 4).

To summarize, any input time slot from input frame N will be always switched to the destination time slot on output frame N+2. In Constant Delay mode the device throughput delay is calculated according to the following formula:

$$DELAY = [32 + (32-IN) + (OUT-1)]$$

IN = the number of the input time slot (from 1 to 32)
OUT = the number of the output time slot (from 1 to 32).

MICROPROCESSOR PORT

The IDT728985 microprocessor port is a non-multiplexed bus architecture. The parallel port consists of an 8-bit parallel data bus (D0-D7), six address input lines (A0-A5) and four control lines ($\overline{CS}$, DS, R/$\overline{W}$ and $\overline{DTA}$). This parallel microport allows the access to the Control Registers, Connection Memory Low, Connection Memory High, and the Data Memory. All locations are read/written except for the Data Memory, which can be read only.

Accesses from the microport to the Connection Memory and the Data Memory are multiplexed with accesses from the input and output TDM ports. This can cause variable Data Acknowledge delays ($\overline{DTA}$). In the IDT728985 device, the $\overline{DTA}$ output provides a maximum acknowledgment delay of 800ns for read/write operations in the Connection Memory. However, for operations in the Data Memory (Processor Mode), the maximum acknowledgment delay can be 1220ns.

SOFTWARE CONTROL

If the A5, A1, A0 address line inputs are LOW then the IDT728985 Internal Control Register is addressed (see Table 2). If A5 input line is high, then the remaining address input lines are used to select the 32 possible channels per input or output stream. As explained in the Control Register description, the address input lines and the Stream Address bits (STA) of the Control register give the user the capability of selecting all positions of IDT728985 Data and Connect memories. See Figure 6 for accessing internal memories.

The data in the control register consists of Memory Select and Stream Address bits, Split Memory and Processor Enable bits (Table 3). In Split Memory

mode (Bit 7 of the Control register) reads are from the Data Memory and writes are to the Connection Memory LOW. The Memory Select bits allow the Connection Memory High or LOW or the Data Memory to be chosen, and the Stream Address bits define internal memory subsections corresponding to input or output streams.

The Processor Enable bit (bit 6) places every output channel on every output stream in Processor Mode; i.e., the contents of the Connection Memory LOW (CML, Table 5) are output on the output streams once every frame unless the ODE input pin is LOW. If PE bit is HIGH, then the IDT728985 behaves as if bits 2 (Channel Source) and 0 (Output Enable) of every Connection Memory High (CMH) locations were set to HIGH, regardless of the actual value. If PE is LOW, then bit 2 and 0 of each Connection Memory High location operates normally. In this case, if bit 2 of the CMH is HIGH, the associated TX output channel is in Processor Mode. If bit 2 of the CMH is LOW, then the contents of the CML define the source information (stream and channel) of the time slot that is to be switched to an output, Table 4.

If the ODE input pin is LOW, then all the serial outputs are high-impedance. If ODE is HIGH, then bit 0 (Output Enable) of the CMH location enables (if HIGH) or disables (if LOW) for that particular channel.
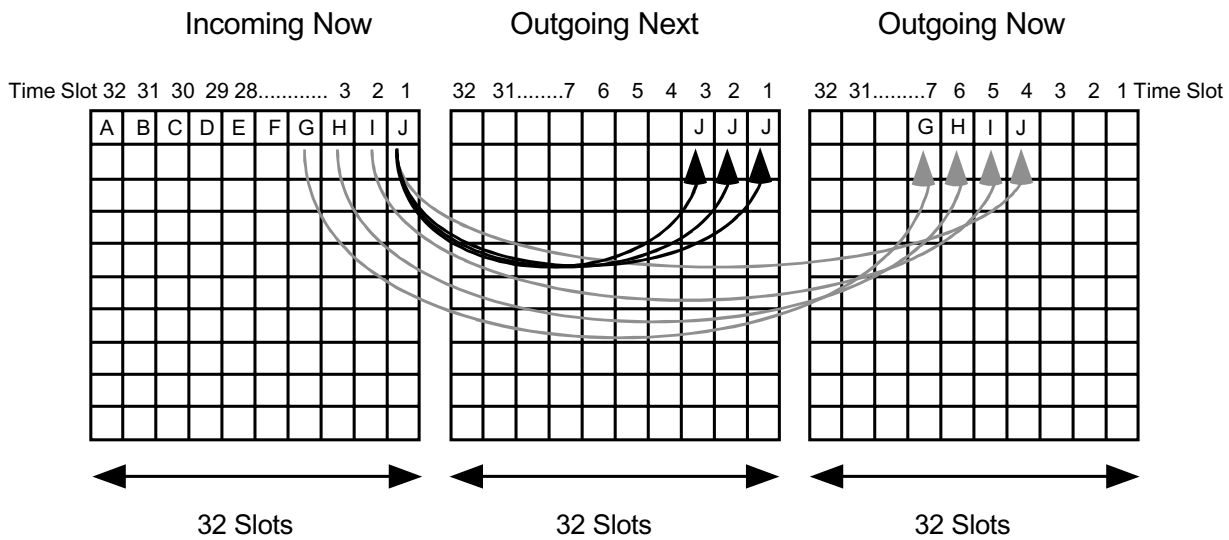
The contents of bit 1 (CCO) of each Connection Memory High Location (see Table 4) is output on CCO pin once every frame. The CCO pin is a 2.048 Mb/s output, which carries 256 bits. If CCO bit is set HIGH, the corresponding bit on CCO output is transmitted HIGH. If CCO is LOW, the corresponding bit on the CCO output is transmitted LOW. The contents of the 256 CCO bits of the CMH are transmitted sequentially on to the CCO output pin and are synchronous to the TX streams. To allow for delay in any external control circuitry the contents of the CCO bit is output one channel before the corresponding channel on the TX streams. For example, the contents of CCO bit in position 0 (corresponding to TX0, CH0), is transmitted synchronously with the TX channel 31, bit 7. Bit 1's of CMH for channel 1 of streams 0-7 are output synchronously with TX channel 0 bits 7-0.

INITIALIZATION

During the microprocessor initialization routine, the microprocessor should program the desired active paths through the matrices, and put all other channels into the high impedance state. Care should be taken that no two Connected TX outputs drive the bus simultaneously. The ODE pin should be held low on power up to keep all output pins in high-impedance. With the CMH setup, the microprocessor controlling the matrices can bring the ODE signal high to relinquish high impedance state control to the Connection Memory High bits outputs.

TABLE 1 — VARIABLE DELAY MODE

Input Channel	Output Channel	Throughput Delay
n	m=n, n+1 or n+2	m-n+32 time slot
n	m>n+2	m-n time slot
n	m<n	32-(n-m) time slot

TABLE 2 — ADDRESS MAPPING

A5	A4	A3	A2	A1	A0	LOCATION
0	X	X	X	0	0	Control Register[1]
1	0	0	0	0	0	Channel 0[2]
1	0	0	0	0	1	Channel 1[2]
1	.	.	.	.	.	.
1	.	.	.	.	.	.
1	.	.	.	.	.	.
1	.	.	.	.	.	.
1	.	.	.	.	.	.
1	1	1	1	1	1	Channel 31[2]

Incoming Now

Time Slot 32 31 30 29 28............ 3 2 1

| A | B | C | D | E | F | G | H | I | J |

32 Slots

Outgoing Next

32 31........7 6 5 4 3 2 1

| | | | | | | | J | J | J |

32 Slots

Outgoing Now

32 31.........7 6 5 4 3 2 1 Time Slot

| | | | G | H | I | J | | | |

32 Slots

For J: DELAY=3 Slots, 32 Slots, 33 Slots, and 34 Slots
For G, H, and I: DELAY= 3 slots

Figure 3. Variable Delay Mode

Incoming

Time Slot 32 31 30 29 28............ 3 2 1

| A | B | C | D | E | F | G | H | I | J |

32 Slots

Switching

32 Slots

Outgoing

32 31 30 29 28............. 3 2 1 Time Slot

| J | I | H | G | F | E | D | C | B | A |

32 Slots
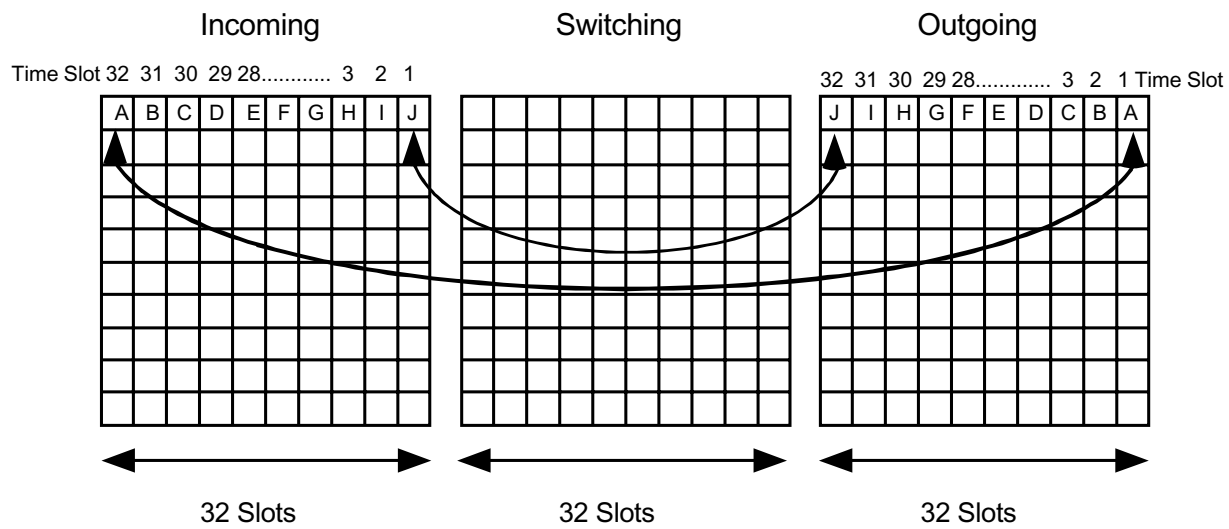
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For Slot 1 ("A"): IN=32, OUT=1, DELAY=(32-32)+32+(1-1)=32 time slots minimum delay
For Slot 32 ("J"): IN=1, OUT=32, DELAY=(32-1)+32+(32-1)=94 time slots maximum delay

Figure 4. Constant Delay Mode

Control Register	CR_b7	CR_b6	CR_b5	CR_b4	CR_b3	CR_b2	CR_b1	CR_b0

The Control Register is only accessed when A5=0. All other address bits have no effect when A5=0. When A5 =1, only 32 bytes are randomly accessable via A0-A4 at any one instant. Which 32 bytes are accessed is determined by the state of CRb0 -CRb4. The 32 bytes correlate to 32 channel of one ST-BUS® stream.
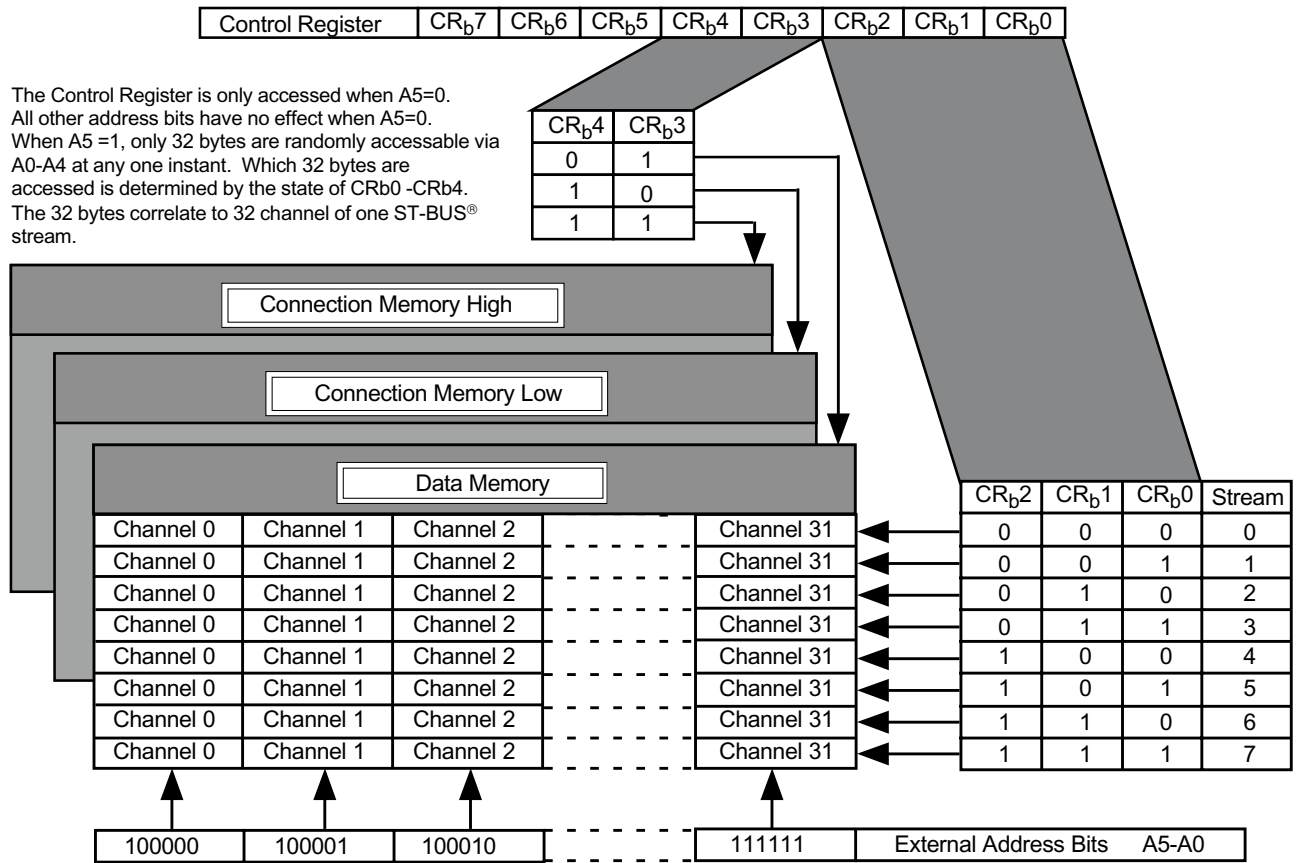
CR_b4	CR_b3
0	1
1	0
1	1

Connection Memory High

Connection Memory Low

Data Memory

					CR_b2	CR_b1	CR_b0	Stream
Channel 0	Channel 1	Channel 2	- - - -	Channel 31	0	0	0	0
Channel 0	Channel 1	Channel 2	- - - -	Channel 31	0	0	1	1
Channel 0	Channel 1	Channel 2	- - - -	Channel 31	0	1	0	2
Channel 0	Channel 1	Channel 2	- - - -	Channel 31	0	1	1	3
Channel 0	Channel 1	Channel 2	- - - -	Channel 31	1	0	0	4
Channel 0	Channel 1	Channel 2	- - - -	Channel 31	1	0	1	5
Channel 0	Channel 1	Channel 2	- - - -	Channel 31	1	1	0	6
Channel 0	Channel 1	Channel 2	- - - -	Channel 31	1	1	1	7

100000	100001	100010	- - - -	111111	External Address Bits A5-A0

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Figure 6. Addressing Internal Memories

TABLE 3 — CONTROL REGISTER

7	6	5	4	3	2	1	0
SM	PE	X	MS1	MS0	STA2	STA1	STA0

Bit	Name	Description
7	SM (Split Memory)	When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory, except when the Control Register is accessed again. The Memory Select bits need to specify the memory for the operations.
6	PE (Processor Mode)	When 1, the contents of the Connection Memory LOW are output on the Serial Output streams except when in high-impedance. When 0, the Connection Memory bits for each channel determine what is output.
5		unused
4-3	MS1-MS0 (Memory Select Bits)	0-0 - Not to be used. 0-1 - Data Memory (read only from the CPU) 1-0 - Connection Memory LOW 1-1 - Connection Memory is HIGH
2-0	STA2-0 (Stream Address Bits)	The number expressed in binary notation on these bits refers to the input or output stream which corresponds to the subsection of memory made accessible for subsequent operations.

x = don't care

TABLE 4 — CONNECTION MEMORY HIGH

7	6	5	4	3	2	1	0
X	$\overline{V}$/C	X	X	X	CS	CCO	OE

Bit	Name	Description
7,5,4,3		unused
6	$\overline{V}$/C (Variable/Constant Throughput Delay Mode)	This bit is used to select between Variable (LOW) and Constant Delay (HIGH) modes on a per-channel basis.
2	CS (Channel Source)	When 1, the contents of the corresponding location in Connection Memory LOW are output on the location's channel and stream. When 0, the contents of the corresponding location in Connection Memory LOW act as an address for the Data Memory and determine the source of the connection to the location's channel and stream.
1	CCO (CCO Bit)	This bit drives a bit time on the CCO output pin.
0	OE (Output Enable)	This bit enables the output drivers on a per-channel basis. This allows individual channels on individual streams to be made high-impedance, allowing switch matrices to be constructed. A HIGH enables the driver and a LOW disables it.

x = don't care

TABLE 5 — CONNECTION MEMORY LOW

7	6	5	4	3	2	1	0
SAB2	SAB1	SAB0	CAB4	CAB3	CAB2	CAB1	CAB0

Bit	Name	Description
7-5	SAB2-0[1] (Source Stream Address Bits)	These three bits are used to select eight source streams for the Connection.
4-0[1]	CAB2-0[1] (Source Channel Address Bits)	These five bits are used to select 32 different source channels for the Connection (the stream where the channel is present is defined by bits SAB2-0). Bit 4 is the most significant bit.

NOTE:
1. If bit 2 of the corresponding Connection HIGH location is 1 or bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise, the bits are used as indicated to define the source of the Connection which is output on the channel and stream associated with this location.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Min.	Max.	Unit
	Vcc - GND	-0.3	7	V
Vi	Voltage on Digital Inputs	GND - 0.3	Vcc +0.3	V
Vo	Voltage on Digital Outputs	GND - 0.3	Vcc +0.3	V
Io	Current at Digital Outputs		40	mA
Ts	Storage Temperature	-65	+150	°C
Pd	Package Power Dissapation		2	W

NOTE:

1. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

| Symbol	Parameter	Min.	Typ.[1]	Max.	Unit
Vcc	Positive Supply	4.75	5.0	5.25	V
Vi	Input Voltage	0	—	Vcc	V
Top	Operating Temperature Commercial	-40	25	+85	°C

NOTE:

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.[1]	Max.	Units	Test Conditions
Icc	Supply Current	—	7	10	mA	Outputs Unloaded
Vih	Input High Voltage	2.0	—	—	V	
Vil	Input Low Voltage	—	—	0.8	V	
Iil	Input Leakage (Inputs)	—	—	5	μA	Vi between GND and Vcc
Iil	Input Leakage (I/O pins)	—	34	100	μA	
Ci	Input Capacitance	—	8	—	pF	
Voh	Output High Voltage	2.4	—	—	V	Ioh = 10mA
Ioh	Output High Current	10	15	—	mA	Sourcing. Voh = 2.4V
Vol	Output Low Voltage	—	—	0.4	V	Iol = 5mA
Iol	Output Low Current	5	10	—	mA	Sinking. Vol = 0.4V
Ioz	High Impedance Leakage	—	—	5	μA	Vo between GND and Vcc
Co	Output Pin Capacitance	—	8	—	pF	

NOTE:

1. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
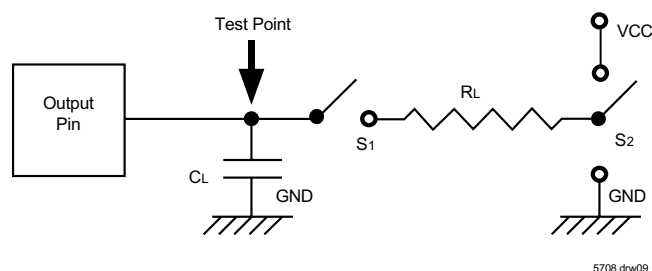
S1 is open circuit except when testing output levels or high impedance states.

S2 is switched to Vcc or GND when testing output levels or high impedance states.

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Figure 6. Output Load

AC ELECTRICAL CHARACTERISTICS[1] — ST-BUS® TIMING

Symbol	Parameter	Min.	Typ.[2]	Max.	Units	Test Conditions
t_{F0iW}	Frame Pulse Width	—	244	—	ns	Outputs Loaded
t_{F0iS}	Frame Pulse Setup Time	10	—	190	ns	
t_{F0iH}	Frame Pulse Hold Time	20	—	190	ns	
t_{DAA}	TX delay Active to Active	—	40	60	ns	C_L = 150pF
t_{STiS}	RX Setup Time	20	—	—	ns	
t_{STiH}	RX Hold Time	20	—	—	ns	
t_{C4i}	Clock Period	200	244	300	ns	
t_{CL}	CK Input Low	85	122	150	ns	
t_{CH}	CK Input High	85	122	150	ns	
t_r, t_f	Clock Rise/Fall Time	—	—	10	ns	

NOTE:

1. Timing is over recommended temperature and power supply voltages (Vcc=5V±5%, GND=0V, TA=40°C to 85°C).
2. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
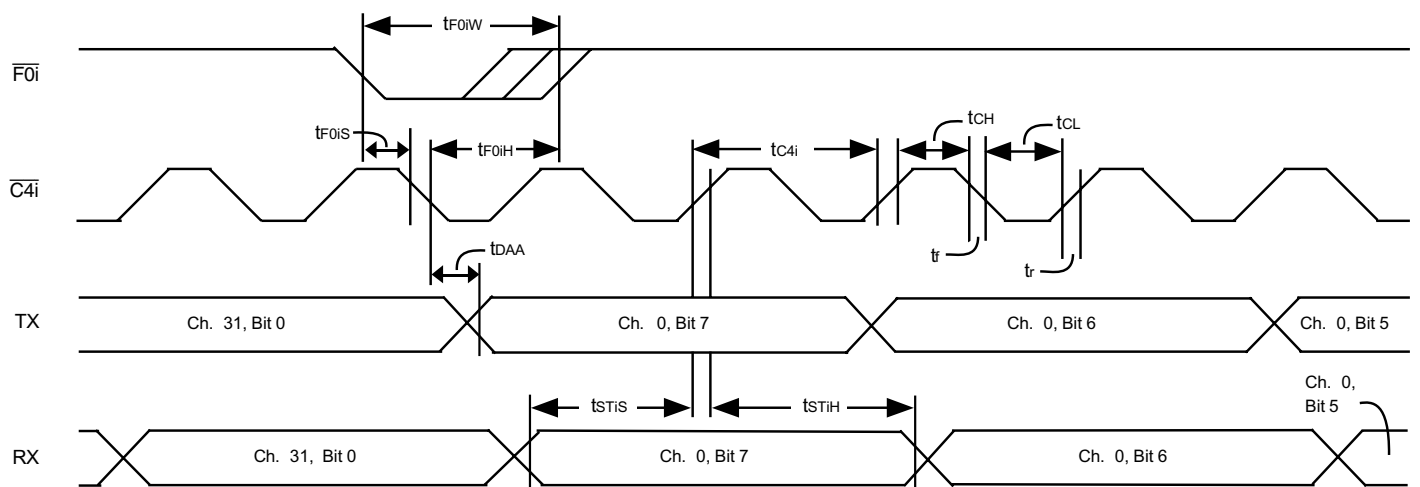

Figure 7. ST-BUS® Timing

AC ELECTRICAL CHARACTERISTICS[1] — GCI TIMING

Symbol	Parameter	Min.	Typ.[2]	Max.	Units	Test Conditions
t_{C4i}	Clock Period	150	244	300	ns	Outputs Loaded
t_{CL}, t_{CH}	Pulse Width	73	122	150	ns	
t_{WFH}	Frame Width High	—	244	—	ns	
t_{F0iS}	Frame Setup	10	—	190	ns	
t_{F0iH}	Frame Hold	20	—	190	ns	
t_{DAA}	Data Delay/Clock Active to Active	—	40	60	ns	$C_L = 150pF$
t_{STiS}	Serial Input Setup	20	—	—	ns	
t_{STiH}	Serial Input Hold	20	—	—	ns	
t_r, t_f	Clock Rise/Fall Time	—	—	10	ns	

NOTE:

1. Timing is over recommended temperature and power supply voltages (V_{CC}=5V±5%, GND=0V, TA=40°C to 85°C).
2. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
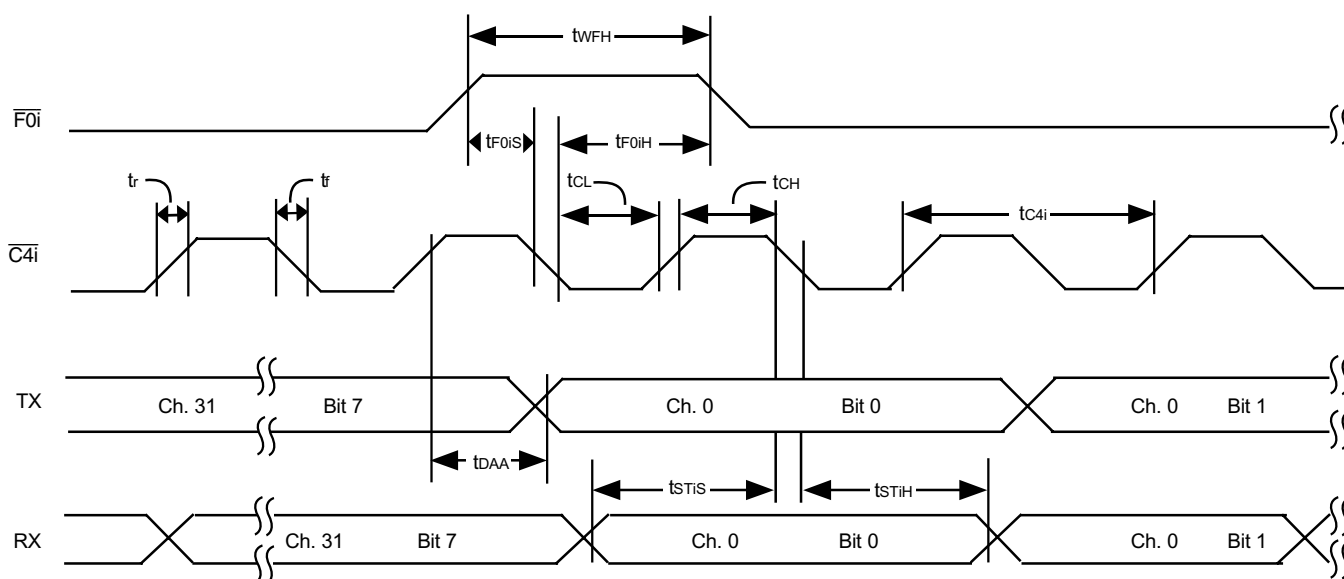
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Figure 8. GCI Timing

AC ELECTRICAL CHARACTERISTICS[1] — SERIAL STREAM TIMING

Symbol	Characteristics	Min.	Typ.[2]	Max.	Unit	Test Conditions
t_{TAZ}	TX0-7 Delay - Active to High Z	—	40	60	ns	$R_L = 1K\Omega$[3], $C_L = 150pF$
t_{TZA}	TX0-7 Delay - High Z to Active	—	40	60	ns	$C_L = 150pF$
t_{OED}	Output Driver Enable Delay	—	40	60	ns	$R_L = 1K\Omega$[3], $C_L = 150pF$
t_{XCD}	CCO Output Delay	0	20	40	ns	$C_L = 150pF$

NOTE:

1. Timing is over recommended temperature and power supply voltages.
2. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
3. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.
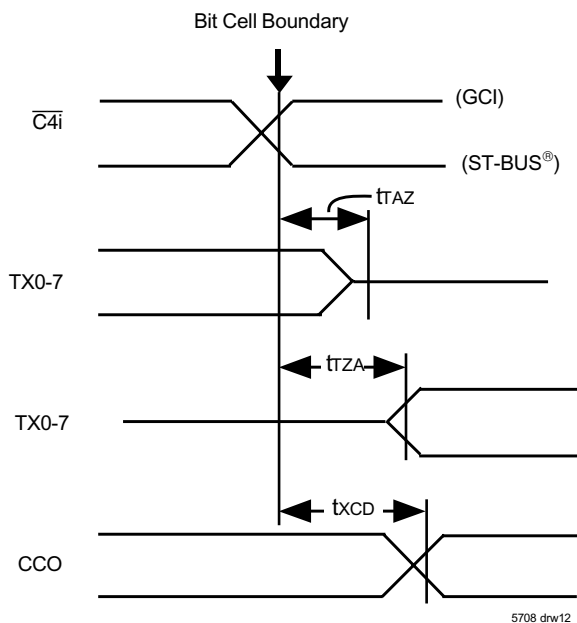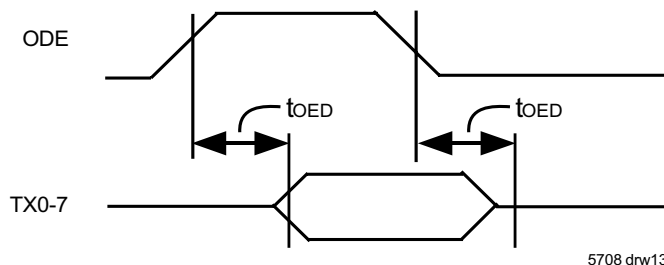

Figure 9. Serial Outputs and External Control

Figure 10. Output Driver Enable

AC ELECTRICAL CHARACTERISTICS[1] — MICROPROCESSOR TIMING

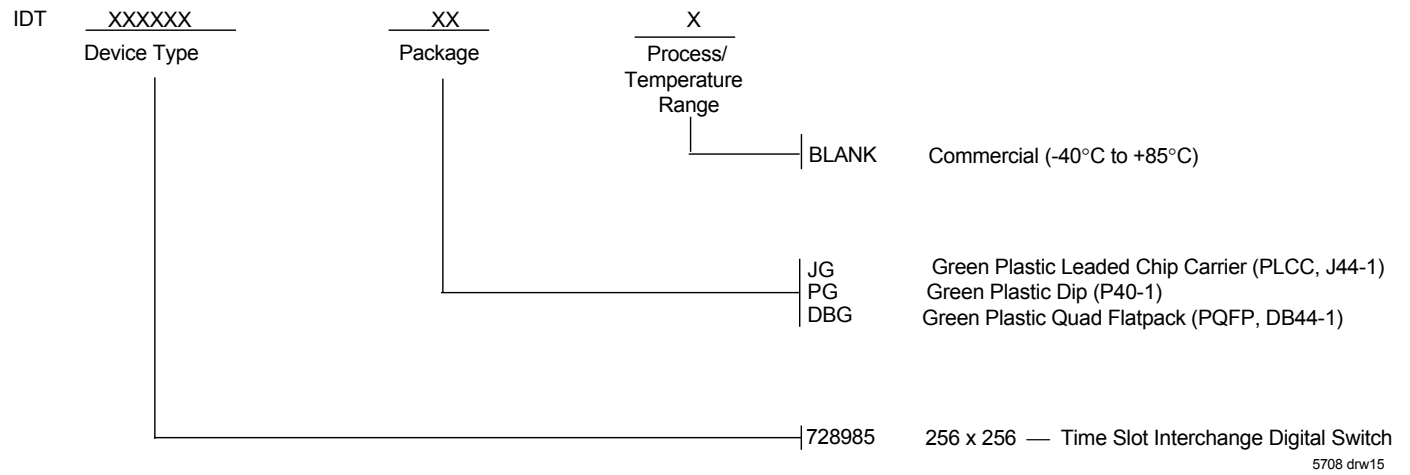| Symbol	Characteristics	Min.	Typ.[2]	Max.	Unit	Test Conditions
t_{CSS}	$\overline{CS}$ Setup from DS Rising	0	—	—	ns	
t_{RWS}	R/$\overline{W}$ Setup from DS Rising	5	—	—	ns	
t_{ADS}	Add Setup from DS Rising	5	—	—	ns	
t_{CSH}	$\overline{CS}$ Hold after DS Falling	0	—	—	ns	
t_{RWH}	R/$\overline{W}$ Hold after DS Falling	5	—	—	ns	
t_{ADH}	Add Hold after DS Falling	5	—	—	ns	
t_{DDR}	Data Setup from $\overline{DTA}$ Low on Read	10	—	—	ns	C_L = 150pF
t_{DHR}	Data Hold on Read	10	50	90	ns	R_L = 1KΩ[3], C_L = 150pF
t_{DSW}	Data Setup on Write (Fast Write)	10	—	—	ns	
t_{SWD}	Valid Data Delay on Write (Slow Write)	—	—	122	ns	
t_{DHW}	Data Hold on Write	8	—	—	ns	
t_{AKD}	Acknowledgment Delay: Reading Data Memory Reading/Writing Connection Memory Writing to Control Register Reading to Control Register	— — — —	 560 300/370 40 40	 1220 730/800 70 70	 ns ns ns ns	C_L = 150pF
t_{AKH}	Acknowledgment Hold Time	10	20	50	ns	R_L = 1KΩ[3], C_L = 150pF

NOTE:

1. Timing is over recommended temperature and power supply voltages.
2. Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
3. High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.
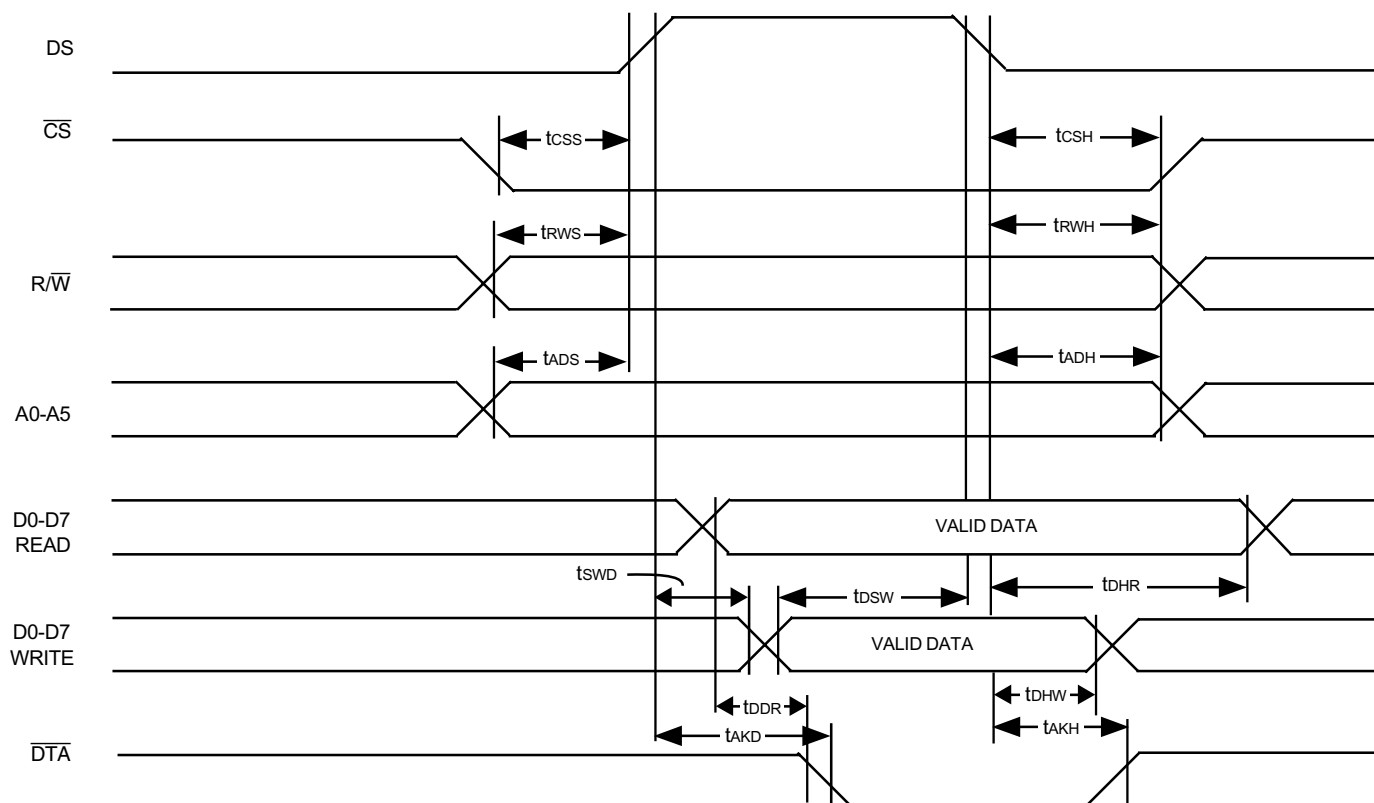
Figure 11. Motorola Non-Multiplexed Bus Timing

ORDERING INFORMATION

```
IDT    XXXXXX              XX            X
      Device Type         Package     Process/
                                     Temperature
                                       Range
```

BLANK   Commercial (-40°C to +85°C)

JG   Green Plastic Leaded Chip Carrier (PLCC, J44-1)
PG   Green Plastic Dip (P40-1)
DBG   Green Plastic Quad Flatpack (PQFP, DB44-1)

728985   256 x 256 — Time Slot Interchange Digital Switch

5708 drw15

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