## 5-Pin Voltage Supervisors with Adjustable Power-On Reset, Dual Voltage Monitoring or Watchdog Timer Capability

The ISL88011 - ISL88015 family of devices offer both fixed and/or adjustable voltage-monitoring that combine popular functions such as Power On Reset control, Watchdog Timer, Supply Voltage Supervision, and Manual Reset assertion in a small 5-pin SOT23 package.

Unique features on the ISL88013 and ISL88015 include a watchdog timer with a 51sec startup timeout and a 1.6sec normal timeout duration. On the ISL88011 and ISL88014, users can increase the nominal 200ms Power On Reset timeout delay by adding an external capacitor to the $C_{POR}$ pin. Both fixed and adjustable voltage monitors are provided by the ISL88012. Complementary active-low and active-high reset outputs are available on the ISL88011, ISL88012 and ISL88013 devices. All devices provide manual reset capability (see Product Features Table).

Seven preprogrammed reset threshold voltages accurate to ±1.5% over temperature are offered (see Ordering Information). The ISL88012, ISL88014 and ISL88015 have a user-adjustable voltage input available for custom monitoring of any voltage down to 0.6V. All parts are specifically designed for low power consumption and high threshold accuracy.

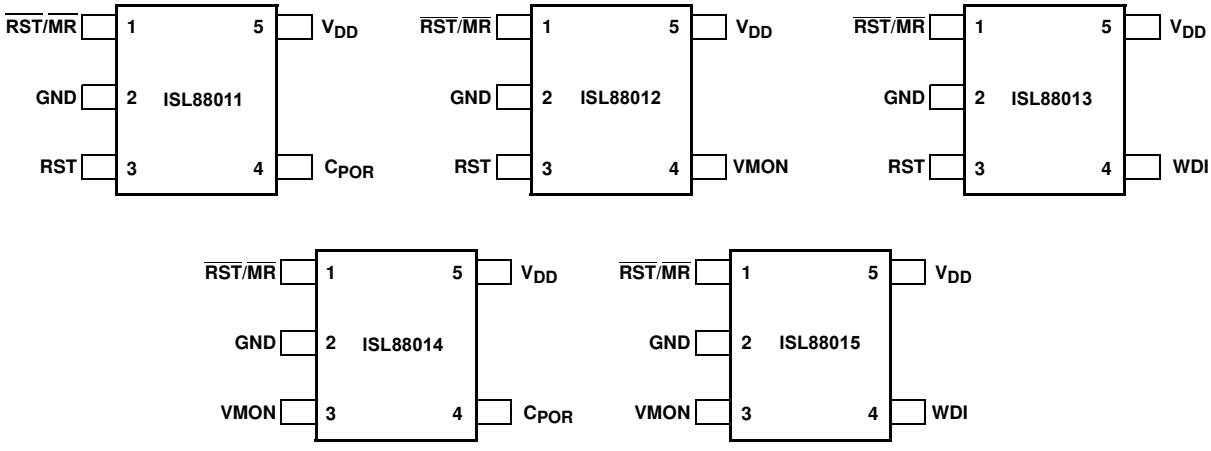
## Features

- Single/Dual Voltage Monitoring Supervisors
- Fixed-Voltage Options Allow Precise Monitoring of +2.5V, +3.0V, +3.3V, and +5.0V Power Supplies
- Dual Supervisor Has One Fixed Voltage Input and Another That is User-Adjustable Down to 0.6V.
- Both RST and $\overline{RST}$ Outputs Available
- Adjustable POR Timeout Delay Options
- Watchdog Timer With 1.6sec Normal and 51sec Startup Timeout Durations
- Manual Reset Input on All Devices
- Reset Signal Valid Down to $V_{DD}$ = 1V
- Accurate ±1.5% Voltage Threshold
- Immune to Power-Supply Transients
- Ultra Low 5.5µA Supply Current
- Small 5-pin SOT-23 Pb Free package
- Pb-Free Plus Anneal Available (RoHS Compliant)

## Applications

- Process Control Systems
- Intelligent Instruments
- Embedded Control Systems
- Computer Systems
- Critical µP and µC Power Monitoring
- Portable/Battery-Powered Equipment
- PDA and Handheld PC Devices

## Pinouts *(ordering information on next page)*



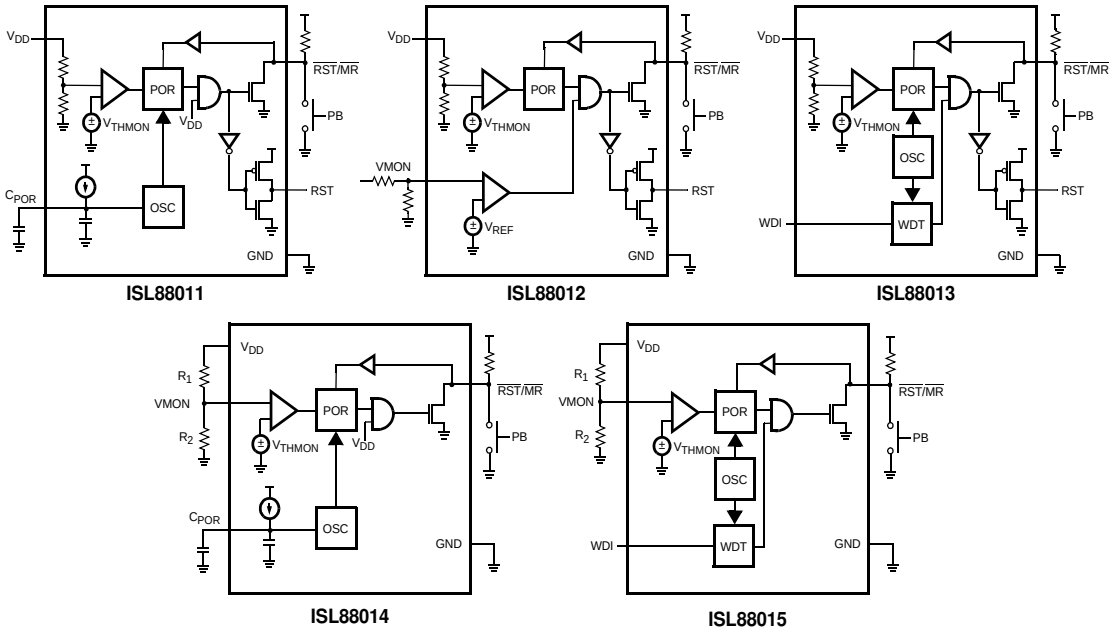
## Ordering Information

| | PART NUMBER (Notes 1, 2) | MARKING | $V_{THVDD}$ | $V_{THVMON}$ | TEMPERATURE RANGE (°C) | PACKAGE (Pb-free) |
|---|---|---|---|---|---|---|
| ISL88011 | ISL88011IH546Z | AGU | 4.64V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88011IH544Z | AGV | 4.38V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88011IH531Z | AGW | 3.09V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88011IH529Z | AGX | 2.92V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88011IH526Z | AGY | 2.63V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88011IH523Z | AGZ | 2.32V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88011IH522Z | AHE | 2.19V | N/A | -40 to +85 | 5 Ld SOT23 |
| ISL88012 | ISL88012IH546Z | AHF | 4.64V | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |
| | ISL88012IH544Z | AHG | 4.38V | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |
| | ISL88012IH531Z | AHH | 3.09V | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |
| | ISL88012IH529Z | AHI | 2.92V | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |
| | ISL88012IH526Z | AHJ | 2.63V | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |
| | ISL88012IH523Z | AHK | 2.32V | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |
| | ISL88012IH522Z | AHL | 2.19V | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |
| ISL88013 | ISL88013IH546Z | AHM | 4.64V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88013IH544Z | AHN | 4.38V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88013IH531Z | AHO | 3.09V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88013IH529Z | AHP | 2.92V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88013IH526Z | AHQ | 2.63V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88013IH523Z | AHR | 2.32V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88013IH522Z | AHS | 2.19V | N/A | -40 to +85 | 5 Ld SOT23 |
| | ISL88014IH5Z | AHT | N/A | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |
| | ISL88015IH5Z | AHU | N/A | 0.6V (Note 3) | -40 to +85 | 5 Ld SOT23 |

NOTES:

1. Add “-TK” suffix for Tape and Reel
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. The voltage trip point can be adjusted to be greater than 0.6V using 2 external resistors. By default, the $V_{THVMON}$ trip point is 0.6V if no external resistors are used.

## Functional Block Diagrams




## Product Features Table

| FUNCTION | ISL88011 | ISL88012 | ISL88013 | ISL88014 | ISL88015 |
|---|---|---|---|---|---|
| Active-Low Reset ($\overline{RST}$) | x | x | x | x | x |
| Active-High Reset (RST) | x | x | x | | |
| Watchdog Timer (WDI) | | | x | | x |
| Dual Voltage Supervision | | x | | | |
| Adjustable POR Timeout ($C_{POR}$) | x | | | x | |
| Manual Reset Input ($\overline{MR}$) | x | x | x | x | x |
| Fixed Trip Point Voltage | x | x | x | | |
| Adjustable Trip Point Voltage | | x | | x | x |

## Pin Descriptions

| PIN | | | | | NAME | FUNCTION |
|---|---|---|---|---|---|---|
| ISL88011 | ISL88012 | ISL88013 | ISL88014 | ISL88015 | | |
| 1 | 1 | 1 | 1 | 1 | $\overline{RST}/\overline{MR}$ | Combined Active-Low Reset Output and Manual Reset Input |
| 2 | 2 | 2 | 2 | 2 | GND | Ground |
| | 4 | | 3 | 3 | VMON | Adjustable Threshold Voltage Input |
| 3 | 3 | 3 | | | RST | Active-High Reset Output |
| 4 | | | 4 | | $C_{POR}$ | Adjustable POR Timeout Delay Input |
| | | 4 | | 4 | WDI | Watchdog Timer Input |
| 5 | 5 | 5 | 5 | 5 | $V_{DD}$ | Supply Voltage and Monitored Input |

## Absolute Maximum Ratings

Temperature under bias . . . . . -40°C to +125°C
Storage temperature . . . . . -65°C to +150°C
Voltage on any pin with respect to GND . . . . . -1.0V to +7V
D.C. output current. . . . . 5mA
Lead temperature (soldering, 10 seconds) . . . . . 300°C

## Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to 85°C
Pull-up Resistance ($R_{PU}$) . . . . . 5kΩ to 100kΩ

## Recommended Operating Conditions

Thermal Resistance (Typical, Note 4) $\theta_{JA}$ (°C/W)
5 Ld SOT-23. . . . . 190
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(SOT-23 Lead Tips Only)

*CAUTION: Absolute Maximum Ratings indicate limits beyond which permanent damage to the device and impaired reliability may occur. These are stress ratings provided for information only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied.*

*For guaranteed specifications and test conditions, see Electrical Specifications. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.*

NOTE:

4. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

## Electrical Specifications

Over the recommended operating conditions unless otherwise specified, $R_{PU}$ = 10kΩ.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | | 2.0 | | 5.5 | V |
| $I_{DD}$ | Supply Current for ISL88011, ISL88012, ISL88013 | $V_{DD}$ = 5.0V | | 8 | 11.5 | µA |
| | | $V_{DD}$ = 3.3V | | 7 | 10 | µA |
| | | $V_{DD}$ = 2.5V | | 5.5 | 9 | µA |
| | Supply Current for ISL88014/15 | $V_{DD}$ = 3.3V | | 4.5 | 8 | µA |
| $I_{LI}$ | Input Leakage Current (VMON) | | | | 100 | nA |
| $I_{LO}$ | Output Leakage Current (VMON) | | | | 100 | nA |
| **VOLTAGE THRESHOLDS** | | | | | | |
| $V_{THVDD}$ | Fixed $V_{DD}$ Voltage Trip Point | ISL88011, 88012, 88013IH5**46** | 4.57 | 4.64 | 4.71 | V |
| | | ISL88011, 88012, 88013IH5**44** | 4.31 | 4.38 | 4.45 | V |
| | | ISL88011, 88012, 88013IH5**31** | 3.04 | 3.09 | 3.14 | V |
| | | ISL88011, 88012, 88013IH5**29** | 2.88 | 2.92 | 2.96 | V |
| | | ISL88011, 88012, 88013IH5**26** | 2.59 | 2.63 | 2.67 | V |
| | | ISL88011, 88012, 88013IH5**23** | 2.29 | 2.32 | 2.35 | V |
| | | ISL88011, 88012, 88013IH5**22** | 2.16 | 2.19 | 2.22 | V |
| $V_{THVDD}$ HYST | Hysteresis at $V_{DD}$ Input | $V_{THVDD}$ = 4.64V | | 46 | | mV |
| | | $V_{THVDD}$ = 4.38V | | 44 | | mV |
| | | $V_{THVDD}$ = 3.09V | | 31 | | mV |
| | | $V_{THVDD}$ = 2.92V | | 29 | | mV |
| | | $V_{THVDD}$= 2.63V | | 26 | | mV |
| | | $V_{THVDD}$ = 2.32V | | 23 | | mV |
| | | $V_{THVDD}$ = 2.19V | | 22 | | mV |
| $V_{THVMON}$ | Adj. Reset Voltage Trip Point (Note 5) | $V_{THVDD}$ = 4.64V | 599 | 605 | 611 | mV |
| | | $V_{THVDD}$ = 4.38V | 597 | 603 | 609 | mV |
| | | $V_{THVDD}$ = 3.09V | 589 | 595 | 601 | mV |
| | | $V_{THVDD}$ = 2.92V | 589 | 595 | 601 | mV |
| | | $V_{THVDD}$= 2.63V | 589 | 595 | 601 | mV |
| | | $V_{THVDD}$ = 2.32V | 597 | 603 | 609 | mV |
| | | $V_{THVDD}$ = 2.19V | 597 | 603 | 609 | mV |

**Electrical Specifications** Over the recommended operating conditions unless otherwise specified, $R_{PU}$ = 10kΩ **(Continued)**

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{THVMON\ HYST}$ | Hysteresis Voltage (Note 5) | | | 3 | | mV |
| **RESET** | | | | | | |
| $V_{OL}$ | Reset Output Voltage Low | $V_{DD} \geq 3.3V$, Sinking 0.5mA | | 0.05 | 0.40 | V |
| | | $V_{DD} < 3.3V$, Sinking 0.5mA | | 0.05 | 0.40 | V |
| $V_{OH}$ | Reset Output Voltage High | $V_{DD} \geq 3.3V$, Sourcing 0.4mA | $V_{DD}$-0.6 | $V_{DD}$-0.4 | | V |
| | | $V_{DD} < 3.3V$, Sourcing 0.4mA | $V_{DD}$-0.6 | $V_{DD}$-0.4 | | V |
| $t_{RPD}$ | $V_{TH}$ to Reset Asserted Delay | | | 6 | | µs |
| $t_{POR}$ | POR Timeout Delay | ISL88012, ISL88013, ISL88015 | 140 | 200 | 260 | ms |
| | | ISL88011, ISL88014 with $C_{POR}$ = OPEN | 200 | 250 | | ms |
| $C_{LOAD}$ | Load Capacitance on Reset Pins | | | 5 | | pF |
| **MANUAL RESET** | | | | | | |
| $V_{MR}$ | $\overline{MR}$ Input Voltage | | 0 | | 100 | mV |
| $t_{MR}$ | $\overline{MR}$ Minimum Pulse Width | | 1 | | | µs |
| **WATCHDOG TIMER (Note 6)** | | | | | | |
| Start $t_{WDT}$ | Startup Watchdog Timeout Period | | 32 | 51 | 64 | sec |
| $t_{WDT}$ | Normal Watchdog Timeout Period | | 1.0 | 1.6 | 2.0 | sec |
| $t_{WDPS}$ | WDI Minimum Pulse Width | | 100 | | | ns |
| $V_{IL}$ | Watchdog Input Voltage Low | | | | 0.3 x $V_{DD}$ | V |
| $V_{IH}$ | Watchdog Input Voltage High | | 0.85 x $V_{DD}$ | | | V |
| $I_{WDT}$ | Watchdog Input Current | | | | 100 | nA |

NOTES:

5. Applies to ISL88012, ISL88014, and ISL88015.
6. Applies to ISL88013 and ISL88015.

## Pin Description

### RST

The push-pull RST output is set to $V_{DD}$ (HIGH) whenever 1) the device is first powered up, 2) either $V_{DD}$ or the voltage on VMON falls below their respective minimum voltage sense levels, 3) $\overline{MR}$ is asserted or 4) the watchdog timeout expires.

### $\overline{RST}$/$\overline{MR}$

This pin functions as both a reset output and a manual reset input. The $\overline{RST}$ output functions identically to the complementary RST output but is an open drain output that is pulled to GND (LOW) when reset is asserted. The $\overline{MR}$ input is an active-low debounced input to which a user can connect a push-button to add manual reset capability or drive with active low signal from a controller.

### $V_{DD}$

The $V_{DD}$ pin is the power supply terminal. It is monitored by the ISL88011, ISL88012 and ISL88013. For these devices, the voltage at this pin is compared against an internal factory-programmed voltage trip point, $V_{THVDD}$. A reset is first asserted when the device is initially powered up to ensure that the power supply has stabilized. Thereafter, reset is again asserted whenever $V_{DD}$ falls below $V_{THVDD}$. The device is designed with hysteresis to help prevent chattering due to noise.

### VMON

The VMON pin on the ISL88012, ISL88014 and ISL88015 is a monitored input voltage that is user-adjustable. The voltage at this pin is compared against an internal 600mV reference voltage ($V_{THVMON}$) and a reset is asserted whenever the monitored voltage falls below this trip point.

### WDI

The Watchdog Input takes an input from a microprocessor and ensures that it periodically toggles the WDI pin, otherwise the internal watchdog timer runs out and reset is asserted. The internal Watchdog Timer is cleared whenever the WDI input pin sees a rising or falling edge or the device is manually reset.

### $C_{POR}$

The $C_{POR}$ input pin lets users increase the Power On Reset timeout delay ($t_{POR}$) by connecting a capacitor between $C_{POR}$ and ground. (See Figure 3)

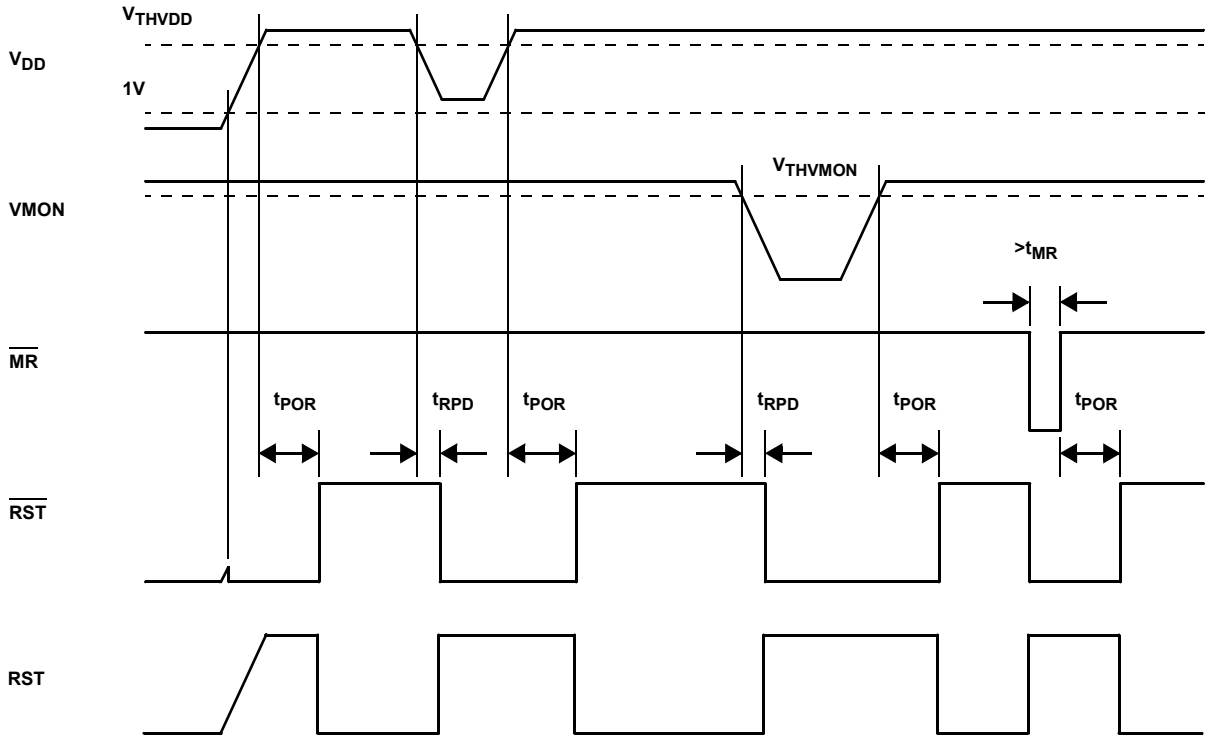



**FIGURE 1. VOLTAGE MONITORING TIMING DIAGRAM**

## Principles of Operation

The ISL88011 - ISL88015 devices provide those functions needed for critical voltage monitoring. These features include Power On Reset control, customizable supply voltage supervision, Watchdog Timer capability, and manual reset assertion. By integrating all of these features into a small 5-pin SOT23 package and using only 5.5µA of supply current, the ISL88011 - ISL88015 devices can assist in lowering system cost, reducing board space requirements, and increasing the reliability of a system.

### Low Voltage Monitoring

During normal operation, these supervisors monitor both the voltage level of $V_{DD}$ (ISL88011,12,13) and/or VMON (ISL88012,14,15). The device asserts a reset if any of these voltages falls below their respective trip points. The reset signal effectively prevents the system from operating during a power failure or brownout condition. This reset signal remains asserted until $V_{DD}$ and the voltage on VMON exceed their voltage threshold setting for the reset time delay period $t_{POR}$ of 200ms (See Figure 1).

The ISL88012, ISL88014 and ISL88015 allow users to customize the minimum voltage sense level on the VMON input pin. To do this, connect an external resistor divider network to the VMON pin in order to set the trip point to some voltage above 600mV according to the following equation (See Figure 2):

$$V_{INTRIP} = 0.6 \times \frac{(R_1 + R_2)}{R_2} \quad \text{(EQ. 1)}$$

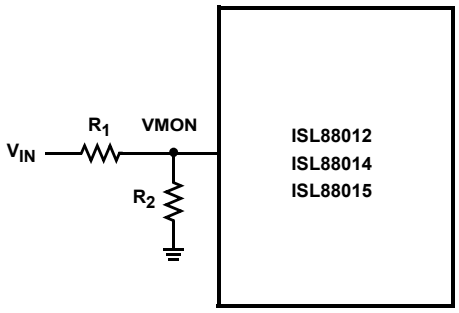



**FIGURE 2. USING VMON TO MONITOR $V_{IN}$ VIA RESISTORS**

### Power On Reset (POR)

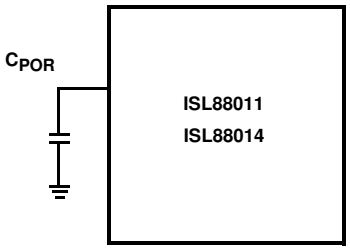
Applying at least 1V to the $V_{DD}$ pin activates a POR circuit which asserts reset (i.e. RST goes HIGH while $\overline{RST}$ goes LOW). The reset signals remain asserted until the voltage at $V_{DD}$ and / or VMON rise above the minimum voltage sense level for time period $t_{POR}$. This ensures that the voltages have stabilized.

These reset signals provide several benefits:

- It prevents the system microprocessor from starting to operate with insufficient voltage.
- It prevents the processor from operating prior to stabilization of the oscillator.
- It ensures that the monitored device is held out of operation until internal registers are properly loaded.
- It allows time for an FPGA to download its configuration prior to initialization of the circuit.

### Adjusting POR Timeout via $C_{POR}$ Pin

On the ISL88011 and ISL88014, users can adjust the Power On Reset timeout delay ($t_{POR}$) up to many times the normal $t_{POR}$ of 250ms. To do this, connect a capacitor between $C_{POR}$ and ground (see Figure 3). For example, connecting a 30pF capacitor to $C_{POR}$ will increase $t_{POR}$ from a typical 250ms to about 2.5sec. **NOTE:** Care should be taken in PCB layout and capacitor placement in order to reduce stray capacitance as much as possible, which lengthens the $t_{POR}$ timeout period.



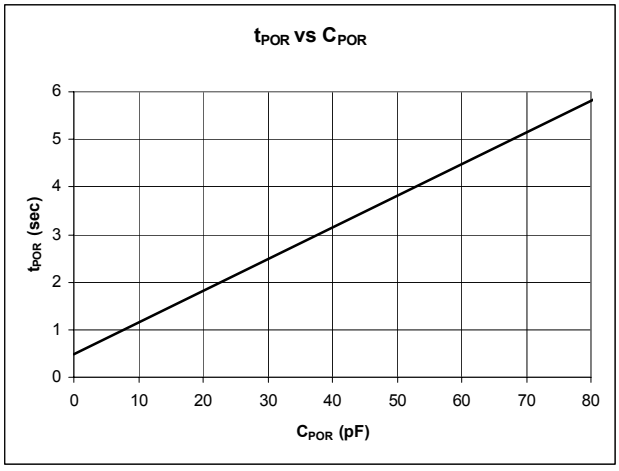




**FIGURE 3. ADJUSTING $t_{POR}$ WITH A CAPACITOR**

### Manual Reset

The manual reset input ($\overline{MR}$) allows the user to trigger a reset by using a push-button switch. The $\overline{MR}$ input is an active-low debounced input. By connecting a push-button directly from $\overline{MR}$ to ground, the designer adds manual system reset capability (see Figure 4). Reset is asserted if the $\overline{MR}$ pin is pulled low to less than 100mV for 1µs or longer while the push-button is closed. After $\overline{MR}$ is released, the reset outputs remain asserted for $t_{POR}$ (200ms) and then released.

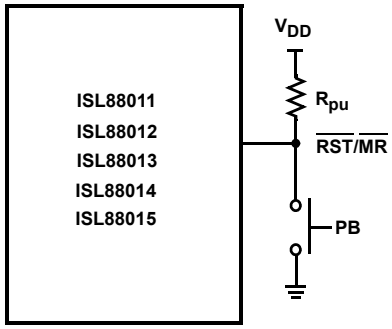



**FIGURE 4. CONNECTING A MANUAL RESET PUSH-BUTTON**

### Watchdog Timer

The Watchdog Timer circuit checks microprocessor activity by monitoring the WDI input pin. The microprocessor must periodically toggle the WDI pin within $t_{WDT}$ (1.6sec nominal), otherwise the reset signal is asserted (see Figure 5). Internally, the 1.6sec timer is cleared by either a reset or by toggling the WDI input.

Besides the 1.6sec default timeout during normal operation, these devices also have a longer 51sec timeout for startup. During this time, a reset cannot be asserted due to the WDI not being toggled. The longer delay at power-on allows an operating system to boot, an FPGA to initialize, or the system software to initialize without the burden of dealing with the Watchdog.

### Symbol Table

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

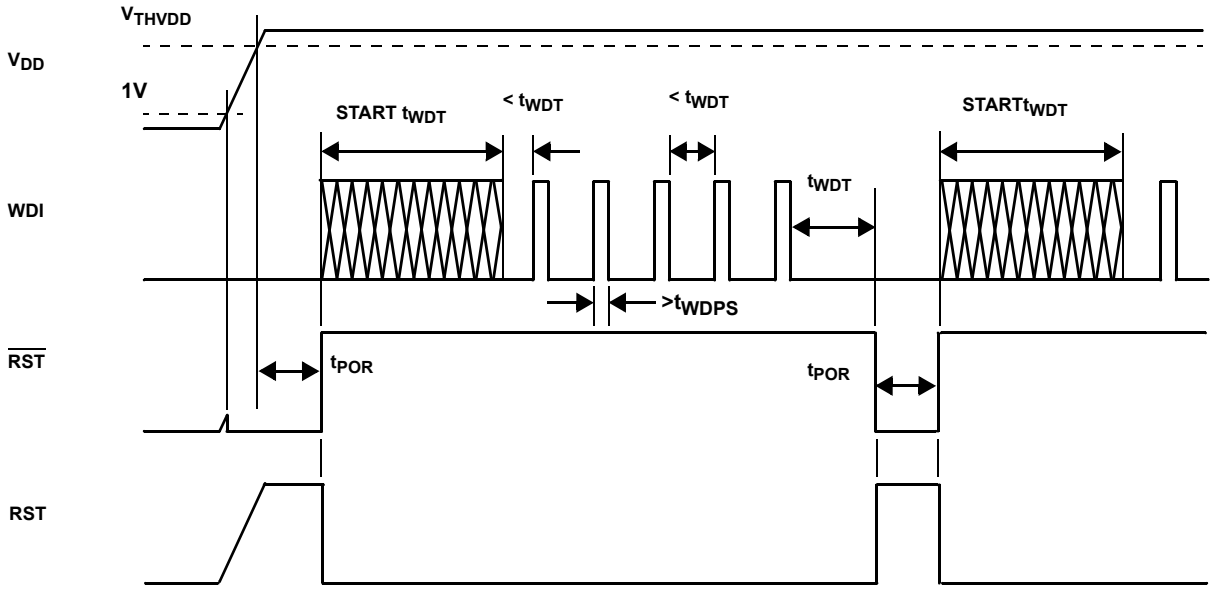



FIGURE 5. WATCHDOG TIMING DIAGRAM

## Typical Application Circuits

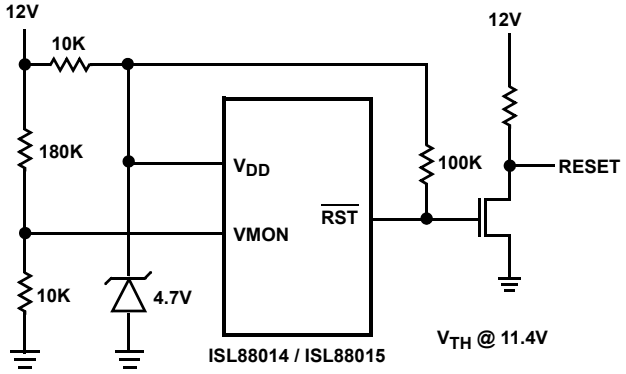



FIGURE 6. HIGH ACCURACY 12V SUPPLY MONITOR

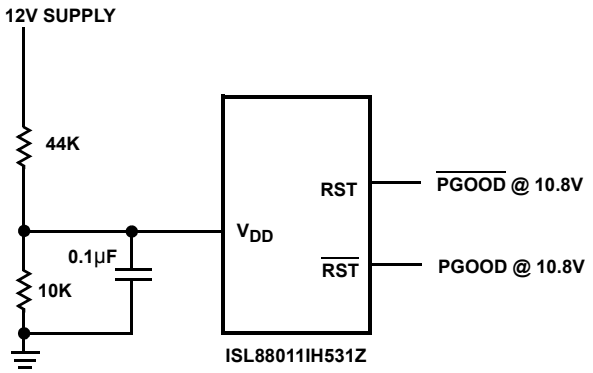



FIGURE 7. 12V SUPPLY PGOOD or $\overline{PGOOD}$

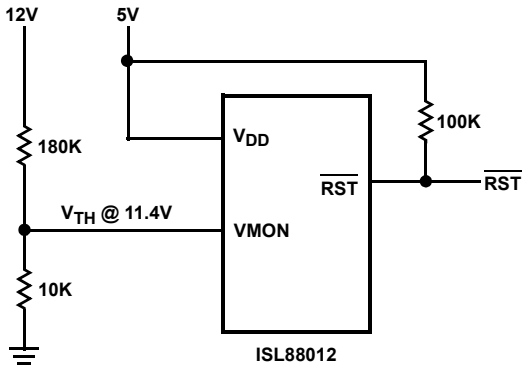
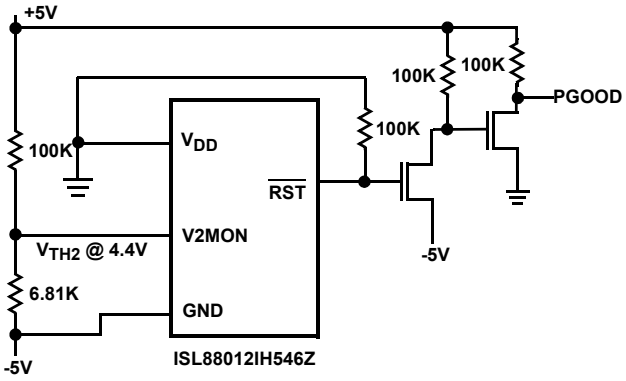


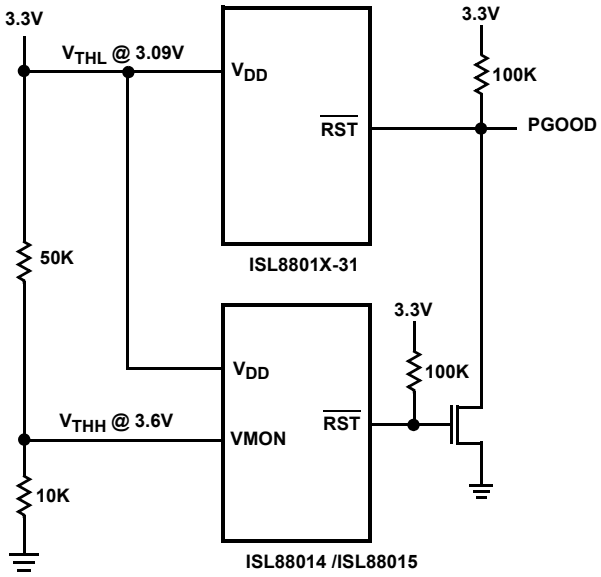

FIGURE 8. MONITOR 5V AND 12V SUPPLIES




PGOOD = HIGH IF -V < -4.6V AND -V + +V > 9.4 (abs)

FIGURE 9. +5V AND -5V MONITOR

## Typical Application Circuits (Continued)




VOLTAGE OUT OF RANGE = PGOOD LOW

FIGURE 10. OVER/UNDERVOLTAGE MONITOR

## Applications: Using the ISL8801XEVAL1 Platform

The ISL8801XEVAL1 board is designed to provide both immediate functional assessment and flexibility to the user when evaluating any of the ISL88011 - ISL88015 variants (illustrated in Figure 11). It consists of two identical banks which each contain the five different pinouts available in this product family.

The top bank comes populated for immediate assessment of functionality and performance. It is populated on the top row with the $V_{THVDD}$ = 4.38V variants of the ISL88011, ISL88012 and ISL88013. The bottom row is populated with the ISL88014 and ISL88015, which monitor positive voltages >0.6V on the VMON input pin.

The bottom bank is left unpopulated to allow other part options of the ISL88011, ISL88012 and ISL88013 to be evaluated with a minimal number of passive components to add. The $\overline{RST}$/$\overline{MR}$ pull-up resistors are included as well as the ISL88014 and ISL88015 since these ICs have no voltage variants.

During power-up, the ISL88011 - ISL88015 supervisors will assert reset once $V_{DD}$ reaches at least 1V. Thereafter, the ISL88011, ISL88012 and ISL88013 will release the reset once the $V_{DD}$ supply stays above 4.38V for the nominal $t_{POR}$ period. The ISL88012, ISL88014 and ISL88015's VMON input pins are biased to trip at 10.7V, 1.93V and 1.2V respectively. Note that because the ISL88012 is a dual voltage supervisor, both of the respective minimum thresholds for the $V_{DD}$ and VMON inputs must be met before reset is released.

All of the parts have the TwinPin™ $\overline{RST}$/$\overline{MR}$, which combines the active-low reset output with a manual reset input. The push-button can be tested by simply driving this to <100mV above ground for at least 1µs.

For the ISL88011 and ISL88014, the POR timeout delay $t_{POR}$ can be increased from the nominal 250ms by connecting a capacitor to the $C_{POR}$ pin. A comparison can be made between the two as the ISL88014 has a 22pF capacitor on its $C_{POR}$ pin while the ISL88011 $C_{POR}$ is left open.

The ISL88013 and ISL88015 have a WDI input pin, which is connects to a microprocessor or microcontroller. This input needs to be periodically toggled within 1sec to prevent the supervisor from asserting reset. The WDI test point on the ISL8801XEVAL1 board provides easy access to this input.

Multiple IC configurations as shown in Figures 6 through 10 are easy to evaluate with this platform as each bank is isolated from the other, thereby making $V_{DD}$ voltages and GND references indepedent of each other.

**SPECIAL CONSIDERATIONS:**

Using good decoupling practices will prevent transients from causing unwanted resets (i.e. due to switching noises and short duration droops in the supply voltage).

When using the $C_{POR}$ pin, avoid stray capacitance during layout as much as possible in order to minimize its effect on the $t_{POR}$ timing.

## ISL8801XEVAL1 BOM (Bill Of Materials)

R1, R2, R7, R8, R9, R10, R15, R20, R21, R22, = 100kΩ $\overline{RST}/\overline{MR}$ Pull-up Resistors

R11, R12 =10kΩ ISL88015 VMON divider to monitor 1.2V

R4 = 10kΩ ISL88014 VMON divider lower R to monitor 1.93V

R3 = 22kΩ ISL88014 VMON divider upper R to monitor 1.93V

R17 = 10.0kΩ ISL88012 VMON divider lower R to monitor 10.7V

R18 = 169kΩ ISL88012 VMON divider upper R to monitor 10.7V

C1, C2 = 1000nF Bias supply decoupling

C3 = DNP CPOR open on ISL88011

C5 = 22pF CPOR cap on ISL88014

U1-U3 = ISL8801XIH544 (Variant noted on bd)

U6-U8 = DNP (left open for any variant to be populated)

U4, U9 = ISL88014

U5, U10 = ISL88015

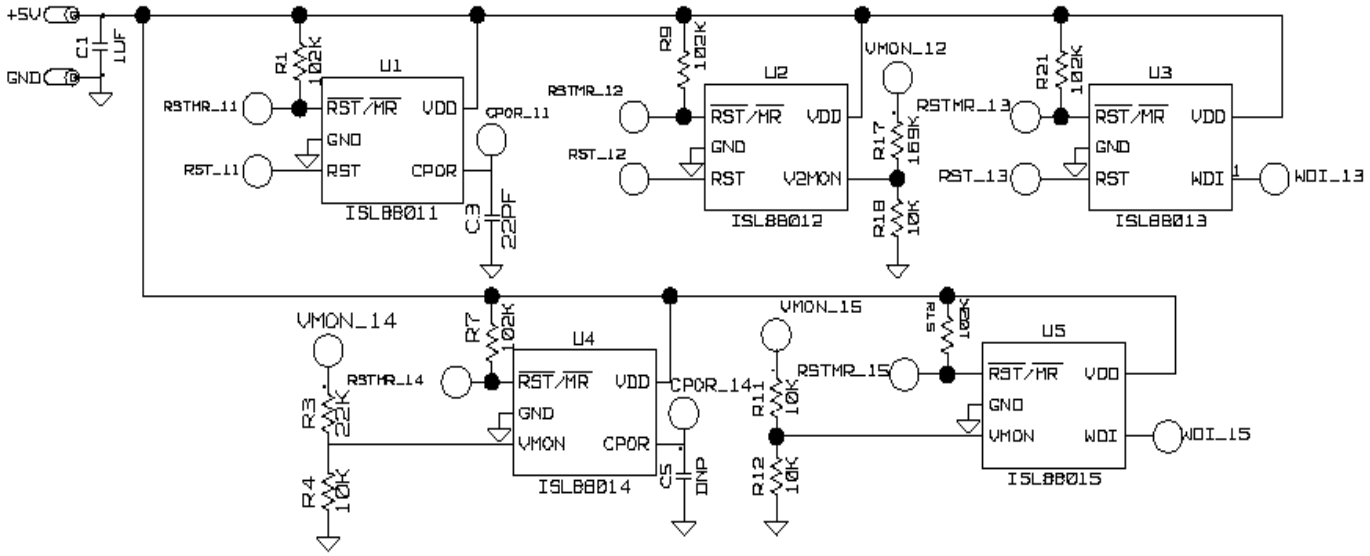
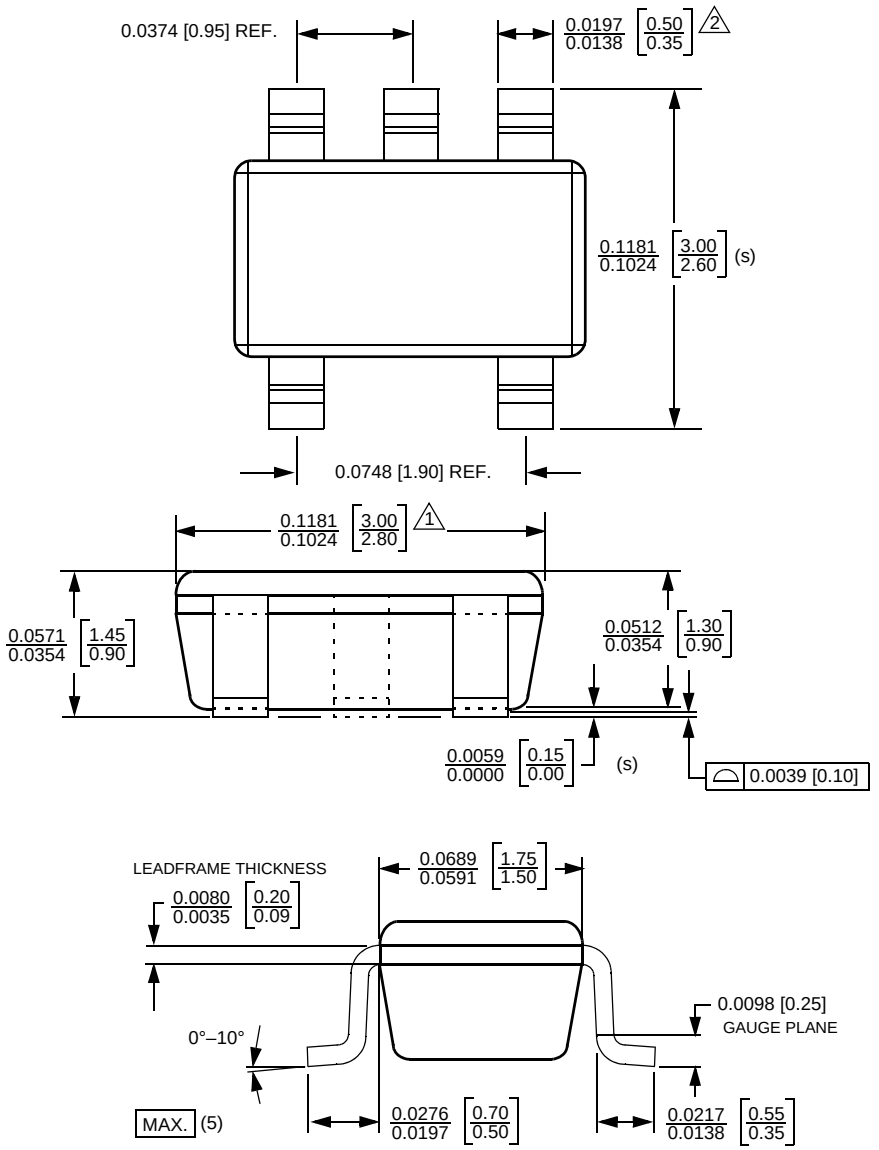



**FIGURE 11. ISL8801XEVAL1 SCHEMATIC AND PHOTOGRAPH**

## Packaging Information

**5-Lead SOT23 Package**




1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.127 MM PER SIDE.
2. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.127 MM PER SIDE.
3. DIE IS FACING UP FOR MOLD. DIE IS FACING DOWN FOR TRIM/FORM.
4. THIS PART IS COMPLIANT WITH EIAJ SPECIFICATION SC74A.
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
6. CONTROLLING DIMENSIONS IN INCHES. [mm]

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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality