TPS92518-Q1 Automotive Dual Channel Buck LED Controller with SPI Interface, Analog and PWM Dimming

1 Features

- AEC-Q100 Qualified for Automotive Applications
  - Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM Classification Level H2
  - Device CDM Classification Level C5
- Wide Input Voltage Range 6.5 V to 65 V
- Two independent Buck LED Controllers
  - High Bandwidth, Quasi-Hysteretic Control
  - Adjustable High-Side Sense
  - Direct PWM Dimming Input
  - Cycle-by-Cycle Current Limit
- SPI Communications Interface
  - Software configurable Set Points (8-bit)
  - Digital Calibration and Binning
  - Fault Monitoring and Reporting
- Advanced, High Precision Dimming
  - 10,000:1 PWM Dimming Range
  - 255:1 Analog Dimming Range
  - High Frequency Shunt FET Dimming

2 Applications

- Automotive LED Lighting: High and Low Beam, DRL, Turn, Position
- Constant Current LED Driver
- Switched Matrix Headlamps
- AFS Headlamps
- LED General Lighting

3 Description

The TPS92518-Q1 family of parts are dual channel buck LED current controllers with a SPI communications interface. The serial communication interface provides a singular communication path for multichannel and platform lighting driver module (LDM) applications.

The TPS92518-Q1 uses a quasi-hysteretic control method that supports switching frequencies ranging from 1 kHz to 2 MHz. This control method enables superior, high frequency shunt FET dimming and also handles the demanding dynamic loads of adaptive LED matrix based headlamp systems.

Software programmable SPI set points (Precision Peak Current, Controlled Off-Time and Output Voltage Sense) enables designers to develop a single LED driver solution for multiple load configurations that can be quickly reconfigured for future LED driver design requirements.

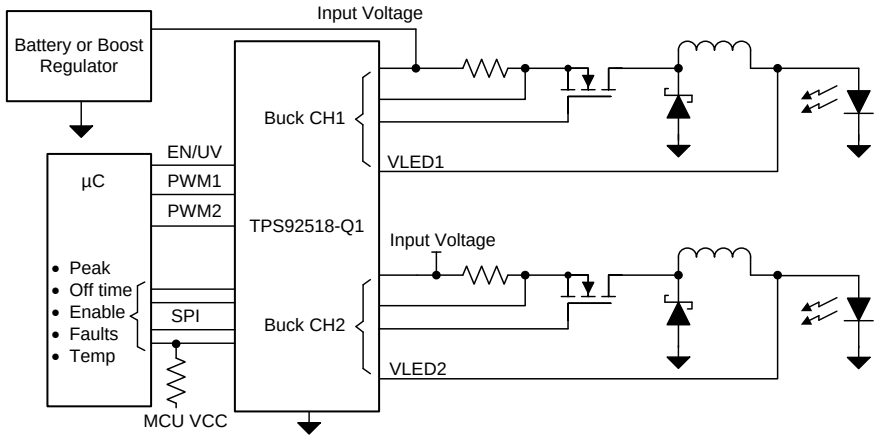
The TPS92518-Q1 device has an input range up to 42 V. The TPS92518HV-Q1 is a high-voltage option with an input range up to 65 V.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92518-Q1	HTSSOP (24)	7.7 mm x 4.4 mm
TPS92518HV-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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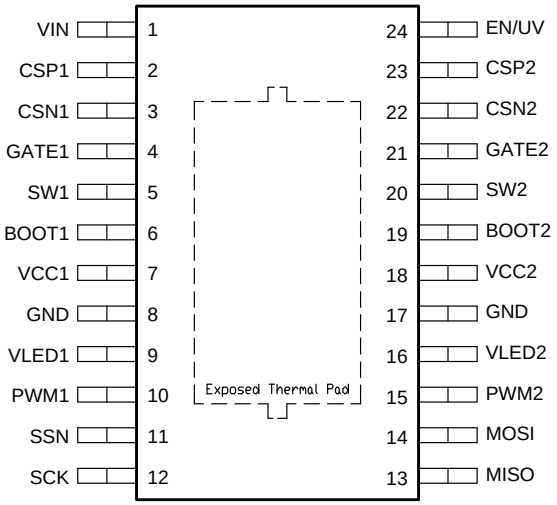
4 Revision History

DATE	REVISION	NOTES
May 2017	*	Initial release.

5 Pin Configuration and Functions

PWP Package
24-Pin HTTSOP
Top View



Pin Functions

PINS		I/O	DESCRIPTION
NAME	NO.		
BOOT1	6	I	Channel 1 bootstrap voltage input
BOOT2	19	I	Channel 2 bootstrap voltage input
CSN1	3	I	Channel 1 negative current sense input
CSN2	22	I	Channel 2 negative current sense input
CSP1	2	I	Channel 1 positive current sense input
CSP2	23	I	Channel 2 positive current sense input
EN/UV	24	I	Device enable. If not configured as under voltage lock out or enable, tie to VCCx. Tie to >23.6V to bypass SPI communication and enable default register values.
GATE1	4	O	Channel 1 gate drive output. Connect to FET gate
GATE2	21	O	Channel 2 gate drive output. Connect to FET gate
GND	8	G	System ground
	17		
MISO	13	O	SPI data output
MOSI	14	I	SPI data input
PWM1	10	I	Channel 1 PWM dimming input. Tie to VCCx if PWM pin control is not required.
PWM2	15	I	Channel 2 PWM dimming input. Tie to VCCx if PWM pin control is not required.
SCK	12	I	SPI clock input
SSN	11	I	SPI slave select input
SW1	5	I	Channel 1 switch node connection
SW2	20	I	Channel 2 switch node connection
VCC1	7	O	Channel 1 supply voltage output. May be used to power low current external circuits. See *Application and Implementation* section.
VCC2	18	O	Channel 2 supply voltage output. May be used to power low current external circuits. See *Application and Implementation* section.
VIN	1	I	Device power supply voltage input. May be common to CSP1, CSP2 or an independent supply.
VLED1	9	I	Channel 1 output voltage sense.
VLED2	16	I	Channel 2 output voltage sense.
Exposed thermal pad		G	Connect to ground. Add vias to improve thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VIN, EN/UV, CSPx, CSNx, SWx, VLEDx to GND	TPS92518HV-Q1	–0.3	67	V
	TPS92518-Q1	-0.3	44	
MOSI, MISO, SCK, SSN to GND		–0.3	5.5	
PWMx, VCCx to GND		–0.3	8.8	
GATEx, BOOTx to SWx		–0.3	8.8	
GATEx, BOOTx to GND	TPS92518HV-Q1	–0.3	75	
	TPS92518-Q1	-0.3	52	
CSPx to CSNx		–0.3	5.5	
SWx to GND, 10ns transient		–2		
Junction temperature, T_J		–40	150	°C
Storage temperature , T_{stg}		–65	165	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per V AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VIN	Input Voltage	TPS92518HV-Q1	6.5	65	V
		TPS92518-Q1	6.5	42	V
T_A	Operating ambient temperature (1)		-40	125	°C
T_J	Operating junction temperature		-40	150	°C

(1) The TPS92518-Q1 can operate at an ambient temperature of up to +125ºC as long as the junction temperature maximum of +150ºC is not exceeded.

6.4 Thermal Information

THERMAL METRIC(1)		TPS92518-Q1 PWP (HTSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{VIN} = 14 V, -40 °C ≤ T_J ≤ 150 °C, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCCx, VIN						
V_{CCx}	VCCx Voltage	V_{VIN} = 40 V or V_{VIN} = 65 V, 0 A ≤ External Load ≤ 500 µA	6.9	7.5	8.25	V
V_{CCx2}	VCCx Voltage with External Load	External Load = 500 µA	6.9	7.5	8.25	V
V_{CCx_UVLO}	VCCx undervoltage lockout	Falling threshold, V_{VIN} = 10 V	5.65	5.9	6.1	V
V_{CCx_UVHYS}	VCCx undervoltage lockout Hysteresis			0.25		V
$I_{VCCx-LIM}$	VCCx regulator current limit	V_{CC} shorted to GND.	25	38	48	mA
I_{VIN}	Operating Current	Not Switching		3	4	mA
V_{DO}	LDO drop-out voltage	I_{VCC} = 5 mA, V_{VIN} = 5 V		90	225	mV
Peak Current Comparator (CSPx, CSNx)						
V_{CSTx}	V_{CSPx}-V_{CSNx} peak current threshold	LEDx_PKTH_DAC = 255	245	255	265	mV
		LEDx_PKTH_DAC = 127	118.5	127	135.5	mV
		LEDx_PKTH_DAC = 10		10		mV
I_{CSN}	CSN input bias current			0.4	1.5	µA
t_{DEL}	CSN pin falling delay	CSNx fall to GATEx fall (1V/us stimulus)		58	110	ns
t_{LEB}	Leading edge blanking (minimum on-time)	Minimum Pulse Width	165	200	235	ns
CSP_{UVLO}	CSPx UVLO Falling Threshold		4.65	4.90	5.15	V
CSP_{UVLO-H}	CSPx UVLO Hysteresis			520		mV
Gate Drivers (GATEx, SWx and BOOTx)						
R_{DSP}	GATEx PFET ($R_{DS\ High}$)			7.3		Ω
R_{DSN}	GATEx NFET ($R_{DS\ Low}$)			2.8		Ω
$V_{BOOT-UVLO}$	Voltage where gate drive is disabled	V_{BOOT} to V_{SW} , V_{BOOT} falling	3.6	4.4	5.2	V
$V_{BOOT-UVLO-HYS}$	Hysteresis on BOOTx UVLO	V_{BOOTx} to V_{SWx}		200		mV
$I_{PD\ PWMx}$	Pull down from SWx when PWMx Low	PWMx low, (BOOTx to SWx) = 5V, V_{SWx}= 8V		200	260	µA
$I_{PD\ BOOTx}$	V_{BOOTx} -V_{SWx} < $V_{BOOT-UVLO}$	PWMx high, (BOOTx to SWx) < BOOT_UVLO, V_{SWx} = 8 V		5	7	mA
I_{BOOT_Q}	BOOTx quiescent current	(BOOTx to SWx) = 5.5 V, 0 V ≤ V_{SWx} ≤ 65 V		100	200	µA
OFF-TIMER						
t_{OFF}	Off-time	V_{LEDx} = 30 V, t_{OFFX}DAC = 255	3.2	4.1	4.8	µs
t_{D-OFF}	COFF threshold to gate rising delay	Specified by design		50		ns
$t_{OFF-MAX}$	Maximum off-time	$t_{OFF-MAX}$DAC = 255		65		µs

Electrical Characteristics (continued)

V_{VIN} = 14 V, -40 °C ≤ T_J ≤ 150 °C, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Enable and Input UVLO						
$V_{EN/UV1}$	EN/UV pin threshold	EN/UV pin rising	1.18	1.24	1.30	V
$V_{EN/UV-HYS1}$	EN/UV pin hysteresis	Difference between rising and falling threshold		100		mV
$t_{EN/UV1}$	EN/UV pin delay	EN/UV pin rising to GATEx pin rising. LEDx_MAXOFF_DAC = 0		300		ns
		EN/UV pin falling to GATEx pin falling		470		ns
$I_{EN/UV-HYST1}$	EN/UV Hysteresis Current	EN/UV = 2 V	12	16	28	µA
$V_{EN/UV2}$	EN/UV LED1_EN and LED2_EN override threshold	EN/UV pin rising writes LED1_EN and LED2_EN = 1		23.4		V
$V_{EN/UV-HYS2}$	EN/UV pin hysteresis	Difference between rising and falling threshold		3		V
$t_{EN/UV2}$	EN/UV pin delay 2	EN/UV pin rising to GATEx pin rising. LEDx_MAXOFF_DAC = 0		520		ns
PWM, MOSI, SCK, SSN						
I_{LKG}	Leakage current				1	µA
V_{IL}	Low level input voltage threshold		0.8			V
V_{IH}	High level input voltage threshold				1.8	V
t_{PWM}	PWM pin delay	PWM pin rising to GATE pin rising		68	105	ns
		PWM pin falling to GATE pin falling		55	100	ns
MISO						
V_{OL}	MISO low, I_{MISO} applied	I_{MISO} = 10 mA		0.26	0.51	V
R_{DS}	MISO Pull-down resistance	I_{MISO} = 10 mA		26		Ω
ADC						
ADC_{TEMP}	ADC Reading T = –40°C			104		Code
	ADC Reading T = 25°C			130		Code
	ADC Reading T= 150°C			171		Code
ADC_{LEDx}	ADC Reading V_{LEDx}= 60 V		226	230	240	Code
	ADC Reading V_{LEDx} = 10 V		37	38	39	Code
	ADC Reading V_{LEDx} = 1 V		2	3	4	Code
SPI Interface						
t_{SS_SU}	SSN Setup Time	Falling edge of SSN to 1st SCK rising edge	500			ns
t_{SS_H}	SSN Hold Time	Falling edge of 16th SCK to SSN rising edge	250			ns
t_{SCK}	SCK Period	Clock period	500			ns
D_{SCK}	SCK Duty Cycle	Clock duty cycle	40		60	%
t_{SU}	MOSI Setup Time	MOSI valid to rising edge SCK	250			ns
t_H	MOSI Hold Time	MOSI valid after rising edge SCK	275			ns
t_{HI_Z}	MISO Tri-State Time	Time to tri-state (deactivate low-side switch) MISO after SSN rising edge	110		320	ns
t_{MISO_HL}	MISO Valid High-to-Low	Time to place valid "0" on MISO after falling SCK edge			320	ns
t_{MISO_LH}	MISO Valid Low-to-High	Time to tri-state (deactivate the internal low-side switch) MISO after falling SCK edge. t_{RC} is the time added by the application total capacitance and resistance.			320+t_{RC}	ns
t_{ZO_HL}	MISO Drive Time High-to-Low	SSN Falling Edge to MISO Falling			320	ns
t_{SS}	SSN High Time	How long SSN must remain high between transactions	1000			ns
THERMAL SHUTDOWN						
TSD	Thermal shutdown temperature			175		°C
TSD HYST	Thermal shutdown hysteresis			10		

6.6 Typical Characteristics

V_{VIN} = 14 V unless otherwise specified. Temperature = Junction Temperature. Note: Any difference between channels does not necessarily illustrate a systematic difference between them.

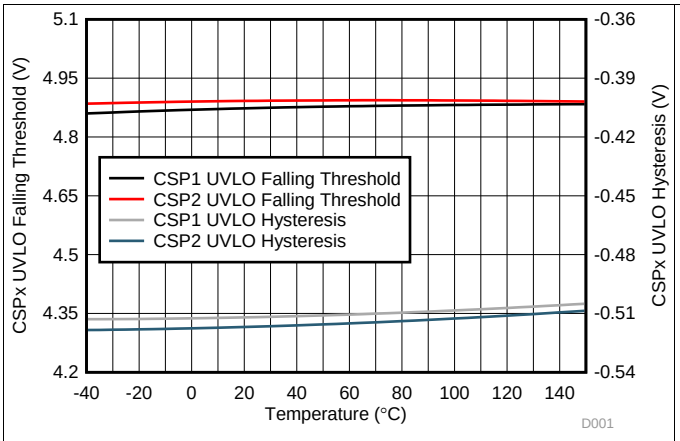


Figure 1. CSPx UVLO Falling Level and Hysteresis

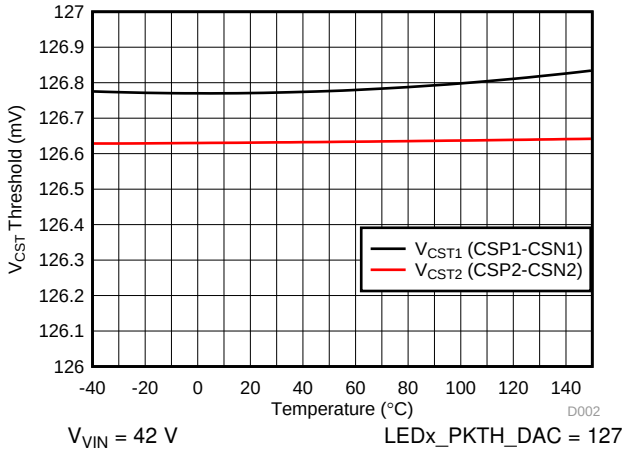


Figure 2. Current Sense Threshold Voltage

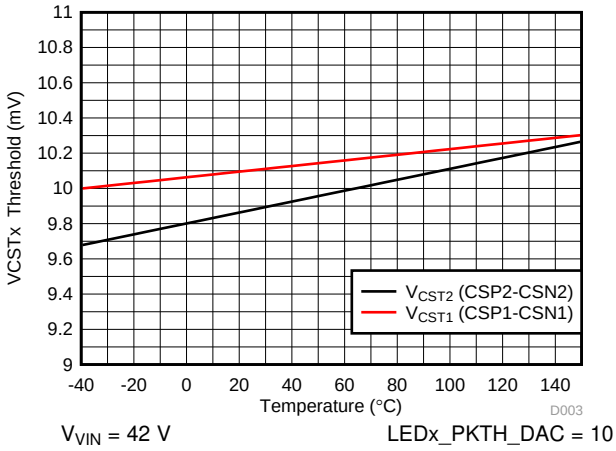


Figure 3. Current Sense Threshold Voltage

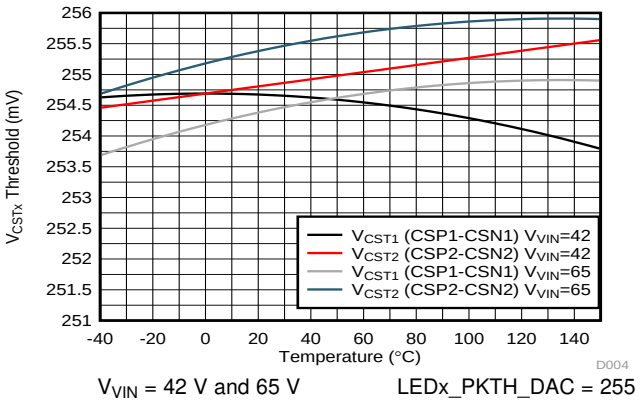


Figure 4. Current Sense Threshold Voltage

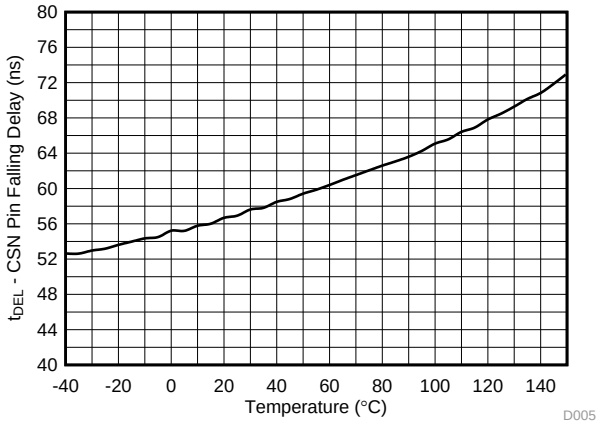


Figure 5. CSN Pin Falling Delay (t_{DEL})

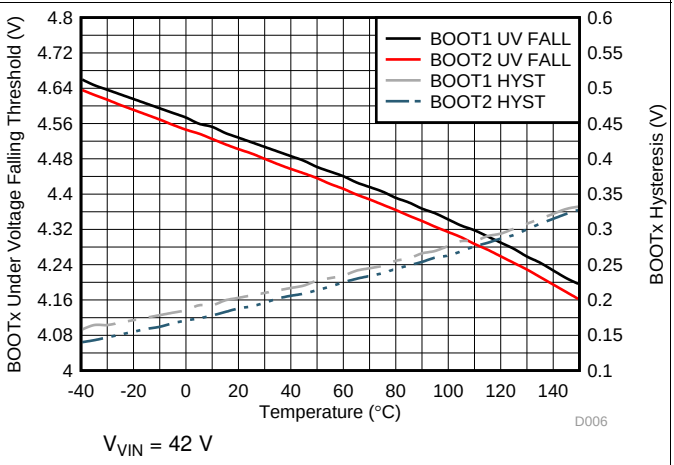


Figure 6. BOOT Undervoltage Lock-out Falling Threshold and Hysteresis

Typical Characteristics (continued)

V_{VIN} = 14 V unless otherwise specified. Temperature = Junction Temperature. Note: Any difference between channels does not necessarily illustrate a systematic difference between them.

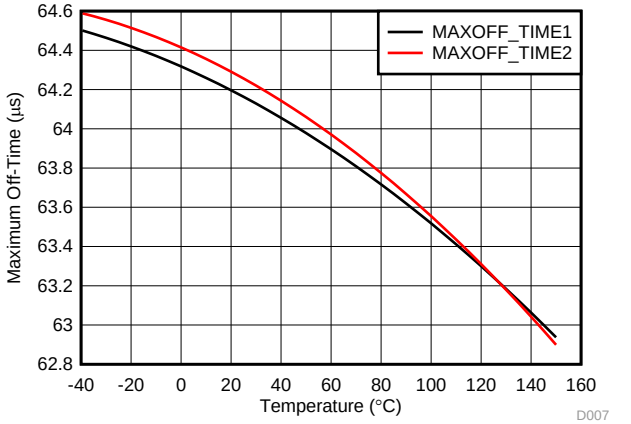


Figure 7. Maximum Off-Time

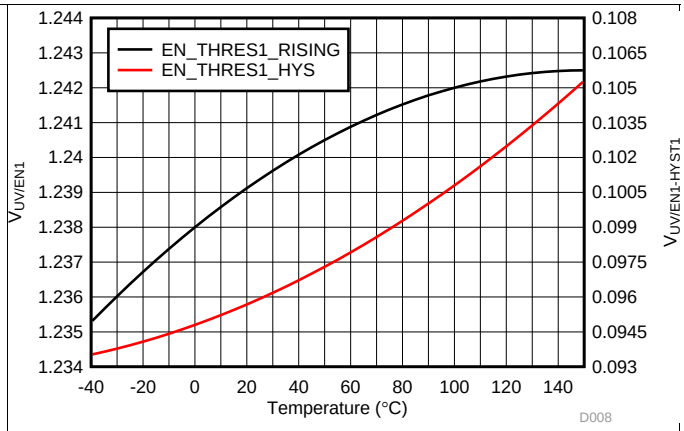


Figure 8. Enable/UV Threshold

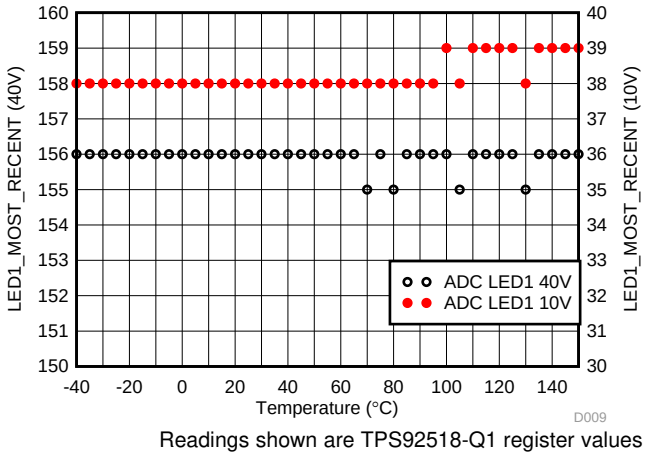


Figure 9. ADC (Analog to Digital) LED Readings

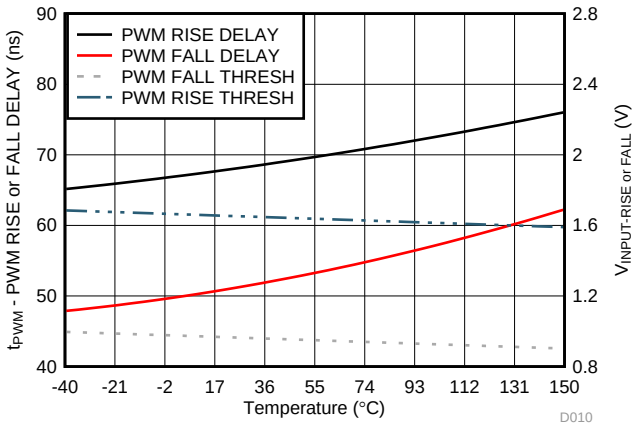


Figure 10. PWM Input Characteristics

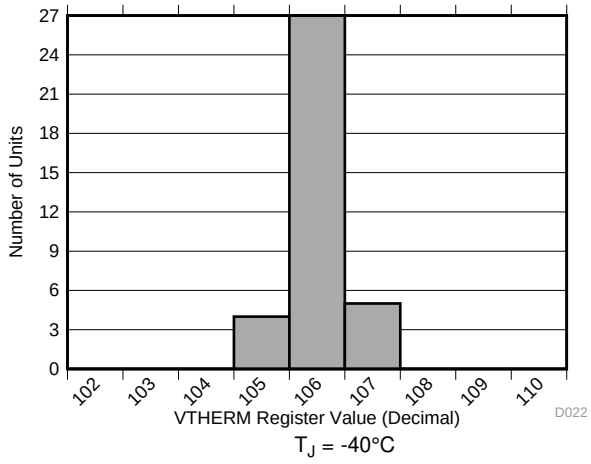


Figure 11. VTHERM Performance

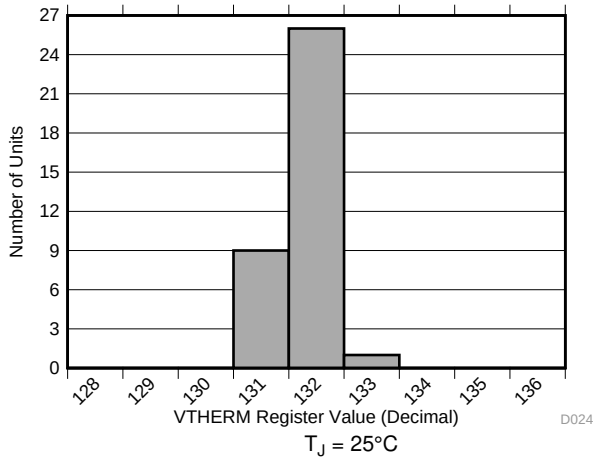


Figure 12. VTHERM Performance

Typical Characteristics (continued)

V_{VIN} = 14 V unless otherwise specified. Temperature = Junction Temperature. Note: Any difference between channels does not necessarily illustrate a systematic difference between them.

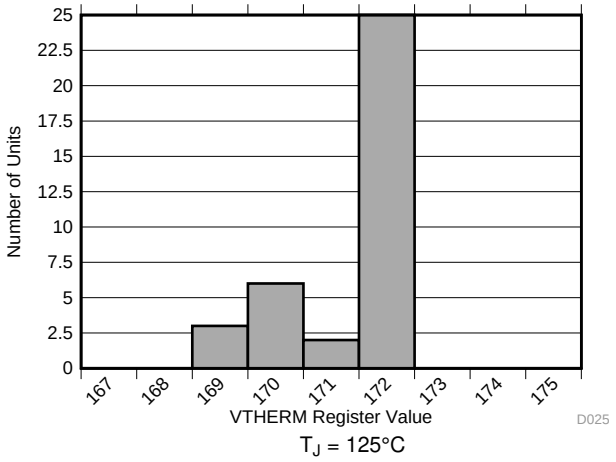


Figure 13. VTHERM Performance

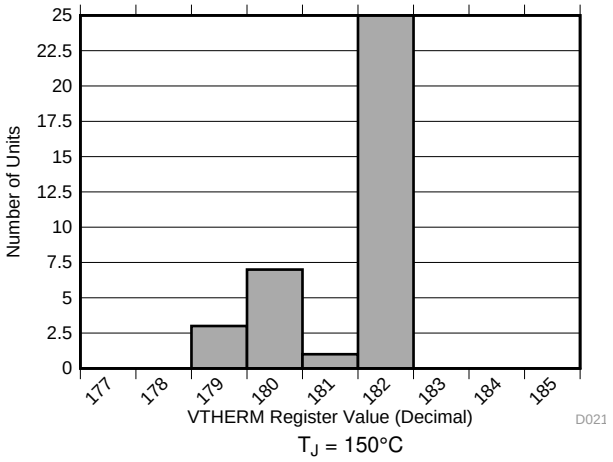


Figure 14. VTHERM Performance

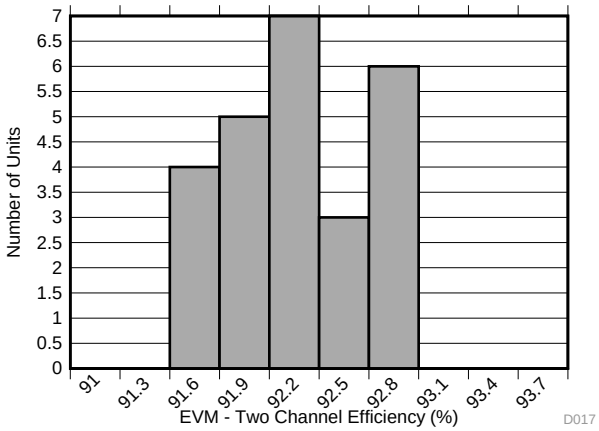


Figure 15. Efficiency Performance

7 Parameter Measurement Information

7.1 CSN Pin Falling Delay (t_{DEL})

A voltage is applied between CSP to CSN to trip the Peak Current threshold. The difference in time between the peak current activation and the Gate signal turning off is measured.

7.2 Off-Timer (t_{OFF})

A voltage is applied to the VLEDx pin. The peak current comparator is tripped and the time between the gate falling and rising is measured.

8 Detailed Description

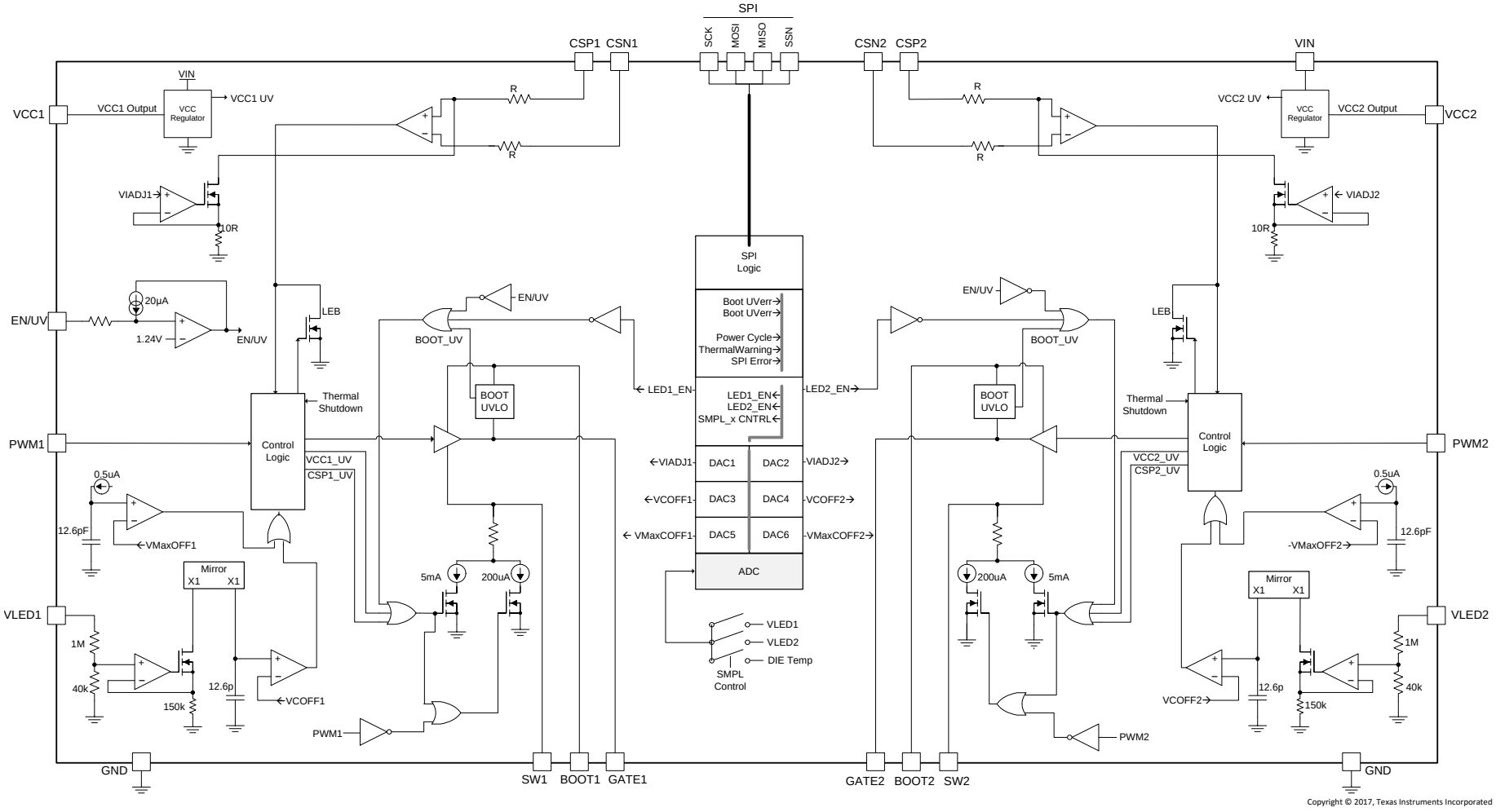
8.1 Overview

The TPS92518-Q1 is a Dual Channel Buck LED controller with SPI Interface. Quasi-hysteretic operation allows a high control bandwidth and is ideal for Shunt FET and Matrix applications (series LED switched network). Internal DACs control the high-side differential peak current sense threshold, the peak-to-peak ripple (off-time) and the maximum off-time.

The high-side differential peak current sense threshold trip voltage is set via a 10:1 divider. The divider allows a lower sense voltage for improved efficiency while still allowing a practical control voltage. The device uses a controlled off-time (COFT) architecture to allow the converter to operate in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) with no external control loop compensation, and provides an inherent cycle-by-cycle current limit because of the peak current detection each cycle. Once an off-time (us·V) target is digitally programmed, analog circuitry adjusts the off-time to maintain a constant peak-to-peak ripple. Since the peak and ripple are fixed, regulation is maintained. The programmable off-time also controls the switching frequency target.

The digitally controlled analog peak current sense threshold allows analog dimming of the LED current over the full output range. The PWM dimming input allows for high-frequency PWM dimming control requiring no external components. An internal configurable maximum off-timer allows for easy implementation of external shunt FET dimming. Refer to *shunt FET dimming information*.This simple regulator contains all the features necessary to implement a high-efficiency, versatile, digitally controlled, high-performance LED driver.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 General Operation

The TPS92518-Q1 operates using a peak-current, constant off-time control as described in Figure 16. Two states dictate the high-side FET control. The switch turns on and stays on until the programmed peak current is reached. The peak current is controlled by monitoring the voltage across the sense resistor. When the voltage drop is higher than the programmed threshold, the peak current is reached. The switch is then turned OFF, which initiates an off-time period. An internal capacitor is then charged by a current source which varies in relation to the VLEDx pin voltage. When the capacitor voltage reaches the DAC controlled threshold, the off-time ends. The off-time capacitor resets and the main switch turns ON, starting the next ON cycle.

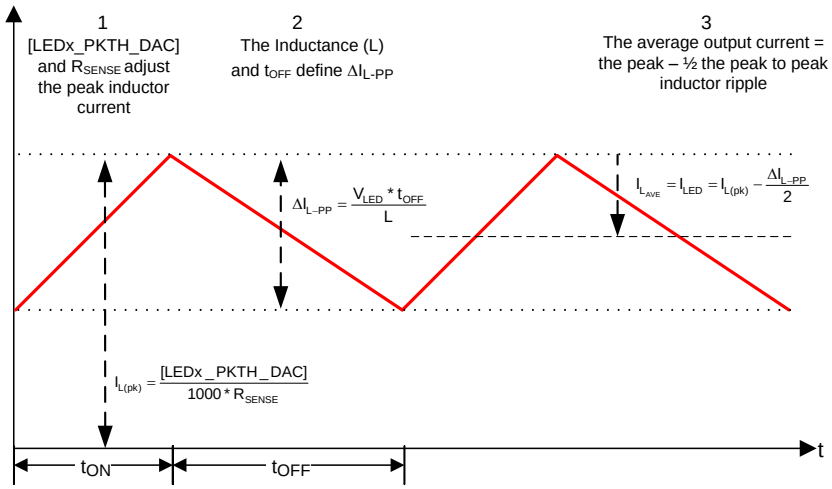


Figure 16. Hysteretic Operation

8.3.1.1 Constant Off-Time vs. Constant µs×V operation

Although commonly referred to as *constant off-time*, the off-time does vary with the output voltage in the standard TPS92518-Q1 configuration. This relation ensures constant peak-to-peak inductor current ripple (ΔI_{L-PP}). Although not common, the VLEDx pin can be set to a fixed value to generate a truly constant off-time and limit changes in frequency, however current regulation degrades. To maintain regulation and a constant ripple over various output voltages, the converter off-time must become shorter or longer as VLEDx pin voltage changes. This results in a change in frequency. In this regard, the off-time register can be considered as a seconds-times-volts setting (s × V) for the converter. The TPS92518-Q1 *Electrical Characteristics* table specification for off-time specifies a certain off time duration for a certain register value. The time is also dependent on the VLEDx pin voltage. For example, the off-time is specified at 4 µs for a V_{VLEDx}= 30 V and LEDx_TOFF_DAC = 255. The internal analog circuitry operates to keep the ripple and µs·V (micro-second volt) product constant. If the LEDx voltage changes to 15 V, the off time adjusts to 8 µs. If the LEDx voltage changes to 60 V the off time adjusts to 2 µs, and so on.

Two general cases can be examined: If the input voltage and output voltage are relatively constant, the frequency also remains constant. If either the input voltage or the output voltage changes, the frequency changes. For a fixed input voltage, the device operates at the maximum frequency at 50% duty cycle and the frequency reduces as the duty cycle becomes shorter or longer. A graphical representation is shown in Figure 17.

For a fixed output voltage (V_{VLEDx}), the off-time stays fixed. The frequency then increases as the duty cycle becomes smaller with an increasing VIN voltage. This relation is shown in Figure 18.

Feature Description (continued)

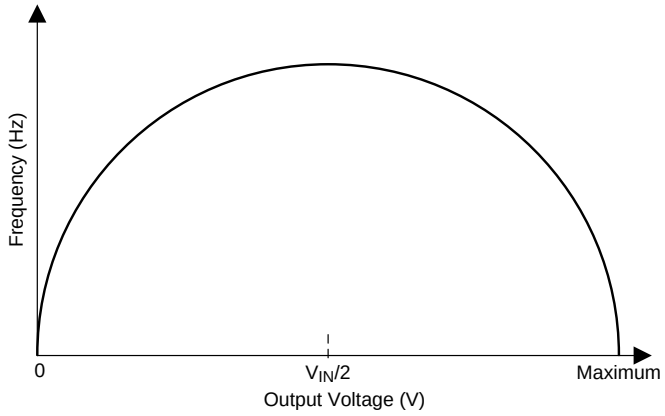


Figure 17. Frequency vs. LED Output Voltage. Fixed Input Voltage

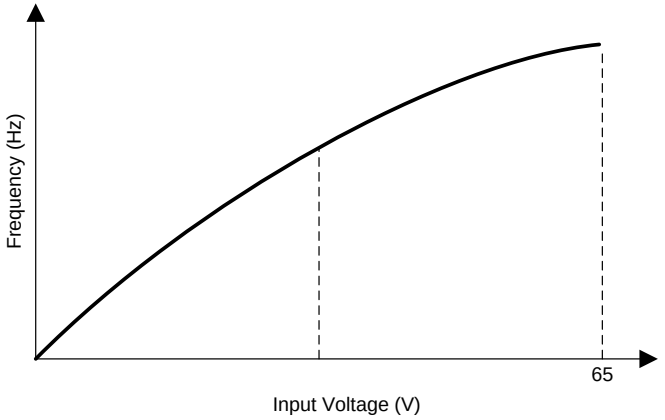


Figure 18. Frequency vs. Input Voltage. Fixed LED Voltage

8.3.1.2 Output Equation

By maintaining the off-time proportional to the output voltage (constant µs·V), it is possible to illustrate how the LED voltage (VLEDx) can be removed from the output current equation.

Starting with the inductor ripple derived from:

$$V = L\frac{di}{dt} \tag{1}$$

and the equation for the off-time:

$$t_{OFF} = \frac{LEDx\_TOFF\_DAC[7:0]}{2.136\times10^{6}\times VLEDx} \tag{2}$$

the VLEDx term is then eliminated and the peak-to-peak inductor current ripple is defined by:

$$\Delta I_{L-PP} = \frac{Vdt}{L} = \frac{VLEDx \times t_{OFF}}{L} = \frac{VLEDx \times \frac{LEDx\_TOFF\_DAC[7:0]}{2.136\times10^{6}\times VLEDx}}{L} = \frac{LEDx\_TOFF\_DAC[7:0]}{L\times2.136\times10^{6}} \tag{3}$$

The final equation for the average LED current is then:

$$I_{LED} = \left[\frac{LEDx\_PKTH\_DAC[7:0]}{1000\times R_{SENSE}}\right] - \left[\frac{LEDx\_TOFF\_DAC[7:0]}{2\times L\times2.136\times10^{6}}\right] \tag{4}$$

Because the control method relies on thresholds to control the main switch, offsets and delays must also be considered when examining the output accuracy. The I_{LED} equation can be expanded to include these error sources as shown in Equation 5. I_{LED} equations include several passive components, so it is important to consider the tolerance of each component. In this case the components are the main inductor and the sense resistor. The $V_{CSTx\text{-}OFFSET}$ parameter is the variation in the V_{CSTx} threshold between the typical and maximum or minimum values as defined in the Electrical Characteristics. The peak current threshold delay (t_{DEL}) and off timer trip point delay ($t_{D\text{-}OFF}$) specifications are also shown in the Electrical Characteristics.

$$I_{LED} = \left(\frac{\left[\frac{LEDx\_PKTH\_DAC[7:0]}{1000} \pm V_{CSTx-OFFSET}\right]}{R_{SENSE}} \pm \frac{(V_{IN} - VLEDx)\times t_{DEL}}{L}\right) - \left(\frac{\left[\left[\frac{LEDx\_TOFF\_DAC[7:0]}{2.136\times10^{6}\times VLEDx}\right] \pm t_{D-OFF}\right]\times VLEDx}{2\times L}\right) \tag{5}$$

Feature Description (continued)

8.3.1.3 OFF Timer

The converter Off-time is controlled via the LEDx_TOFF_DAC[7:0] register and VLEDx pin. The VLEDx pin voltage is converted to a current that charges an internal capacitor to a voltage set by the LEDx_TOFF_DAC creating a delay. Details of this circuit are shown in the Functional Block Diagram. Deriving the off-time from the output voltage creates a ramp representing the inductor current.

When the TPS92518-Q1 is first enabled (All UVLO levels are cleared) both timer capacitor pull-downs are disabled allowing voltage to increase on the internal timer capacitors. When either capacitor reaches the matching DAC control voltage, the high-side FET is turned on, starting a switching cycle. The maximum off-time timer is always dominant at start-up when the output is completely discharged or when shunt FET dimming and the shunt FET shunts the output for the required period.

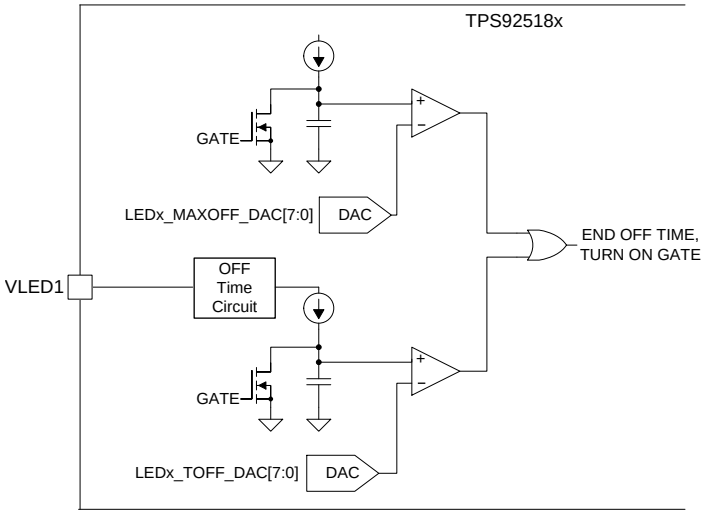


Figure 19. TPS92518-Q1 Simplified Internal Off-Timers Detail

8.3.1.3.1 Off-time and Maximum Off-time Calculations

Circuitry in the TPS92518-Q1 adjusts the off-time to ensure a constant peak-to-peak ripple. The off-time follows the relationship defined by Equation 6

$$t_{OFF} = \frac{LEDx\_TOFF\_DAC[7:0]}{2.136 \times 10^{6} \times VLEDx} \quad (6)$$

Or

$$t_{OFF} \times VLEDx = \frac{LEDx\_TOFF\_DAC[7:0]}{2.136 \times 10^{6}} \quad (7)$$

The maximum off-time circuit operates from its own independent current source that is not related to the VLEDx pin voltage. The equation for the maximum off-time is defined by Equation 8

$$\text{Maximum Off-time (s)} = LEDx\_MAXOFF\_DAC[7:0] \times \left(251 \times 10^{-9}\right) \quad (8)$$

8.3.2 Important System Considerations: Off-Timer and Maximum Peak Threshold Values

To allow full application flexibility, controls have not been implemented to limit values written to any SPI register. The system firmware must ensure control of all register values, but these two in particular must have safeguards in place.

Two potential application architectures that may allow a register modification after system engineering is complete are:

- A system has been engineered to allow firmware updates at a later time creating a situation where the Peak Current Threshold [LEDx_PKTH_DAC] value may be modified. The system LEDs can not support any higher

Feature Description (continued)

than the designed current.

- A system has been engineered to allow fine tuning of the register values during a calibration step in manufacturing.

Section *Peak Current Sense Comparator* and *Off-Time Thresholds - LEDx_TOFF_DAC and LEDx_MAXOFF_DAC* discuss a few of many system approaches to ensure values remain correct.

8.3.2.1 Peak Current Sense Comparator

A comparator, two resistors and a current source create a peak current detection circuit block. See the *Functional Block Diagram* for details. A current source controlled by LEDx _PKTH_DAC[7:0] draws a current across a resistor in series with the comparator, forcing a proportional offset. The resistor in the current source (10 R) and in series with the comparator (R) are sized with a 10:1 ratio. This ratio allows for a practical voltage range of operation for the IADJ pin and maintains a small current sense voltage for low losses and less impact on efficiency. The ON cycle begins with the offset in place via IADJ across the resistor R at the VIN pin. When the current rises enough to create a voltage across the sense resistor to match the offset, the comparator trips. The end of the on-time period starts an off-time cycle.

Trace resistance can have an impact on accuracy, so care must be used when routing the traces to CSPx and CSNx from the sense resistor. Because the sense resistor value is typically in milli-ohms, use a short kelvin connection if possible.

8.3.2.2 Peak Current Threshold - LEDx _PKTH_DAC

- Always use a current sense resistor sized so the full scale current occurs at or close to the maximum value of 255. This is also a good practice for accuracy.
- Impose a limit in firmware. Monitor the LEDxPKTH_DAC variable before each write and ensure a maximum value is maintained.

8.3.2.3 Off-Time Thresholds - LEDx_TOFF_DAC and LEDx_MAXOFF_DAC

- Do not write '0' to the LEDx_TOFF_DAC or LEDx_MAXOFF_DAC registers. Writing a '0' to the LEDx_TOFF_DAC or LEDx_MAXOFF_DAC registers is the equivalent to: *do not turn the FET off*. Damage occurs to the device when a value of 0 is written to this register.
- Do not write an off-time value that causes the TPS92518-Q1 to operate beyond the maximum frequency possible for the conversion voltage ranges. For example: for a given application switching frequency and V_{IN} to V_{LED} conversion, there is a required duty cycle. If the duty cycle requirement is shorter than the TPS92518-Q1 minimum on-time (t_{LEB}) current can not regulate. If the Off-time is made sufficiently short such that the inductor current is not able to reset given the V-s reached during the leading edge blanking time, the inductor current continues to increase until the inductor is saturated and the system may be damaged. The maximum frequency can be estimated, starting with Equation 9

$$\frac{V_{LED}}{V_{IN}} = \frac{t_{ON}}{T} = t_{ON} \times f_{SW} \tag{9}$$

Then the maximum frequency can be derived using the minimum on-time (t_{LEB} leading edge blanking)

$$\frac{V_{LED-MIN}}{V_{IN-MAX}} = \frac{t_{LEB}}{T_{MIN}} = t_{LEB} \times f_{SW-MAX} \tag{10}$$

Using an example condition: V_{IN}= 65 V, V_{LED}= 6 V, t_{LEB}= 250 ns, $\Delta I_{L\text{-}PP}$= 250 mA, we can find the maximum switching frequency and an Off-time minimum value.

$$\frac{V_{LED-MIN}}{V_{IN-MAX}} = \frac{6\,V}{65\,V} = 250\,ns \times f_{SW-MAX} \quad \text{then} \quad f_{SW-MAX} = 369\,kHz \tag{11}$$

$$t_{OFF-MIN} = \frac{\Delta I_{L-PP} \times L}{V_{LED}} = \frac{0.25 \times 100\,\mu H}{6} = 4.17\,\mu s \quad \text{then}$$

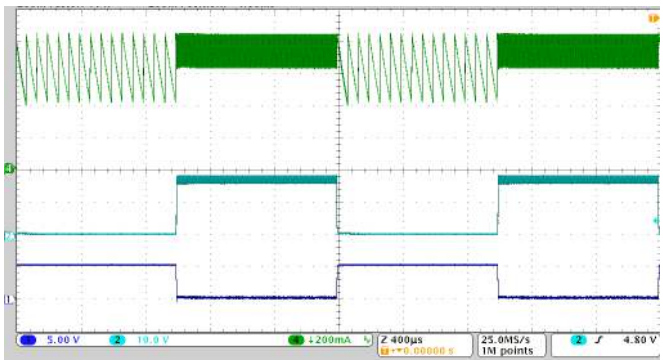
$$LEDx\_TOFF\_DAC[7:0]_{MIN} = t_{OFF-MIN} \times V_{LED} \times 2.136 \times 10^{6} = 53 \tag{12}$$

Feature Description (continued)

The system controller must be programmed with a minimum LEDx_TOFF_DAC value of 55 allowing for some margin above the computed value of 53. (a smaller value = higher switching frequency) Note this is the correct value for this example. Each application is different. All register values, minimums and maximums must be considered for each application separately.

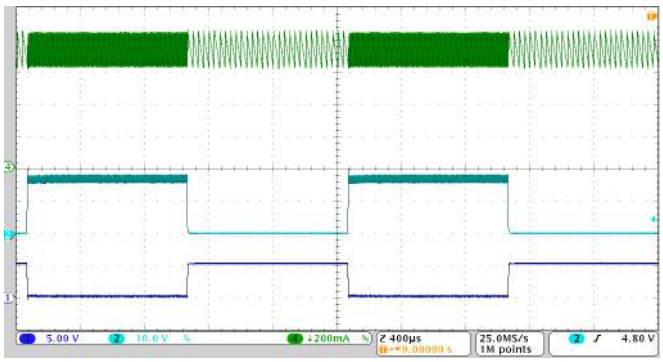
8.3.3 Shunt FET or Matrix dimming: Maximum Off-timer Calculation

Shunt FET or Matrix dimming is typically used where precise control of the LED current is required. For the LED current and light output to most accurately match the control signal, the current source supplying the LEDs must be as close to ideal as possible. With the TPS92518-Q1 hysteretic control and maximum off-time setting, the LED current can approach ideal. Two waveforms show the result during shunt FET dimming with and without optimized maximum off-time control. The result with maximum off-time control is superior and approaches an ideal current source.



CH4 (Green) : Inductor Current (200 mA per division)
CH2 (Cyan) : V_{VLEDx} (10 V per division)
CH1 (Blue) : Shunt FET Control Signal

Figure 20. Shunt FET Dimming: Non-Optimized Maximum Off-time



CH4 (Green) : Inductor Current (200 mA per division)
CH2 (Cyan) : V_{VLEDx} (10 V per division)
CH1 (Blue) : Shunt FET Control Signal

Figure 21. Shunt FET Dimming: Optimized Maximum Off-time.

To ensure the correct maximum off-time when shunt dimming it is necessary to calculate the off-time required when the output is in the shunted condition. The following procedure may be used:

1. Estimate or measure the output voltage during the shunted condition.

$$V_{SHUNT} = FET_{RDS-ON_{MAX}} \times I_{LED} \quad (13)$$

Or for the Matrix approach:

$$V_{SHUNT} = R_{ALL(on)} \times I_{LED} \quad (14)$$

2. Compute the off-time required ($t_{OFF\text{-}Shunt}$) when the output is shunted.

$$t_{OFF-Shunt} = \frac{\Delta I_{Lpk-pk} \times L}{V_{SHUNT} + (0.7)} \quad (15)$$

3. Compute the Maximum Off-time Register Value.

$$LEDx\_MAXOFF\_DAC[7:0] = \frac{\text{Maximum Off-time(s)}}{251 \times 10^{-9}} \quad (16)$$

8.3.3.1 Output Ringing and TPS92518-Q1 Protection

During shunt dimming, ringing may occur at the channel output due to PCB and device parasitic capacitances and inductances. This should be checked as part of the design process. If the ringing approaches the absolute maximum of any pin, a clamping diode must be added to the design. Connect the diode anode to the output at VLEDx and the cathode to the input voltage. This protection must also be used if the LED load is ever to be connected or removed while the output is enabled.

Feature Description (continued)

8.3.3.2 Live Peak and Off-Time Threshold Changes

All TPS92518-Q1 thresholds may be changed at any time. Once the SPI transaction completes, the change is seen in operation in ~100ns.

8.3.4 VIN and the VCC Internal Regulators

The device incorporates a linear regulator for each channel to generate the 7.5-V (typ) VCC voltage. Both VCC rails are powered from the VIN pin. VIN may be connected to the input of either channel or to a separate external supply. The VCC output voltages are internally monitored to implement undervoltage lockout (UVLO) protection for the respective channel. For example, if UVLO is reached on CH1, CH2 remains active. The VCC undervoltage lockout thresholds are fixed and cannot be adjusted.

The device has been designed to supply current for the device operation as well as additional power for external circuitry. If a 7.5-V rail is required in an application, the device can allow up to 500 μA to be drawn in addition to the device load. A capacitance of 1 μF or ≥ 10× the BOOT capacitance to a maximum of 10 μF is recommended.

The device requires adequate input decoupling in order to lower ΔV_{IN-PP} ripple for the best VCC supply voltage performance. ΔV_{IN-PP} must not exceed 10% of the input voltage or 3V, whichever is lower.

8.3.5 Output Enable Control Logic

Several safeguards and control states must be satisfied before switching can begin as shown in Figure 22. VCC, BOOT and the CSP input must not be in under voltage lock-out. The device must not be in thermal shut-down and the EN/UV pin must be high. The PWM pin for the channel must also be high. It is not possible to override the PWM pin logic via the SPI interface. If PWM dimming is not required, tie the pins to VCC.

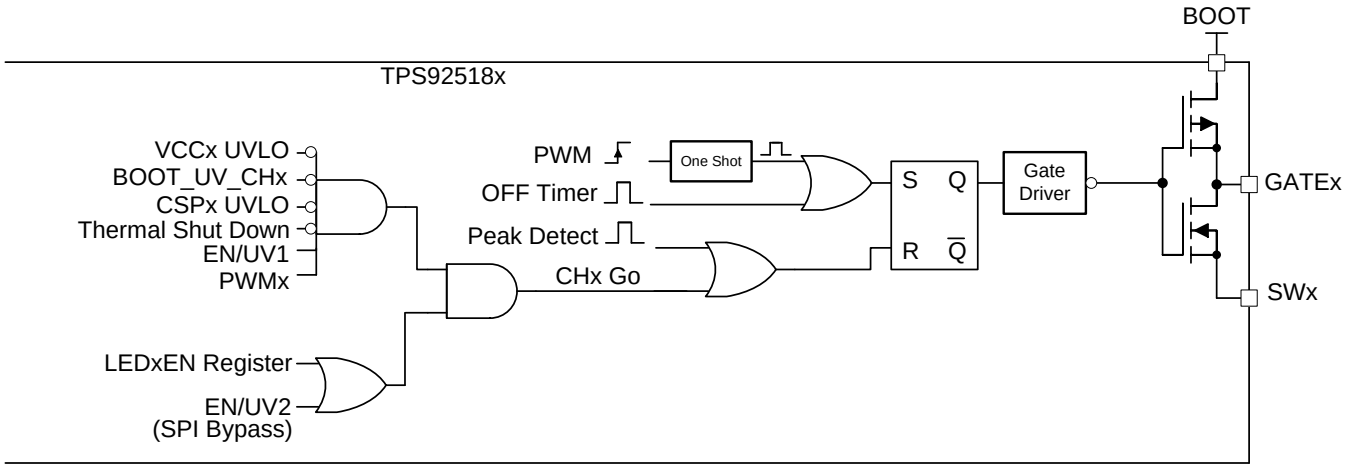


Figure 22. TPS92518-Q1 Output Enable Control

8.3.5.1 EN/UV2 - SPI Control Bypass

Note that the TPS92518-Q1 does allow a means to enable the part without SPI communication. By applying a voltage above the second threshold level, EN/UV2 (23.6 V typical), the state of the LEDxEN register is bypassed. This allows a TPS92518-Q1 to be powered and operated using the default register values (see Registers. A quick summary is that peak and off-time thresholds are set to 127 out of 255) without SPI communication. All other required operation points must still be satisfied as shown in Figure 22.

This could be useful in a manufacturing flow or during system troubleshooting. The logic path is highlighted again in Figure 23.

Feature Description (continued)

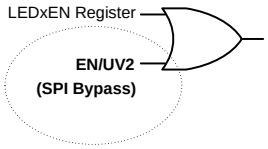


Figure 23. Output Enable Control Logic

8.3.6 BOOT Capacitor and BOOT UVLO

The BOOT capacitor provides the power for the high-side gate drive circuitry. The capacitor is charged each cycle from VCC during the off-time phase of the switching cycle. During the off-time, the free-wheeling diode conducts, pulling the switchnode (SW) low and providing a conduction path to charge the capacitor. During the on-time, the current required to charge the high-side FET gate and power the driver are supplied by the capacitor.

A minimum boot capacitor can be calculated by considering: the MOSFET Qg, the driver quiescent current, and the desired nominal maximum on-time. Other factors include: the BOOT diode Vf, the minimum BOOT operation voltage, and the level of the switchnode (SWx) during the off-time. A rough estimate can be calculated using Equation 17: or just use 0.1µF.

$$C_{BOOT} \geq \frac{Q_g + (I_Q \times T_{ON})}{V_{CC} - V_{f(bd)} - V_{BOOT-UVLO(MAX)} - V_{SW(OFF)}} \quad (17)$$

The variables are defined by:

Table 1. C_{BOOT} Variables

Variable	Description
Q_g	High-side FET total gate charge (Qg) as shown in the FET datasheet.
V_{CC}	7.5 V
$V_{SW(off)}$	The switchnode voltage when the high-side FET is off. Use 0 V.
$V_{BOOT-UVLO(MAX)}$	5.2 V
I_{BOOT-Q}	200 µA
t_{ON}	Estimate your worst case on-time or use 500 µs
$V_{f(bd)}$	Forward drop of the boot diode

A typical solution calculates a minimum C_{BOOT} of approximately 60 nF, justifying the 100 nF selection.

If conditions are created which cause the boot capacitor to become depleted (see *Drop-out Operation*) and reach $V_{BOOT-UVLO}$, switching is disabled until V_{BOOT} increases by $V_{BOOT-UVLO-HYST}$.

8.3.7 Drop-out Operation

If the input or output voltage change such that they become close to the same value, a condition known as *drop-out* is created. During drop-out conditions the output LED current may fall out of regulation. If the input reaches the target output voltage or below, the LED current can drop to zero. There are two stages of drop-out when operating with a hysteretic device like the TPS92518-Q1. The two stages are described in *Early Drop-Out (Boot Capacitor Voltage >> $V_{BOOT-UVLO}$)* and *Full Drop-Out (Boot Capacitor Voltage reaching $V_{BOOT-UVLO}$)* .

8.3.7.1 Early Drop-Out (Boot Capacitor Voltage >> $V_{BOOT-UVLO}$)

the first effects of drop-out can be seen when the input voltage approaches a few volts above the output voltage. Unless there is sufficient output capacitance, the change in the LED voltage during the ramp up of the inductor and output current can cause a non-linearity in the ramp.

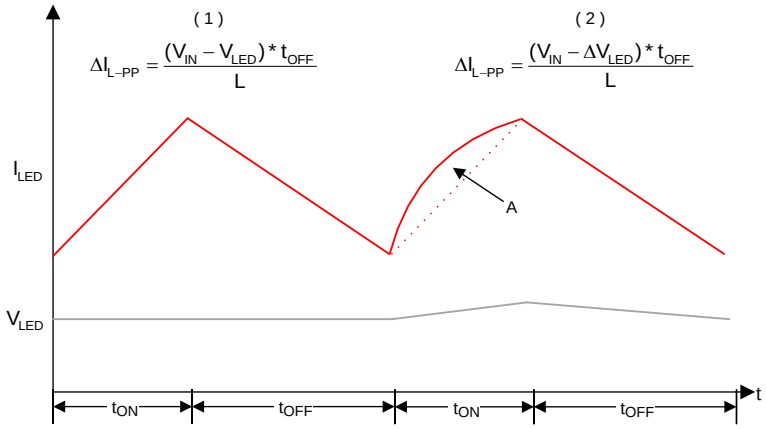


Figure 24. Inductor on-time Current Non-linearity

In case (1) shown in , V_{IN}-V_{LED} is sufficiently large that variations in V_{LED} are not relevant and/or not present because of sufficient output capacitance.

In case (2), V_{IN} and V_{LED} are closer in value making the difference lower and more easily affected by variations in V_{LED}. ΔV_{LED} is the total variation in the voltage across the inductor and includes the I_{LED} x $R_{L\text{-}DCR}$ voltage drop which also changes with I_L and impacts the inductor current linearity. The combination of factors leads to an inductor current on-time non-linearity which increases the average value of the inductor current, and hence the LED current. This means the first affect of approaching drop-out is always an increase in LED current.

It is important to note that the output current is always limited to the peak limit set by the internal programmed reference and the sense resistor. (The peak current threshold) This means a design having a smaller overall inductor current ripple (smaller $\Delta I_{L\text{-}PP}$) will have less error when a drop-out condition occurs.

8.3.7.2 Full Drop-Out (Boot Capacitor Voltage reaching $V_{BOOT\text{-}UVLO}$)

If V_{IN} and V_{LED} are sufficiently close the duty cycle demand increases. Because of the TPS92518-Q1 hysteretic control method, the high-side FET attempts to remain ON until the programmed peak current is reached. Keeping the high-side FET ON requires energy from the BOOT capacitor which depletes the BOOT capacitor voltage. If the high-side FET is ON for sufficient duration, the BOOT capacitor voltage eventually reaches $V_{BOOT\text{-}UVLO}$ level at which point the high-side FET is turned off. This allows for long on-times and duty cycles >99.5%, since the time the high-side FET can remain ON is long (>1 ms) compared to the time required the recharge the BOOT capacitor (approximately 100 ns). The typical maximum on-time can be estimated by Equation 18

$$t_{ON-MAX_{(TYP)}} = \frac{C\,dv}{i} = \frac{C_{BOOT}\ x\ (V_{CC} - V_{BOOT-UVLO})}{I_{BOOT-O}} \approx \frac{0.1\mu F\ x\ (7.5 - 4.6)}{100\mu A} \approx 2.9 ms \quad (18)$$

8.3.7.3 Minimum BOOT Voltage and FET Control

The minimum $V_{BOOT\text{-}UVLO}$ is also the minimum voltage available to drive the external FET. Check the FET Output Characteristics (I_D versus V_{DS}) at the minimum BOOT voltage and ensure the FET is sufficiently enhanced under this condition. If the turn-on is marginal, the FET may operate in the linear region causing increased losses and possibly damage the device.

8.3.7.4 BOOT Controlled internal Pull-Down

Each time $V_{BOOT} \leq V_{BOOT\text{-}UVLO}$ an internal pull-down ($I_{PD\ BOOTx}$ = 5 mA typical) from the SWx pin to ground is enabled. This behavior occurs during drop-out conditions such as *Full Drop-Out (Boot Capacitor Voltage reaching $V_{BOOT\text{-}UVLO}$)* . This behavior also occurs at Start-Up if the output is pre-charged.

If the TPS92518-Q1 application uses an output capacitor and the output is disabled and re-enabled before the output voltage reduces (or is otherwise pre-charged) a condition can be created where the SWx pin voltage is not low enough for the BOOT capacitor to charge. (V_{SWx} << V_{CC}) BOOT-UV is then activated and the internal pull-down circuitry enabled. The pull-down circuitry reduces the time required to deplete the output voltage to allow the BOOT capacitor to be charged. Note that the internal pull-down circuitry can not act as a synchronous FET.

8.3.8 Analog and PWM Dimming

8.3.8.1 Dimming Methods

The TPS92518-Q1 has been designed to support three dimming methods. Analog, PWM and Shunt-FET or Matrix (TPS92661/TPS92662 device family) dimming. Analog dimming is still accomplished via the SPI interface through adjustment of the LEDx_PKTH_DAC register. PWM dimming is accomplished by using the PWMx pin. Shunt-FET or Matrix Dimming is optimized by using the LEDx_MAXOFF_DAC register. One or more dimming methods may also be combined to obtain extreme contrast ratios. To obtain an ultra-fine adjustment, the LEDxTOFF_DAC register may be also adjusted allowing average output current modifications in the range of 100 µA per LSB.

8.3.8.2 PWMx Pin Operation

PWM dimming can be used to adjust the output brightness by changing the applied PWM duty cycle to a channels' corresponding PWM pin. Each channel can be controlled with an independent frequency and duty cycle.

When the PWM pin signal is < 0.8 V, the corresponding channel's gate logic is disabled. When PWM rises above 1.6 V the rising edge sets the gate drive latch and turns on the FET. If PWM dimming is not required, PWMx be tied to VCC.

Treat the PWM pin as a digital input. Avoid slow transitions of the pin voltage level around the logic thresholds. Ensure the signal edge rate is adequate (<100ns) when measured at the device PWMx pin to prevent false level interpretations. If the edge is too slow, a small capacitor may be required. If the PWM pin edge rate is too slow and is not adequately decoupled, the TPS92518-Q1 PWM pin logic may interpret one transition as multiple ON-OFF transitions. This can cause the output current to ratchet beyond the desired set-point and possibly cause the system to be damaged.

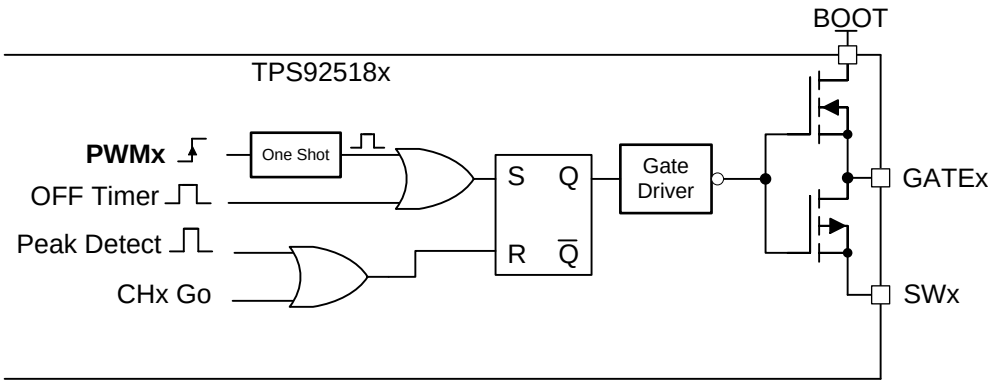


Figure 25. Gate Control Logic

8.3.8.3 PWM Dimming - Current Rise Performance

A unique feature of the TPS92518-Q1 hysteretic control allows the first switching pulse of a PWM dimming on-time to rise completely to the correct peak current in one switching cycle. An example is shown in Figure 26. When the rising edge of the PWM signal is seen by the PWMx pin the main FET is turned on. The FET remains ON until the programmed peak current threshold is reached. Once reached, switching continues until the PWMx pin voltage goes low. The TPS92518-Q1 can also operate when using pulse widths that are sufficiently narrow that the programmed peak is not reached. The on-time is terminated at the end of the PWM pulse and another on-time initiated when the PWMx pin goes high again.

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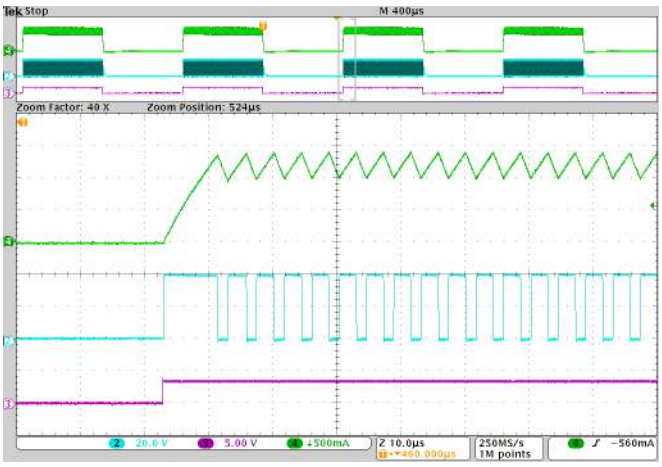
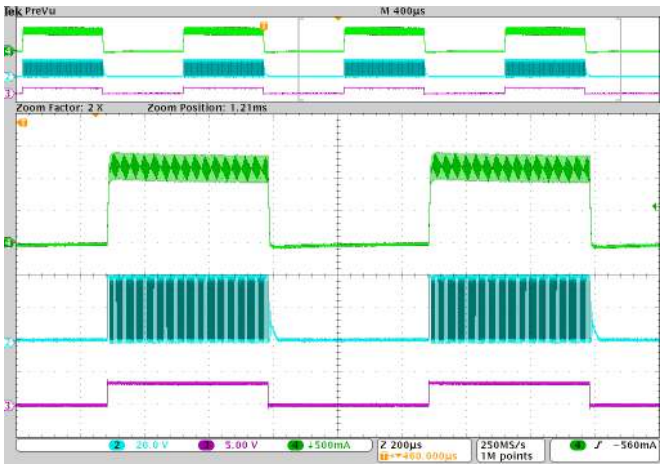


CH4: Inductor Current CH3: PWMx Pin CH2: SWNx

Figure 26. PWM Dimming, Pulse after Rising Edge



CH4: Inductor Current CH3: PWMx Pin CH2: SWNx

Figure 27. PWM Dimming, Two Periods

8.3.8.4 PWM and Analog Dimming - Linearity Limitations and Buck Converters

8.3.8.4.1 PWM:

A linearity limitation occurs at very small PWM duty cycles; the PWM dimming on-time becomes short enough that it contains only one or a few switching cycles. If the PWMx pulse falls during an off-time (see Figure 28), the pulse length is not able to change because the switch is already off. This can lead to a small 'stair-case' dimming curve in this region as the duty cycle affects the average current during on-times and then not during off-times. This situation can be improved by increasing the switching frequency. This limitation is common to all Buck converters during very small PWM dimming duty cycles.

Shunt FET PWM dimming avoids this issue as the average current is affected during switching ON and OFF times. Shunt FET PWM dimming can out-perform PWM dimming, but is more complicated to implement.

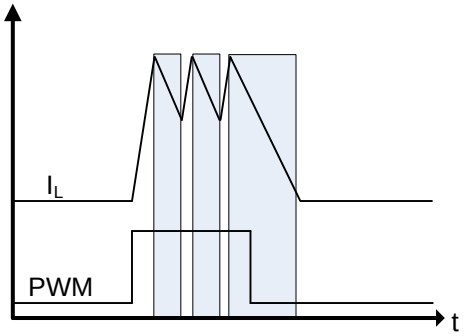


Figure 28. PWM Dimming Limitation

8.3.8.4.2 ANALOG:

Another impact on linearity can occur when analog dimming (LEDx_PKTH_DAC threshold adjustment) and the inductor current becomes discontinuous. Discontinuous conduction mode (DCM) occurs when the inductor current reaches 0 A each off-time. When the device enters DCM, the output current is no longer the peak current minus half the ripple current (as shown in Figure 16) and is no longer a linear relationship between the LEDx_PKTH_DAC value and the average output current. The linear range can be extended by lowering the ripple, $\Delta I_{L\text{-}PP}$ to extend the natural linear region of operation.

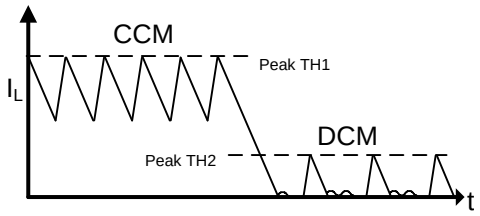


Figure 29. Analog Dimming Limitation

Another approach can be used by first analyzing the system operation. The point at which DCM is entered can be calculated as well as the average current value when in DCM. The micro-controller writing the LEDx_PKTH_DAC values can simply write alternate values in the DCM area to ensure net linear response to the LED average current. See *DCM Current Calculation* for information on calculating the average current when in DCM.

8.3.8.5 DCM Current Calculation

The converter is considered to be operating in DCM (Discontinuous conduction mode) when the peak current is less than the peak-to-peak inductor current ripple. ($I_{L(pk)} < \Delta I_{L\text{-}PP}$). Equations Equation 20 through Equation 25 define the calculation described by Equation 19. Note that the value of the LED voltage is different when operating in DCM.

Starting with the basic equation for a buck converter **in DCM**:

$$I_{LED_{DCM}} = \frac{D_1 \text{ x } T}{2 \text{ x } L} \text{ x } \left(D_1 + D_2\right) \text{ x } (V_{IN} - VLEDx) \tag{19}$$

followed by: (η is the estimated converter efficiency):

$$D_1 = \frac{1}{1 + \left[\frac{t_{OFF} \text{ x } ((V_{IN} x \eta) - VLEDx)}{L \text{ x } I_{Lx-peak}}\right]} \tag{20}$$

$$D_2 = \frac{I_{Lx-peak} \text{ x } L}{T_{DCM} \text{ x } VLEDx} \tag{21}$$

Where T defines the switching converter period.

$$T_{DCM} = t_{ON-DCM} + t_{OFF} \tag{22}$$

$$t_{ON-DCM} = \frac{I_{Lx-peak} \text{ x } L}{V_{IN} - VLEDx} \tag{23}$$

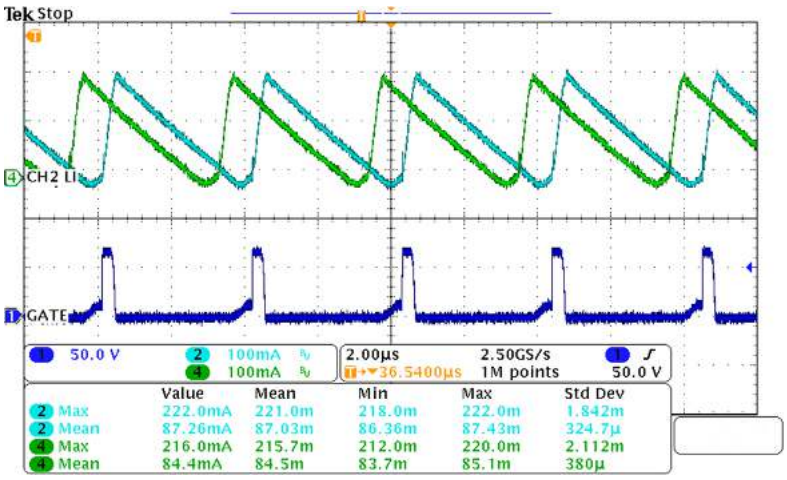
$$t_{OFF} = \frac{LEDx\_TOFF\_DAC[7:0]}{2.136 \times 10^6 \times VLEDx} \tag{24}$$

$$I_{Lx-peak} = \frac{LEDx\_PKTH\_DAC[7:0]}{1000 \times R_{SENSE}} \tag{25}$$

See Equation 4 for the CCM (continuous current mode) equation.

8.3.8.6 Current Sharing

The TPS92518-Q1 can be configured to operate as a Two Channel, Single Output converter by configuring each channel identically and connecting the outputs together. Figure 30 illustrates the current sharing capability with each channel handling approximately the equal share of the output current load. Statistics are enabled and the average inductor current of each channel is also shown. The total output current for this configuration is 438 mA. Note that both channels must be enabled at the same time to allow charging of the boot capacitors. When a channel is paralleled, it may not be enabled after the first channel is enabled.



TPS92518-Q1 Channel 1 and 2 Outputs Connected in Parallel.

CH4 (Green) : Inductor Current (100 mA per division)

CH2 (Cyan) : Inductor Current (100 mA per division)

CH1 (Blue) : SW1 Node (50 V per division)

Figure 30. TPS92518-Q1 Channels Connected to Current Share

8.3.9 VIN and CSPx Pin Configuration

The TPS92518-Q1 has been designed to support single or dual input voltage sources. The VIN pin connection is also flexible and may be connected to the input supply of either channel or from a third independent channel.

The Electrical Characteristics table defines CSP_{UVLO} as the minimum voltage required by a channel to continue operating. This limit is set regardless of the VIN and VCCx voltages. The VIN pin does not have an under voltage lock-out level, but must support the VCCx voltage for the channel. The minimum VIN pin voltage is limited to 6.5 V because two items depend on the voltage level for operation that have their own UVLO (under voltage lock-out) levels: VCCx and BOOTx. The 6.5-V level is derived from the maximum V_{CCx_UVLO} level with some added margin. Alternately the maximum $V_{BOOT-UVLO}$ level may be used. If we consider this level and add the drop of the boot diode, we obtain the same value and with some margin obtain the same VIN pin minimum level of 6.5 V.

8.3.10 Enable and Undervoltage Lock-out Configuration

If drop-out operation is not desired, configure a resistor divider to disable switching of both channels at the desired input voltage.

The value of resistors R2 and R3 establish the undervoltage lockout level as shown in Figure 31. Include a small level of capacitance (approximately 0.1 µF) at the UVLO pin for noise immunity. If the application does not require drop-out operation (operation when V_{VIN} approximates V_{VLEDx}) program a UVLO level that allows no switching to occur until there is adequate input voltage available.

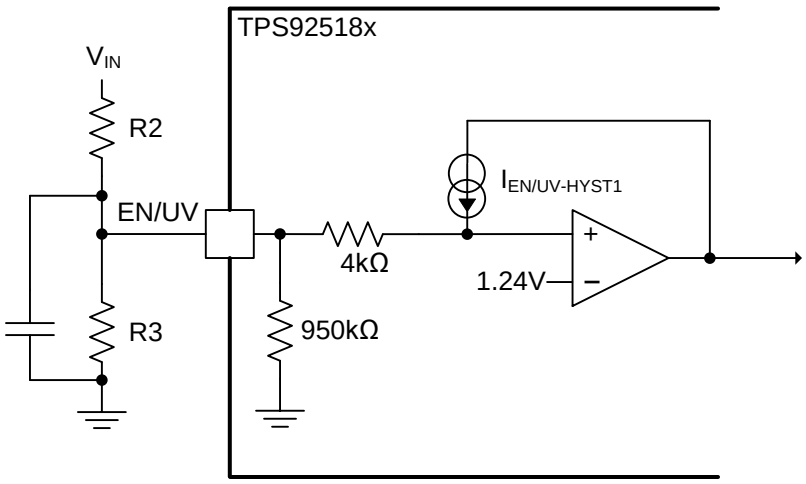


Figure 31. EN/UV Programming Resistors

Select the desired amount of voltage hysteresis and the desired turn-ON threshold ($V_{IN\text{-}RISE\_THRESHOLD}$). Because of the small amount of fixed-voltage hysteresis and fixed-hysteresis current, some combinations of turn-ON and turn-OFF thresholds are not possible. If the calculation results in values that are zero or negative, the combinations selected are not possible. After selecting a turn-ON point and desired amount of voltage hysteresis (V_{HYST}) use Equation 26 and Equation 27 to calculate R3 and R2.

$$R_2 = \frac{V_{HYST} - \left[\frac{0.1 \times V_{IN\text{–}RISE\_THRESHOLD} - 0.124}{1.24}\right] - 0.1}{18 \times 10^{-6}} \quad (26)$$

$$R_3 = \frac{1.24\,(R_2)}{V_{IN\text{–}RISE\_THRESHOLD} - 1.24} \quad (27)$$

8.3.11 Voltage Sampling and DAC Operation

The TPS92518-Q1 integrates an ADC (analog to digital converter) and 6 DACs (digital to analog converters). The single ADC is multiplexed to provide the VLEDx pin voltages (starting with: *LED1 Voltage*) and the TPS92518-Q1 die temperature (*Die Temperature Reading*). A simplified diagram is shown in Figure 32.

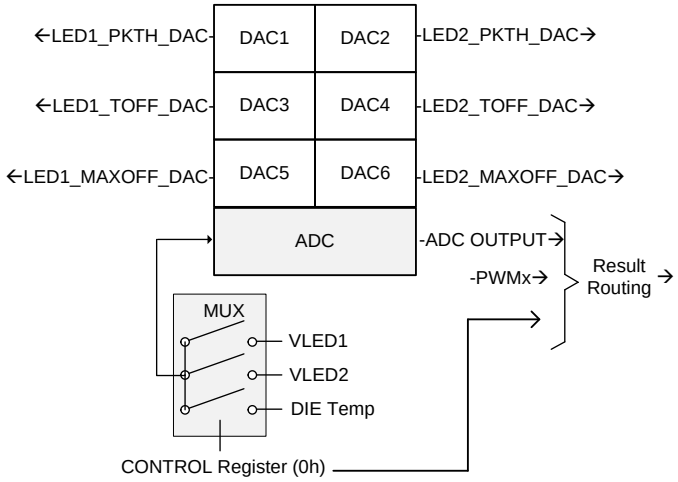


Figure 32. TPS92518-Q1 Internal Digital Blocks

8.3.11.1 ADC Control and LED Voltage Updating

Each of the analog outputs are controlled via their own individual DAC. The DAC's operate asynchronously and changes to controlling register values are updated immediately (~1 µs).

The ADC (analog to digital converter) sampling intervals are asynchronous to the incoming PWM1 and PWM2 signals. The TPS92518-Q1 logic determines which register(s) to update based on the state of the corresponding PWM signal at the time of ADC sampling. There are three LED voltage registers per channel:

- LEDx_MOST_RECENT
- LEDx_LAST_ON
- LEDx_LAST_OFF

The LEDx_MOST_RECENT registers are updated periodically every time the ADC has a new sample. Sampling a single input increases the sampling frequency. For example: an ADC sample and conversion requires ~100us. If one item is selected it is sampled at roughly 10 kHz. If all three inputs are selected each is sampled at ~3.3 kHz.

The LEDx_LAST_ON registers are only updated when the corresponding PWM input has toggled from high to low, and the LEDx_LAST_OFF registers are only updated when the corresponding PWM input has toggled from low to high. This allows the last sample before the falling edge of PWM to be saved as the LAST_ON value, and the last sample before the rising edge of PWM to be saved as the LAST_OFF value ensuring the most consistent LED voltage reading.

8.3.12 Device Functional Modes

8.3.12.1 Analog Dimming

Analog dimming refers to the method of controlling the peak inductor current as the method to set the continuous average output current. Analog dimming is controlled digitally via the SPI interface. The register control value is converted via a digital to analog converter and the peak inductor current is compared to this analog voltage level. The level can be updated at any time during operation.

8.3.12.2 PWM Dimming

PWM Dimming is accomplished via a channel's corresponding PWM pin. A 1.6-V (typical) rising threshold and a 0.8-V (typical) falling threshold are required.

8.4 Serial Interface

The 4-wire control interface is compatible with the Serial Peripheral Interface (SPI) bus. The control bus consists of four signals: SSN, SCK, MOSI, and MISO. The SSN, SCK, and MOSI pins are TTL inputs into the TPS92518-Q1 while the MISO pin is an open-drain output. The SPI bus can be configured for both star-connect and daisy chain hardware connections.

A bus transaction is initiated by a MCU on a falling edge of SSN. While SSN is low, the input data present on the MOSI pin is sampled on the rising edge of SCK, MSbit first. The output data is asserted on the MISO pin at the falling edge of SCK. The figure below shows the data transition and sampling edges of SCK.

A valid transfer requires a non-zero integer multiple of 16 SCK cycles (i.e., 16, 32, 48, etc.). If SSN is pulsed low and no SCK pulses are issued before SSN rises, a SPI error is reported. Similarly, if SSN is raised before the 16th rising edge of SCK, the transfer is aborted and a SPI error is reported. If SSN is held low after the 16th falling edge of SCK and additional SCK edges occur, the data continues to flow through the TPS92518-Q1 shift register and out the MISO pin. When SSN transitions from low-to-high, the internal digital block decodes the most recent 16 bits that were received prior to the SSN rising edge.

SSN must transition high only after a multiple of 16 SCK cycles for a transaction to be valid and not set the SPI error bit. In the case of a write transaction, the TPS92518-Q1 logic performs the requested operation when SSN transitions high. In the case of a read transaction, the read data is transferred during the next frame, regardless of whether a SPI error has occurred.

Serial Interface (continued)

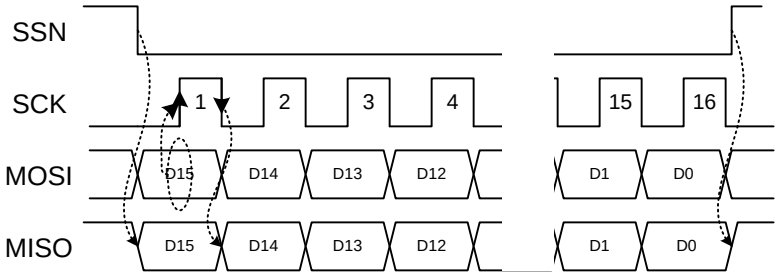


Figure 33. SPI Data Format

The data bit on MOSI is shifted into an internal 16-bit shift register (MSbit first) while data is simultaneously shifted out the MISO pin. While SSN is high (bus idle), MISO is tri-stated by the open-drain driver. While SSN is low, MISO is driven according to the 16-bit data pattern being shifted out based on the prior received command. At the falling edge of SSN to begin a new transaction, MISO is driven to the MSbit of the outbound data, and is updated on each subsequent falling edge of SCK.

NOTE

The first MISO transition happens on the first falling edge AFTER the first rising edge of SCK.

8.4.1 Command Frame

There is only one defined format for frames coming in on MOSI from the master. These are called Command frames. A Command frame can be either a read command or a write command.

A Command frame consists of a CMD bit, five bits of ADDRESS, a PARITY bit (odd parity), and nine bits of DATA. The format of the Command frame is shown in Figure 34. The bit sequence is as follows:

1. The COMMAND bit (CMD). CMD = 1 means the transfer is a write command; CMD = 0 means it is a read command.
2. The five-bit read or write ADDRESS (A4..A0).
3. The PARITY bit (PAR). This bit is set by the following equation: PARITY = XNOR(CMD, A4..A0, D8..D0).
4. Nine bits of read or write DATA (D8..D0). For a read, all data bits must be 0.

Both the Read Command and the Write Command follow the Command frame format as shown in Figure 34.

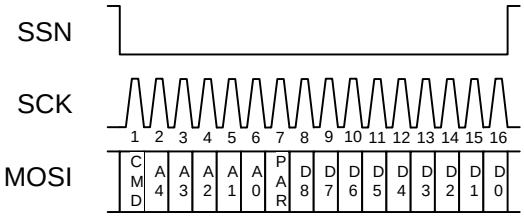


Figure 34. Command Frame Format

8.4.2 Response Frame Formats

There are three possible response frame formats: Read Response, Write Response and Write Error/POR. These formats are further described below.

Serial Interface (continued)

8.4.2.1 Read Response Frame Format

The Read Response frame has the following format. The read response frame contains the state of the four fault bits. A special command is not required to poll the status of the bits, they are returned in every read response.

1. The SPI Error bit (SPE).
2. Two reserved bits (always 1).
3. The POWER CYCLED bit PC).
4. The LED2 BOOTUV ERROR bit (UV2).
5. The LED1 BOOTUV ERROR bit “UV1).
6. The THERMAL WARNING bit (TW).
7. Nine bits of DATA (D8..D0).

This is shown in Figure 35 below. This frame is sent out by the TPS92518-Q1 following a read command.

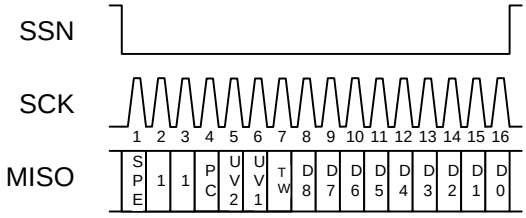


Figure 35. Read Response Frame Format

8.4.2.2 Write Response Frame Format

The Write Response frame has the following format:

1. The SPI Error bit (SPE).
2. The COMMAND bit (CMD).
3. Five bits of ADDRESS (A4..A0).
4. Nine bits of DATA (D8..D0).

This is shown in Figure 36. This frame is sent out following a write command if the previously received frame was a write command and no SPI Error occurred during that frame.

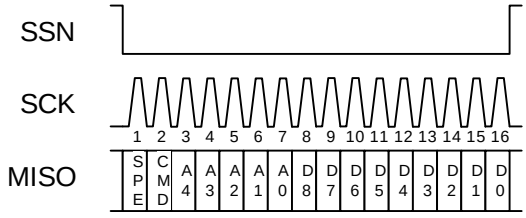


Figure 36. Write Response Frame Format

Serial Interface (continued)

8.4.2.3 Write Error/POR Frame Format

The Write Error/POR frame is simply a '1' in the MSB, followed by all zeroes (see Figure 37) This frame is sent out by the TPS92518-Q1 Internal digital block during the first SPI transfer following power-on reset, or following a write command with a SPI Error.

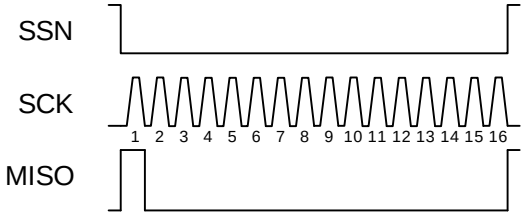


Figure 37. Write Error/POR

8.4.2.4 SPI Error

The TPS92518-Q1 records a SPI Error if any of the following conditions occur:

- The SPI command has a non-integer multiple of 16 SCK pulses.
- Any of the DATA bits during a read command are non-zero.
- There is a parity error in the previously received command.

If any of these conditions are true, the TPS92518-Q1 sets the SPI_ERROR bit in the Status Register. This is reported by setting the SPE (MSbit) in the next response frame. A write command with a SPI Error (not 16-bit aligned or bad parity) does NOT write to the register being addressed. The bad write is ignored and discarded. The TPS92518-Q1 attempts to respond to read requests regardless of SPI Error status since there is no danger to the system.

The SPI_ERROR bit can be cleared by reading the STATUS register.

8.5 Registers

Table 2 lists the memory-mapped registers. All register offset addresses not listed in Table 2 are considered as reserved locations and the register contents should not be modified.

Table 2. Registers

Address	Acronym	Register Name	Section
0h	CONTROL	Control Register	Go
1h	STATUS	Status Register	Go
2h	THERM_WARN_LMT	Thermal Warning Limit Register	Go
3h	LED1_PKTH_DAC	LED1 Peak Threshold DAC Register	Go
4h	LED2_PKTH_DAC	LED2 Peak Threshold DAC Register	Go
5h	LED1_TOFF_DAC	LED1 Off Time DAC Register	Go
6h	LED2_TOFF_DAC	LED2 Off Time DAC Register	Go
7h	LED1_MAXOFF_DAC	LED1 Maximum Off Time DAC Register	Go
8h	LED2_MAXOFF_DAC	LED2 Maximum Off Time DAC Register	Go
9h	VTHERM	VTHERM Register	Go
Ah	LED1_MOST_RECENT	LED1 Most Recent Register	Go
Bh	LED1_LAST_ON	LED1 Last ADC On Register	Go
Ch	LED1_LAST_OFF	LED1 Last ADC Off Register	Go
Dh	LED2_MOST_RECENT	LED2 Most Recent ADC Register	Go
Eh	LED2_LAST_ON	LED2 Last On ADC Register	Go
Fh	LED2_LAST_OFF	LED2 Last Off ADC Register	Go
10h	RESET	Reset Register	Go

8.5.1 CONTROL Register (Address = 00h) [reset = 00h]

CONTROL is shown in Figure 38 and described in Table 3.

Return to Summary Table.

Figure 38. CONTROL Register

8	7	6	5	4	3	2	1	0
RESERVED				THERM SMPL EN	VLED2 SMPL EN	VLED1 SMPL EN	LED2 EN	LED1 EN
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

(1) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 3. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
8-5	RESERVED	R	0	Reserved
4	THERM_SMPL_EN	R/W	0	Thermal sample enable 0 = Disable sampling 1 = Enable sampling
3	VLED2_SMPL_EN	R/W	0	VLED2 sample enable 0 = Disable sampling 1 = Enable sampling
2	VLED1_SMPL_EN	R/W	0	VLED1 sample enable 0 = Disable sampling 1 = Enable sampling
1	LED2_EN	R/W	0	LED2 enable. This bit controls the operation state of channel 2. 0 = Disable LED channel 2 1 = Enable LED channel 2
0	LED1_EN	R/W	0	LED1 enable. This bit controls the operation state of channel 1. 0 = Disable LED channel 1 1 = Enable LED channel 1

xSMPL_EN: The TPS92518-Q1 Analog to Digital Converter (ADC) input is multiplexed between 3 inputs: the thermal sensor and the two output voltages. Each input is sampled consecutively. Sampling a single input increases the sampling frequency. For example: an ADC sample and conversion requires ~100us. If one item is selected it is sampled at roughly 10 kHz. If all three inputs are selected each is sampled at ~3.3 kHz.

LEDx_EN: The TPS92518-Q1 PWMx pin AND the corresponding LEDxEN bit must be high for a channel to be enabled. If not using the external PWM input, tie the pin to VCC. The use of the LEDxEN register also enables the corresponding channel SWx pin internal pull-down to ensure no current flows to the LED load. A sample of the timing and waveforms around a SPI enable write are shown in Figure 39.

LEDxEN control may be bypassed using an analog activated override via the EN/UV pin. By applying a voltage $>V_{EN/UV2}$ (23.6 V Typical) the contents of LEDxEN are ignored and the TPS92518-Q1 operates without SPI communication using the default register values. This is discussed in EN/UV2 - SPI Control Bypass

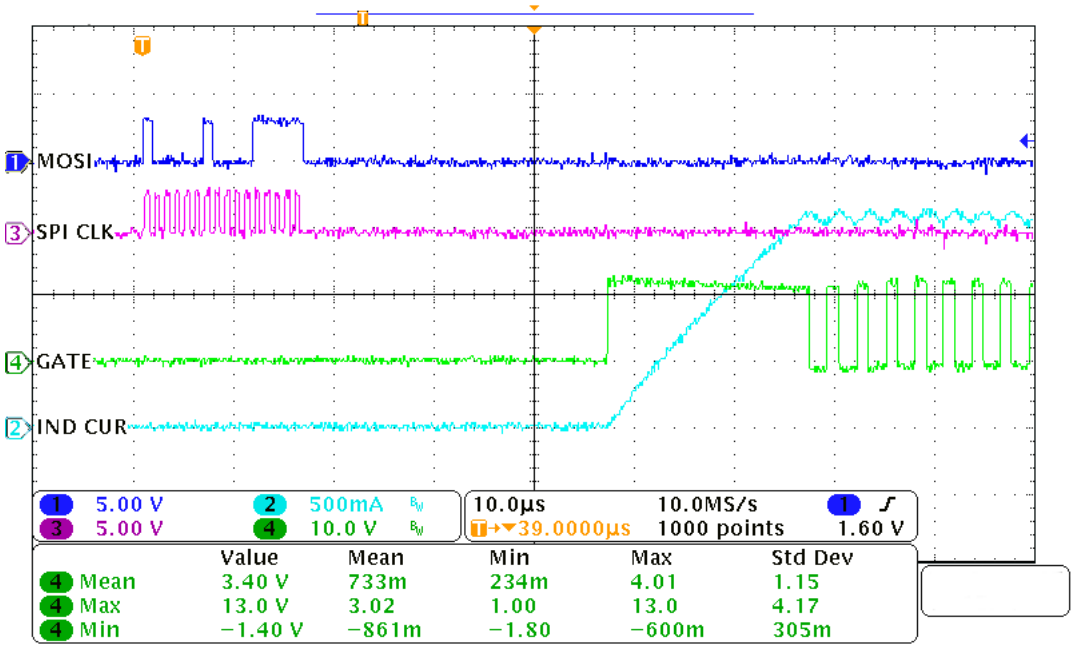


Figure 39. SPI Enable Write Waveform Example

8.5.2 STATUS (FAULT) Register (Address = 01h) [reset = 10h]

STATUS is shown in Figure 40 and described in Table 4.

Return to Summary Table.

Figure 40. STATUS Register

8	7	6	5	4	3	2	1	0
RESERVED				POWER CYCLED	LED2BOOTUV ERROR	LED1BOOTUV _ERROR	THERMAL _ WARNING	SPI _ERROR
R-0h				RtoCl-1h	RtoCl-0h	RtoCl-0h	RtoCl-0h	RtoCl-0h

(1) R/W = Read/Write; R = Read Only RtoCl = Read to clear bit; -n = value after reset

Table 4. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
8-5	RESERVED	R	0	Reserved
4	POWER_CYCLED	RtoCl	1	Power cycled. This bit indicates that a power-on reset has occurred since the last STATUS register read. 0h = No power cycle has occurred since the last STATUS read. 1h = A power cycle has occurred since the last STATUS read.
3	LED2_BOOTUV_ERROR	RtoCl	0	Latched LED2 BOOTUV error. This bit is cleared by reading the STATUS register if the condition is no longer present.
2	LED1_BOOTUV_ERROR	RtoCl	0	Latched LED1 BOOTUV error. This bit is cleared by reading the STATUS register if the condition is no longer present.
1	THERMAL_WARNING	RtoCl	0	Latched thermal warning flag: This bit is cleared by reading the STATUS register if the condition is no longer present. 0h = No thermal warning has occurred since the last STATUS read. 1h = A thermal warning has occurred since the last STATUS read.

Table 4. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	SPI_ERROR	RtoCl	0	Latched SPI error flag 0h = No SPI error occurred since the last STATUS read. 1h = A SPI error has occurred since the last STATUS read.

POWER_CYCLED: This bit is set each time the input power is cycled to the TPS92518-Q1, including the first time the TPS92518-Q1 is powered on. To utilize this feature, read the bit as part of the start-up routine.

x_BOOTUV_ERROR: Set any time the high-side FET 'BOOT' drive circuit falls below $V_{BOOT-UVLO}$ (4.6 V typical). *Note*: This can be used to detect that the LED load is open, or that a drop-out condition is occurring. (any time V_{VIN} ~= V_{VLEDx}) For example: the LED load is removed from the output. There is no path for current flow and no increase of voltage on the sense resistor. The high-side FET remains ON requiring some current draw from the BOOT capacitor. After some time (milli-second magnitude) the capacitor is depleted, and reaches $V_{BOOT-UVLO}$. At this point the high-side FET is turned off and the LEDx_BOOTUV_ERROR flag set. The boot capacitor is then be re-charged. See *BOOT Capacitor and BOOT UVLO* for more information.

SPI_ERROR: This error is cleared by reading the STATUS register. A SPI error is caused by any of the following conditions:

- A non-integer-multiple of 16 clocks received during a SPI transfer
- Any of the DATA bits are non-zero during a SPI read command
- SPI parity error during a SPI read or write command.

The TPS92518-Q1 detects and reports certain communication and system conditions. The SPI Error status is reported with every response frame. This is useful to quickly diagnose a communication problem and attempt to fix it. On a read response frame, the TPS92518-Q1 reports the Power Cycled, Boot UV and Thermal Warning status bits, as reflected in the STATUS register. Any power and/or system faults are immediately reported on ANY read response which allows the controlling MCU to more quickly respond to system problems. (See Read Response Frame Format)

8.5.3 THERM_WARN_LMT Register (Address = 02h) [reset = 80h]

THERM_WARN_LMT is shown in Figure 41 and described in Table 5.

Return to Summary Table.

Figure 41. THERM_WARN_LMT Register

8	7	6	5	4	3	2	1	0
Reserved	THERM_WARN_LMT							
R-0h	R/W-80h							

(2) R/W = Read/Write; R = Read Only; RtoCl = Read to clear bit; -n = value after reset

Table 5. THERM_WARN_LMT Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	THERM_WARN_LMT	R/W	80h	Thermal warning voltage limit. If the ADC value of VTHERM (Register 9h) exceeds this limit, the THERMAL_ERROR bit in the STATUS register is set.

THERM_WARN_LMT : The Thermal Warning status register is controlled by the content of this register.

Use Equation 28 to calculate the value for the register for the desired Thermal Warning Limit.

$$\text{Thermal Warning Limit } (^{o}\text{C}) = \left[2.439 \text{ x VTHERM\_WARN\_LMT}[7:0]\right] - 293.5 \quad (28)$$

8.5.4 LED1_PKTH_DAC Register (Address = 03h) [reset = 80h]

LED1_PKTH_DAC is shown in Figure 42 and described in Table 6.

Return to Summary Table.

Figure 42. LED1_PKTH_DAC Register

8	7	6	5	4	3	2	1	0
Reserved	LED1_PKTH_DAC							
R-0h	R/W-80h							

(3) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 6. LED1_PKTH_DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED1_PKTH_DAC	R/W	80h	Channel 1 peak threshold DAC value.

The content of the register is used to set the peak inductor current ($I_{Lx\text{-}peak}$). The register value sets the voltage across the sense resistor (V_{CSPx}-V_{CSNx}) that ends the converter on-time.

The register value can be modified at any time during operation and the DAC analog value is then updated in ~1us. Always use the highest value that the application allows to reduce accuracy error. For example, the amount of variation in the actual peak threshold for LEDx_PKTH_DAC = 255 is less than for LEDx_PKTH_DAC = 127.

The Peak Current Threshold Voltage in volts (the voltage measured across the sense resistor that trips the peak current comparator) is simply the register value divided by 1000. (Consider the decimal register value to be in milli-volts)

The Peak Current Threshold in Amps can be calculated using Equation 29

$$I_{Lx-peak} = \frac{\text{LEDx\_PKTH\_DAC}[7:0]}{1000 \times R_{SENSE}} \quad (29)$$

8.5.5 LED2_PKTH_DAC Register (Address = 04h) [reset = 80h]

LED2_PKTH_DAC is shown in Figure 43 and described in Table 7.

Return to Summary Table.

Figure 43. LED2_PKTH_DAC Register

8	7	6	5	4	3	2	1	0
Reserved	LED2_PKTH_DAC							
R-0h	R/W-80h							

(4) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 7. LED2_PKTH_DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED2_PKTH_DAC[7:0]	R/W	80h	Channel 2 peak threshold DAC value.

The content of the register is used to set the peak inductor current ($I_{Lx\text{-}peak}$). The register value sets the voltage across the sense resistor (V_{CSPx}-V_{CSNx}) that ends the converter on-time.

The register value can be modified at any time during operation and the DAC analog value is then updated in ~1us. Always use the highest value that the application allows to reduce accuracy error. For example, the amount of variation in the actual peak threshold for LEDx_PKTH_DAC = 255 is less than for LEDx_PKTH_DAC = 10.

The Peak Current Threshold Voltage in volts (the voltage measured across the sense resistor that trips the peak current comparator) is simply the register value divided by 1000. (Consider the decimal register value to be in milli-volts)

The Peak Current Threshold in Amps can be calculated using Equation 30

$$I_{Lx-peak} = \frac{LEDx\_PKTH\_DAC[7:0]}{1000 \times R_{SENSE}} \quad (30)$$

8.5.6 LED1_TOFF_DAC Register (Address = 05h) [reset = 80h]

LED1_TOFF_DAC is shown in Figure 44 and described in Table 8.

Return to Summary Table.

Figure 44. LED1_TOFF_DAC Register

8	7	6	5	4	3	2	1	0
Reserved	LED1_TOFF_DAC							
R-0h	R/W-80h							

(5) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 8. LED1_TOFF_DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED1_TOFF_DAC[7:0]	R/W	80h	Channel 1 off time DAC value.

See LED2_TOFF_DAC Register (Address = 06h) [reset = 80h] for information on setting LED1_TOFF_DAC.

8.5.7 LED2_TOFF_DAC Register (Address = 06h) [reset = 80h]

LED2_TOFF_DAC is shown in Figure 45 and described in Table 9.

Return to Summary Table.

Figure 45. LED2_TOFF_DAC Register

8	7	6	5	4	3	2	1	0
Reserved	LED2_TOFF_DAC							
R-0h	R/W-80h							

(6) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 9. LED2_TOFF_DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED2_TOFF_DAC[7:0]	R/W	80h	Channel 2 off time DAC value.

LEDx_TOFF_DAC: The content of this register AND corresponding VLEDx pin set the corresponding channel off-time.

Important: →Ensure code controlling the TOFF register for both channels maintains limits on this register value. It is possible to write a value that is too low that may damage the application. See Off-Time Thresholds - LEDx_TOFF_DAC and LEDx_MAXOFF_DAC for more details about controlling this register value.

$$t_{OFF} = \frac{LEDx\_TOFF\_DAC[7:0]}{2.136 \times 10^{6} \times VLEDx} \quad (31)$$

Where t_{OFF} is in seconds. It can also be described as a setting for the channel V·µs product. The V·µs relation ensures the converter peak-peak ripple is constant and maintains the converter regulation.

8.5.8 LED1_MAXOFF_DAC Register (Address = 07h) [reset = 80h]

LED1_MAXOFF_DAC is shown in Figure 46 and described in Table 10.

Return to Summary Table.

Figure 46. LED1_MAXOFF_DAC Register

8	7	6	5	4	3	2	1	0
Reserved	LED1_MAXOFF_DAC							
R-0h	R/W-80h							

(7) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 10. LED1_MAXOFF_DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED1_MAXOFF_DAC[7:0]	R/W	80h	Channel 1 maximum off time DAC value.

See LED2_MAXOFF_DAC Register (Address = 08h) [reset = 80h] for information on setting the LED1_MAXOFF_DAC register.

8.5.9 LED2_MAXOFF_DAC Register (Address = 08h) [reset = 80h]

LED2_MAXOFF_DAC is shown in Figure 47 and described in Table 11.

Return to Summary Table.

Figure 47. LED2_MAXOFF_DAC Register

8	7	6	5	4	3	2	1	0
Reserved	LED2_MAXOFF_DAC							
R-0h	R/W-80h							

(8) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 11. LED2_MAXOFF_DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED2_MAXOFF_DAC[7:0]	R/W	80h	Channel 2 maximum off time DAC value.

LEDx_MAXOFF_DAC: the content of this register sets the maximum off-time for the corresponding channel, regardless of output voltage. LEDxMAXOFF and LEDx_TOFF operate in parallel. In normal operation, LEDxMAXOFF must always be longer in time than LEDxTOFF so as not to interfere with the normal operation of the converter.

$$\text{Maximum Off Time (s)} = \text{LEDx\_MAXOFF\_DAC}[7:0] \times (251 \times 10^{-9}) \quad (32)$$

The MaxOffTime value is most useful in LED Matrix or shunt-FET dimming applications. When the output LED voltage is sufficiently low (<2V), regular operation of the off-timer is not possible. This parallel timer does not rely on the output voltage and can be set to maintain consistent inductor current peak-to-peak ripple. Refer to the application section *Off-Time Thresholds - LEDx_TOFF_DAC and LEDx_MAXOFF_DAC* for equations to properly set the maximum off time under shunted conditions.

The Maximum off-time is also the time that must expire before the first cycle is initiated at start-up, or after a POR.

8.5.10 VTHERM Register (Address = 09h) [reset = 0h]

VTHERM is shown in Figure 48 and described in Table 12.

Return to Summary Table.

Figure 48. VTHERM Register

8	7	6	5	4	3	2	1	0
Reserved	VTHERM							
R-0h	R-0h							

(9) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 12. VTHERM Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	VTHERM[7:0]	R	0h	Most recent ADC value of voltage on internal thermal sensor (based on a DeltaVBE).

The content of the VTHERM register represents the TPS92518-Q1 die temperature. Use Equation 33 to convert to degrees Celsius. The conversion is approximately 2.5ºC per LSB. The part-to-part temperature reading variation is ±10ºC or ±4lsb. This is the maximum variation a population of parts will have at a given temperature. If a single part temperature is read and then the temperature changes and returns to the same temperature, the reading will vary ±1 lsb from the original reading.

$$\text{Die Temperature (°C)} = \left(2.439 \text{ x VTHERM}[7:0]\right) - 293.5 \quad (33)$$

8.5.11 LED1_MOST_RECENT Register (Address = 0Ah) [reset = 0h]

LED1_MOST_RECENT is shown in Figure 49 and described in Table 13.

Return to Summary Table.

Figure 49. LED1_MOST_RECENT Register

8	7	6	5	4	3	2	1	0
PWM1	LED1_MOST_RECENT							
R-0h	R-0h							

(10) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 13. LED1_MOST_RECENT Register Field Descriptions

Bit	Field	Type	Reset	Description
8	PWM1	R	0	State of PWM1 when most recent ADC conversion of VLED1 voltage was started.
7-0	LED1_MOST_RECENT[7:0]	R	0h	Most recent ADC value of voltage on the VLED1 pin.

This register contains the last LEDx reading recorded by the internal ADC along with the state of the corresponding PWM pin state at the time the value was recorded. See *Voltage Sampling and DAC Operation* for more detailed information about LED voltage sampling control. This sample occurs at anytime and is not co-ordinated with the PWMx input pin.

$$\text{LEDx\_MOST\_RECENT (Volts)} = \text{LEDx\_MOST\_RECENT}[7:0] \text{ x } 0.26 \quad (34)$$

8.5.12 LED1_LAST_ON Register (Address = 0Bh) [reset = 0h]

LED1_LAST_ON is shown in Figure 50 and described in Table 14.

Return to Summary Table.

Figure 50. LED1_LAST_ON Register

8	7	6	5	4	3	2	1	0
Reserved	LED1_LAST_ON							
R-0h	R-0h							

(11) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 14. LED1_LAST_ON Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED1_LAST_ON[7:0]	R	0h	Last ADC value of voltage on VLED1 pin before falling edge of PWM1

Contains the last ADC recorded value of the LED1 voltage before the falling edge of PWM1. This ensures the most stable and consistent recorded value of the output voltage.

$$LEDx\_LAST\_ON\,(Volts) = LEDx\_LAST\_ON[7:0] \times 0.26 \quad (35)$$

See Voltage Sampling and DAC Operation for more information on LED voltage sampling.

8.5.13 LED1_LAST_OFF Register (Address = 0Ch) [reset = 0h]

LED1_LAST_OFF is shown in Figure 51 and described in *Table 15*.

Return to Summary Table.

Figure 51. LED1_LAST_OFF Register

8	7	6	5	4	3	2	1	0
Reserved	LED1_LAST_OFF							
R-0h	R-0h							

(12) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 15. LED1_LAST_OFF Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED1_LAST_OFF[7:0]	R	0h	~~!~ Last ADC value of voltage on VLED1 pin before rising edge of PWM1~~ !~ Last ADC value of voltage on VLED1 pin before rising edge of PWM1

Contains the last ADC recorded value of the LED1 voltage before the rising edge of PWM1. This ensures the most stable and consistent recorded value of the output voltage when the PWM signal was low.

$$LEDx\_LAST\_OFF\,(Volts) = LEDx\_LAST\_OFF[7:0] \times 0.26 \quad (36)$$

See *Voltage Sampling and DAC Operation* for more information on LED voltage sampling.

8.5.14 LED2_MOST_RECENT Register (Address = 0Dh) [reset = 0h]

LED2_MOST_RECENT is shown in Figure 52 and described in Table 16.

Return to Summary Table.

Figure 52. LED2_MOST_RECENT Register

8	7	6	5	4	3	2	1	0
Reserved	LED2_MOST_RECENT							
R-0h	R-0h							

(13) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 16. LED2_MOST_RECENT Register Field Descriptions

Bit	Field	Type	Reset	Description
8	PWM2	R	0	State of PWM2 when most recent ADC conversion of VLED2 pin voltage was started.
7-0	LED2_MOST_RECENT[7:0]	R	0h	Most recent ADC value of voltage on the VLED2 pin.

See section *LED1_MOST_RECENT Register*. Information on *LED1_MOST_RECENT Register (Address = 0Ah) [reset = 0h]* is the same as *LED2_MOST_RECENT Register*

8.5.15 LED2_LAST_ON Register (Address = 0Eh) [reset = 0h]

LED2_LAST_ON is shown in Figure 53 and described in Table 17.

Return to Summary Table.

Figure 53. LED2_LAST_ON Register

8	7	6	5	4	3	2	1	0
Reserved	LED2_LAST_ON							
R-0h	R-80h							

(14) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 17. LED2_LAST_ON Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED2_LAST_ON[7:0]	R	0h	Last ADC value of voltage on VLED2 pin before falling edge of PWM2

See section *LED1_LAST_ON Register (Address = 0Bh) [reset = 0h]* for more information on LED2_LAST_ON. Operation of each of the LAST_ONx registers is the same.

8.5.16 LED2_LAST_OFF Register (Address = 0Fh) [reset = 0h]

LED2_LAST_OFF is shown in Figure 54 and described in Table 18.

Return to Summary Table.

Figure 54. LED2_LAST_OFF Register

8	7	6	5	4	3	2	1	0
Reserved	LED2_LAST_OFF							
R-0h	R-0h							

(15) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 18. LED2_LAST_OFF Register Field Descriptions

Bit	Field	Type	Reset	Description
8	RSVD	R	0	Reserved
7-0	LED2_LAST_OFF[7:0]	R	0h	Last ADC value of voltage on the VLED2 pin before rising edge of PWM2

See section LED1_LAST_OFF Register (Address = 0Ch) [reset = 0h] for more information on LED2_LAST_OFF. Operation of each of the LAST_OFFx registers is the same.

8.5.17 Reset Register (Address = 10h) [reset = 0h]

Reset is shown in Figure 55 and described in Table 19.

Return to Summary Table.

Figure 55. Reset Register

8	7	6	5	4	3	2	1	0
Reset								
R/W-0h								

(16) R/W = Read/Write; R = Read Only ; RtoCl = Read to clear bit; -n = value after reset

Table 19. Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
8	Reset[8:0]	R/W	0h	Write 0x0C3 to the RESET register to reset all writable registers to their default values. This register is write-only. Reads of this register return 0.

The RESET register provides a means to reset all the writable registers to their default values.

8.6 Programming

Coding examples outline common TPS92518-Q1 tasks.

8.6.1 TPS92518-Q1 Register Typedef - Sample Code

```
// TPS92518 Registers
typedef enum
{
            CONTROL = 0x00,
            STATUS = 0x01,
            THERM_WARN_LMT = 0x02,
            LED1_PKTH_DAC = 0x03,
            LED2_PKTH_DAC = 0x04,
            LED1_TOFF_DAC = 0x05,
            LED2_TOFF_DAC = 0x06,
            LED1_MAXOFF_DAC = 0x07,
            LED2_MAXOFF_DAC = 0x08,
            VTHERM = 0x09,
            LED1_MOST_RECENT = 0x0A,
            LED1_LAST_ON = 0x0B,
            LED1_LAST_OFF = 0x0C,
            LED2_MOST_RECENT = 0x0D,
            LED2_LAST_ON = 0x0E,
            LED2_LAST_OFF = 0x0F,
            RESET = 0x10
}Registers518;
```

8.6.2 Command Frame - Sample Code

The *Command Frame* can be constructed using the following code:

```
//assemble the 16-bit command
uint_t AssembleSPICmd(bool write, Registers518 regAddr, uint16_t data)
{
        uint16_t assembledCmd = 0; // Build this to shift through parity calc
        uint16_t parity = 0;       // Parity bit calculated here
        uint16_t packet = 0;       // This will be what we send

    // Set the CMD bit high if this is a write
    if(write)
    {
        assembledCmd |= 0x8000;  // Set CMD = 1
    }

    // Move the register address into the correct position
    assembledCmd |= (( regAddr << 10) & 0x7C00);

    // Append the data for a write
    if(write)
    {
        assembledCmd |= (data & 0x01FF);
    }

    // Save this off into the returned variable
    packet = assembledCmd;

    // Calculate the parity bit
    while(assembledCmd > 0)
    {
        // Count the number of 1s in the LSb
        if(assembledCmd & 0x0001)
        {
            parity++;
        }
        // Shift right
        assembledCmd >>= 1;
    }

    // If the LSb is a 0 (even # of 1s), we need to add the odd parity bit
    if(!(parity & 0x0001))
    {
        packet |= (1 << 9);
```

Programming (continued)

```
    }

    return(packet);
}
```

8.6.3 SPI Read/Write - Sample Code

Perform a SPI read/write; with assumption that the buffer holding write data has been filled using the AssembleSPICmd function, Then send the 16-bit characters. Lower numbered array elements are nearer the MCU in the daisy-chain.

```
/* Perform the SPI read/write; assumed that the buffer holding write data has been filled
 * using the AssembleSPICmd function. */

void SendSPIPacket(uint16_t chainID, uint16_t *writeBuf_ptr, uint16_t *readBuf_ptr)
{
        uint16_t i;

        // Which SSN to take low; SSx_LOW is a macro for GPO manipulation switch(chainID)
        {
        case 0:
            SS0_LOW();
            break;
        case 1:
            SS1_LOW();
            break;
        case 2:
            SS2_LOW();
            break;
        default:
            break;
        }

  // Send the 16-bit characters; lower numbered array elements are nearer the MCU in the daisy-chain
    for(i = NUM_DEVICES_PER_CHAIN; i >= 1; i--)
    {
        SpibRegs.SPITXBUF = *(writeBuf_ptr + (i-1));   // Send each 16-bit piece of the packet
        while(SpibRegs.SPISTS.bit.INT_FLAG == 0);      // Wait for buffer to empty
        *(readBuf_ptr + (i-1)) = SpibRegs.SPIRXBUF;    // Grab the TPS92518 response
    }

    // Small delay to ensure all data is shifted out
    DELAY_US(5);

    // Make sure all SSN#s are high (SSx_HIGH is a macro)
    SS0_HIGH();
    SS1_HIGH();
    SS2_HIGH();
}
```

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS92518-Q1 buck current controller is suitable for implementing step-down LED drivers. This section presents a simplified design process for an LED driver with the specifications shown in Design Requirements:

Use the following design procedure to select component values for this and similar buck applications.

9.2 Typical Application

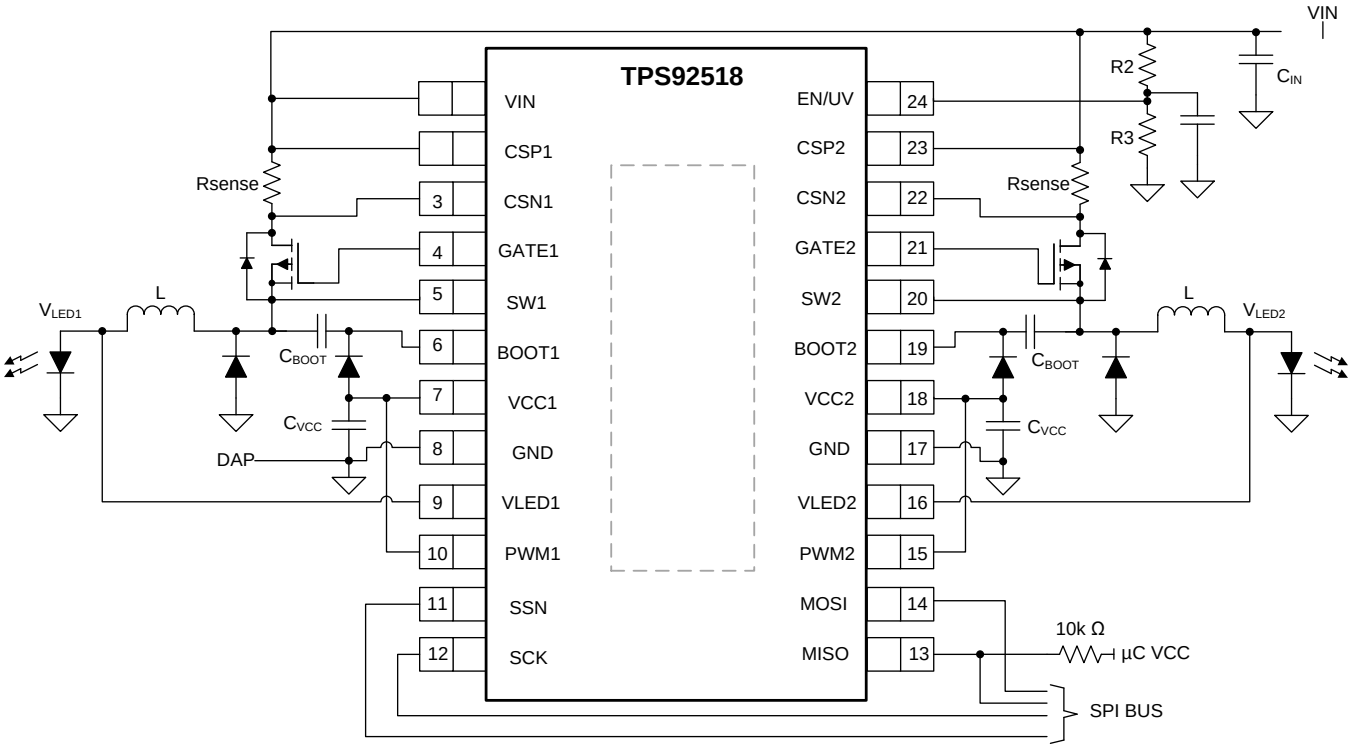


Figure 56. Typical Application Schematic

9.2.1 Design Requirements

Buck converter topology.

Table 20. Design Requirements

PARAMETER		VALUE	UNIT
V_{IN}	Input voltage	50	V
I_{LED}	LED current	1.6	A
V_{LED}	LED voltage	9.4	V
ΔI_{L-PP}	Ripple voltage change	12.5%	
LEDx_PK_DAC[7:0]	Target switching frequency	550	kHz
$V_{EN/UV}$		40	V

Typical Application (continued)

Table 20. Design Requirements (continued)

PARAMETER		VALUE	UNIT
$V_{EN/UV-HYST}$		5	V

9.2.2 Detailed Design Procedure

TPS92518-Q1 Design Equations and sample Calculations.

Start by calculating the converter Duty Cycle

1. **Calculate D:**

$$D = \frac{VLEDx}{V_{IN} \times \eta} = \frac{9.4}{50 \times 0.9} = 0.209 \quad (37)$$

2. **Calculate Off Time Estimate:**
   1. Using Switching Period (T)
      1. $T = t_{OFF} + t_{ON} = t_{OFF} + (D \times T)$, and $T = 1/f_{SW}$

         then:

$$t_{OFF} = \frac{1}{f_{SW}} \times (1-D) = \frac{1}{550\,kHz} \times (1-0.209) = 1.44\,\mu s \quad (38)$$

3. **Compute the off-time register value:**

$$[LEDx\_TOFF\_DAC] = t_{OFF} \times (2.136x10^6) \times VLEDx = 1.44\,\mu s \times 2.136x10^6 \times 9.4 = 29 = 1Dh \quad (39)$$

4. **Calculate the inductance:** Where ΔI_{L-PP} is in Amps.

$$\Delta I_{L-PP}(Amps) = \Delta I_{L-PP\%} \times I_{LED} = 0.125 \times 1.6 = 200mA \quad (40)$$

$$L = \frac{t_{OFF} \times VLEDx}{\Delta I_{L-PP}} = \frac{1.44\,\mu s \times 9.4}{0.2} = 67.68\,\mu H \quad (41)$$

   The user has the option of choosing a value of 68µH, however, this design uses the next common value of 100 µH in order to meet the ripple requirements. When selecting an inductor, ensure both the average and peak current values are met with adequate margin.

5. **Calculate the sense resistor:**For the highest current set-point, set the peak threshold register to be as high as possible. Use [LEDx_PKTH_DAC] = 255 (the maximum value) if possible to increase the converter accuracy. Only use something lower if it is possible the average current level requires adjustment after the design is complete and the BOM is complete. For example, if the production flow includes a trimming step.

$$I_{Lx-peak} = I_{LED} + \frac{\Delta I_{L-PP}}{2} = 1.6 + \frac{0.2}{2} = 1.7A \quad (42)$$

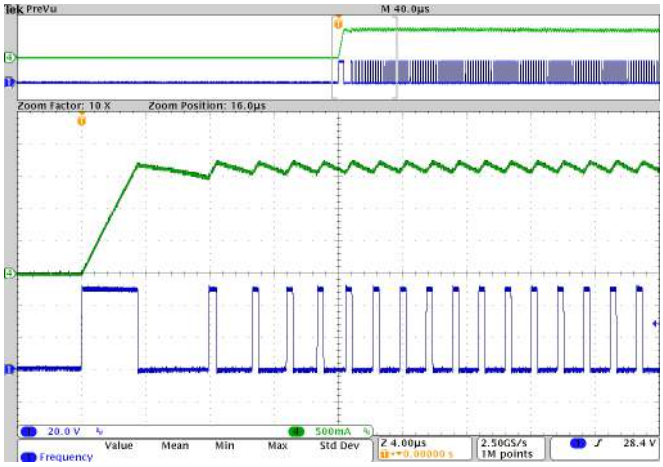
$$R_{SENSE} = \frac{[LEDx\_PKTH\_DAC]}{1000 \times I_{Lx-peak}} = \frac{255}{1000 \times 1.7} = 0.15\Omega \quad (43)$$

6. **Calculate the UVLO Resistors:** Considering the turn-on point of 40 V and a 5 V hysteresis values for the UVLO resistors can be selected. (Refer to Figure 31 for configuration details.)

$$R_2 = \frac{V_{HYST} - \left[\frac{0.1 \times V_{IN-RISE\_THRESHOLD} - 0.124}{1.24}\right] - 0.1}{18 \times 10^{-6}} = \frac{5 - \left[\frac{(0.1 \times 40) - 0.124}{1.24}\right] - 0.1}{18 \times 10^{-6}} = 98.6\,k\Omega \quad (44)$$

$$R_3 = \frac{1.24\,(R_2)}{V_{IN-RISE\_THRESHOLD} - 1.24} = \frac{1.24\,(98.6k)}{40 - 1.24} = 3.15\,k\Omega \quad (45)$$

9.2.3 Application Curves

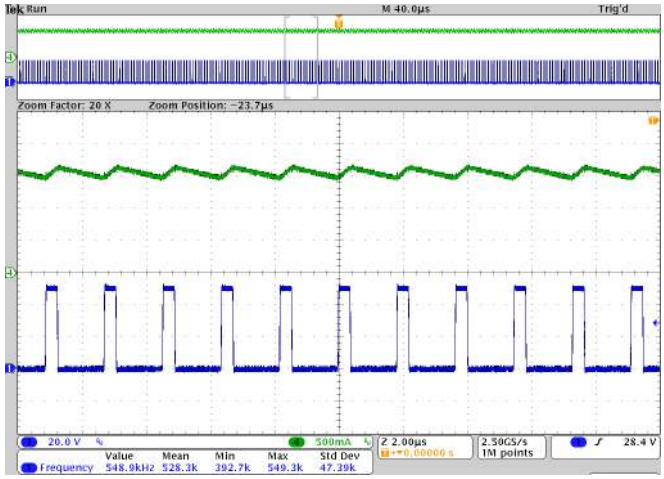


CH4 (Green) : Inductor Current (500 mA per division)

CH1 (Blue) : SWx Node (20 V per division)

Time Base: 4µs per division

Figure 57. TPS92518-Q1 Start-Up



CH4 (Green) : Inductor Current (500 mA per division)

CH1 (Blue) : SWx Node (20 V per division)

Time Base: 2µs per division

Figure 58. TPS92518-Q1 Normal Steady-State Operation

TPS92518-Q1 Useful Equations:

Converter Output Equation (A) (Ideal)

$$I_{LED} = \left[\frac{LEDx\_PKTH\_DAC[7:0]}{1000 \times R_{SENSE}}\right] - \left[\frac{LEDx\_TOFF\_DAC[7:0]}{2 \times L \times 2.136 \times 10^{6}}\right] \quad (46)$$

Converter Output Equation (A) (With error sources)

$$I_{LED} = \left(\frac{\left[\frac{LEDx\_PKTH\_DAC[7:0]}{1000} \pm V_{CSTx-OFFSET}\right]}{R_{SENSE}} \pm \frac{(V_{IN} - VLEDx) \times t_{DEL}}{L}\right) - \left(\frac{\left[\left[\frac{LEDx\_TOFF\_DAC[7:0]}{2.136 \times 10^{6} \times VLEDx}\right] \pm t_{D-OFF}\right] \times VLEDx}{2 \times L}\right) \quad (47)$$

9.3 Dos and Don'ts

Do:

- Check the TPS92518-Q1 case and junction temperature during and after prototyping of any solution.
- Check the soldering of the device thermal pad (DAP) in production

Don't:

- Don't write 0 (zero) to any of the off-time registers ([LEDx_TOFF_DAC] or LEDxMAXOFF_DAC] unless the use case is well understood and tested.

10 Power Supply Recommendations

The TPS92518-Q1 was designed with the consideration of two main input source possibilities: direct from battery or from the output of a boost stage. For either application, ensure input voltage ripple requirements are met. The input ripple must go no higher than 10% of the input voltage to a maximum of 3 V.

10.1 Input Source Direct from Battery

Operation direct from battery has been considered when designing the TPS92518-Q1. The device ratings are such that load dump and other battery voltage excursions should not exceed the ratings of the device. When the battery voltage drops, the device's ability to run in to drop-out and various UVLO controls ensure a controlled recovery and no device damage. The BOOT UVLO protection allows duty cycles over 99%.

10.2 Input Source from a Boost Stage

The TPS92518-Q1 maximum input voltage of 65 V makes it a suitable second stage buck regulator(s) for a variety of applications and LED output configurations. For an average LED forward voltage of 3.5 V, and allowing for some headroom below the 65-V maximum input, the TPS92518-Q1 can successfully control up to 17 LEDs connected in series.

11 Layout

11.1 Layout Guidelines

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines maximizes noise rejection and minimizes the generation of EMI within the circuit. Figure 59 shows a sample layout and the associated current loops.

- Discontinuous currents are the type of current most likely to generate EMI, therefore care should be taken when routing these paths. – The main path for discontinuous current contains the input capacitor, the recirculating diode, the MOSFET (CSN pin to SW pin), and the sense resistor (RSENSE) shown as LOOP2. Make LOOP2 as small as possible. – Make the connections between all three components short and thick to minimize parasitic inductance. In particular, the switchnode (where L1, D1 and the SW pin connect, shown as LOOP1) should be only large enough to connect the components without excessive heating from the current it carries.
- In some applications the LED load can be far away (several inches or more) from the device, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED load is large or separated from the main converter, the output capacitor must be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

11.2 Layout Example

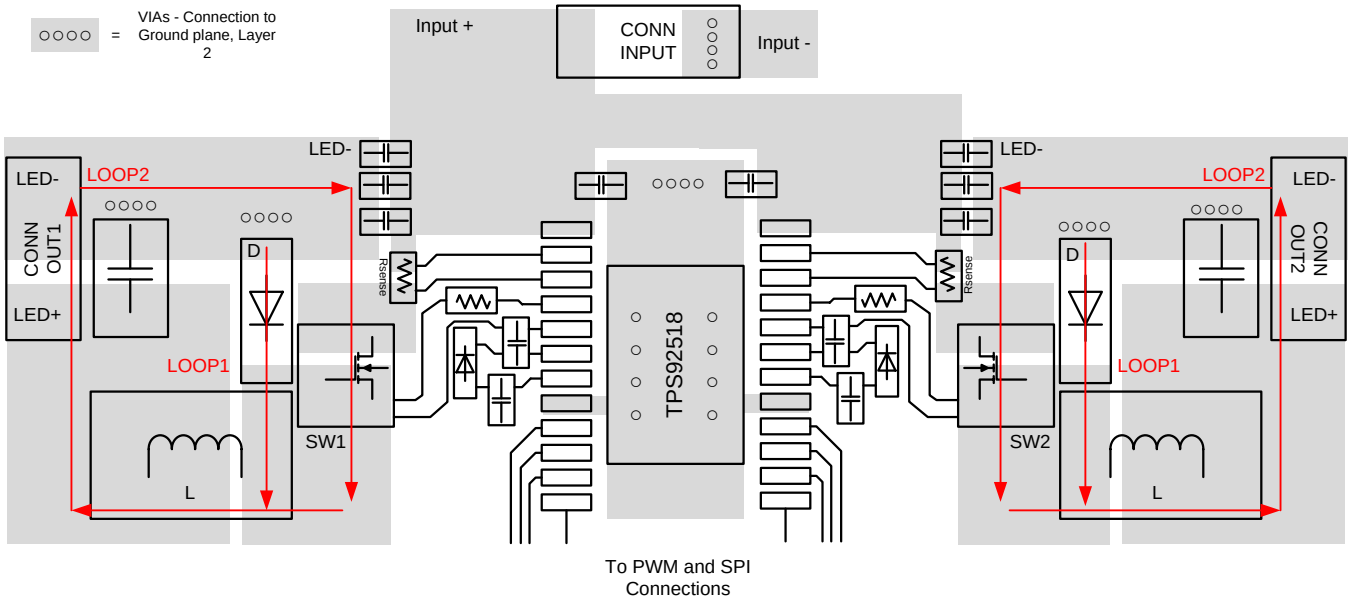


Figure 59. TPS92518-Q1 Layout Guideline

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

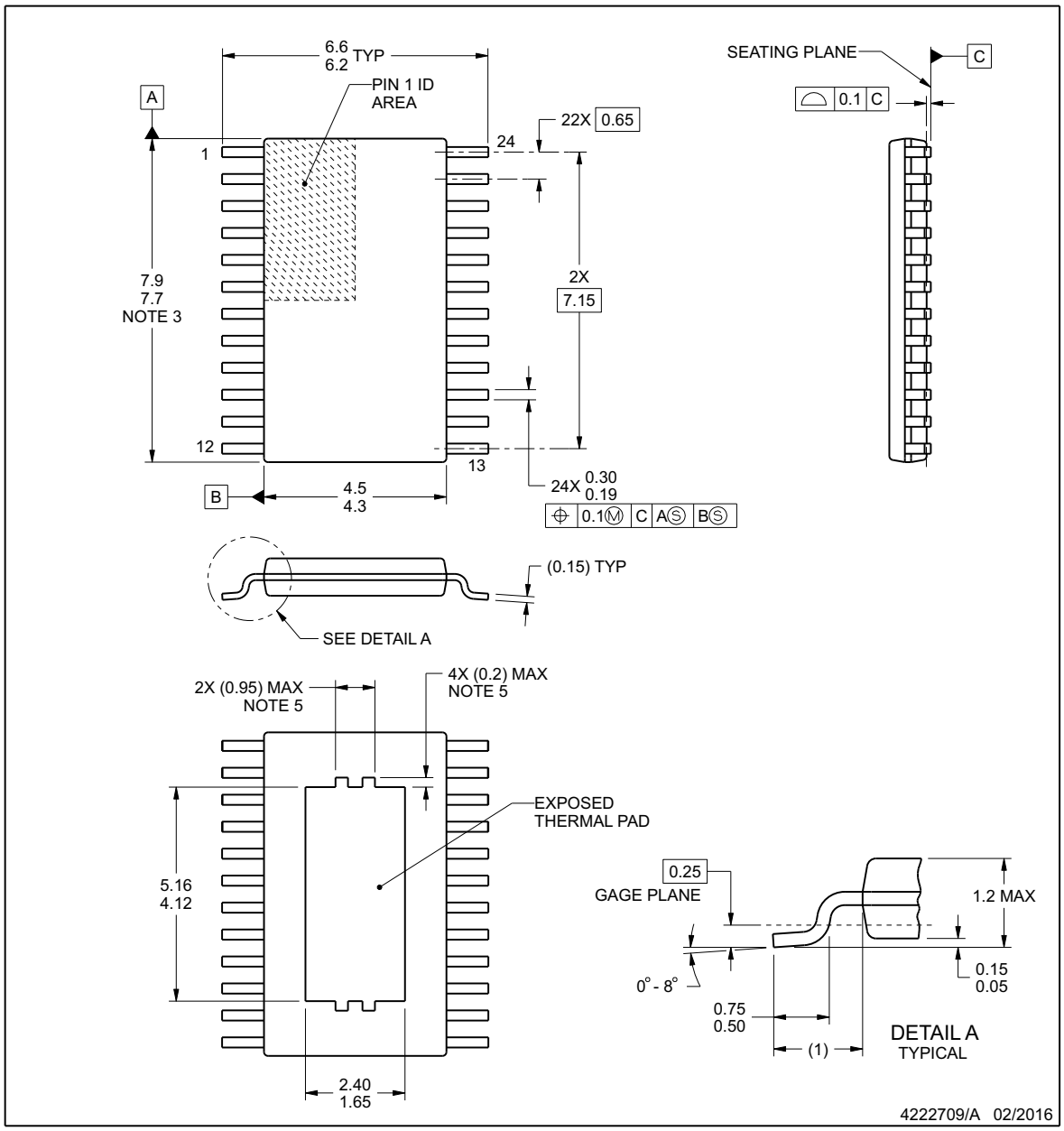
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

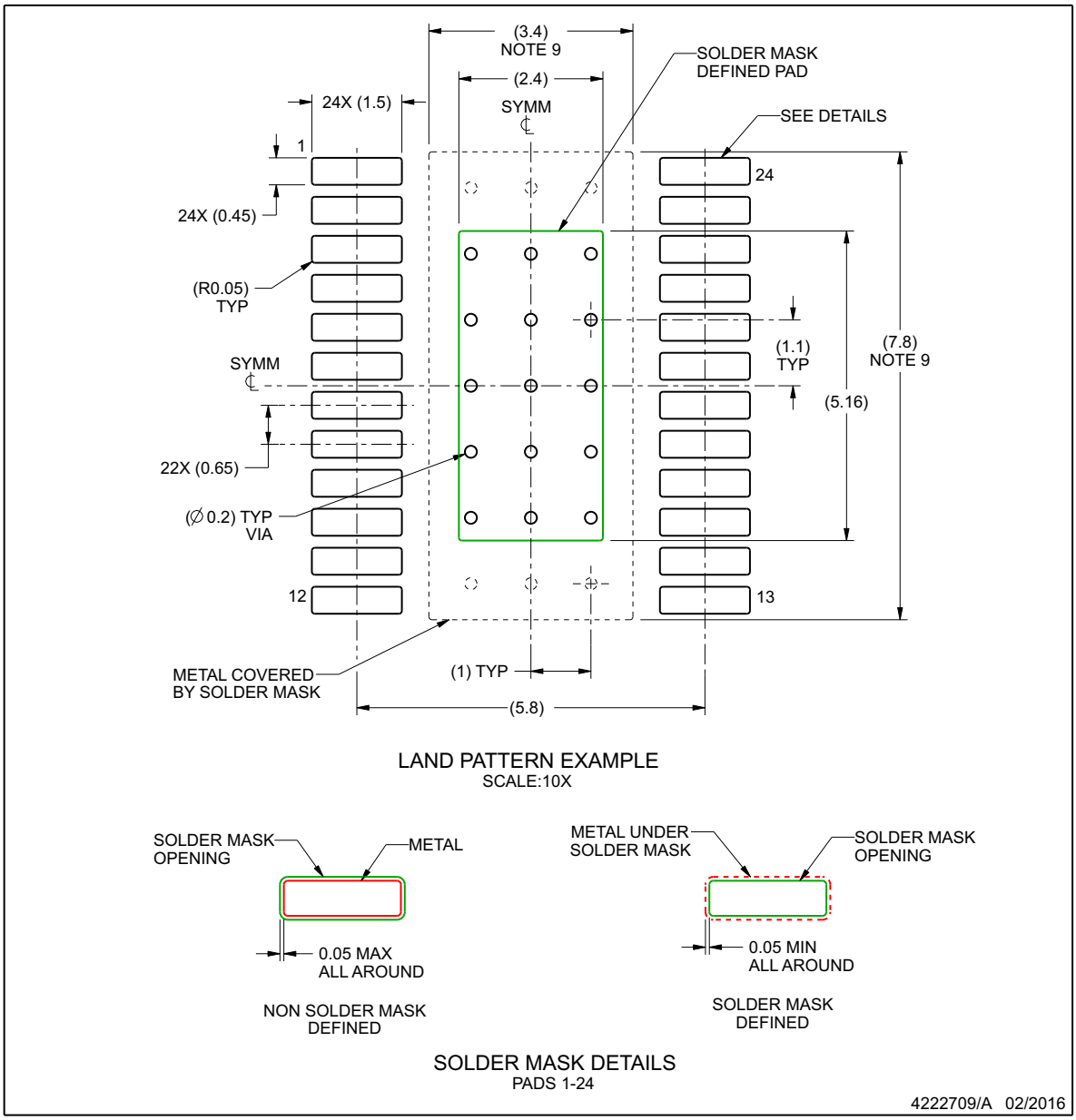
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.

EXAMPLE BOARD LAYOUT

PWP0024B — **PowerPAD™ TSSOP - 1.2 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

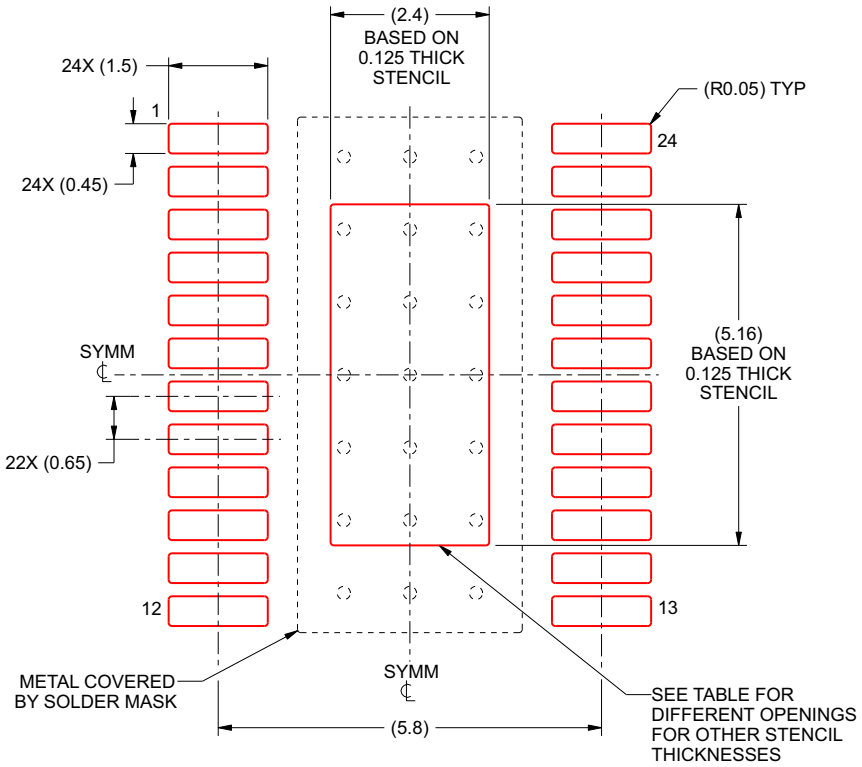
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PWP0024B

PowerPAD ™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92518HVQPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92518HVQ	Samples
TPS92518HVQPWPTQ1	ACTIVE	HTSSOP	PWP	24	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92518HVQ	Samples
TPS92518QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92518Q	Samples
TPS92518QPWPTQ1	ACTIVE	HTSSOP	PWP	24	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	92518Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS92518-Q1, TPS92518HV-Q1 :

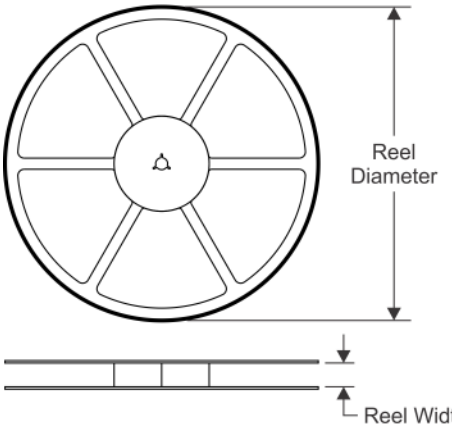
- Catalog: TPS92518, TPS92518HV

NOTE: Qualified Version Definitions:

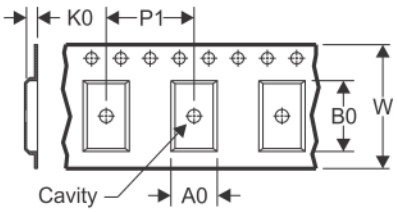
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

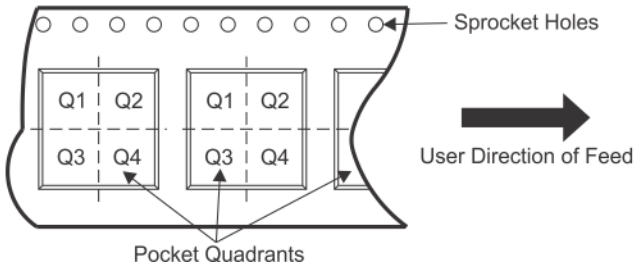


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

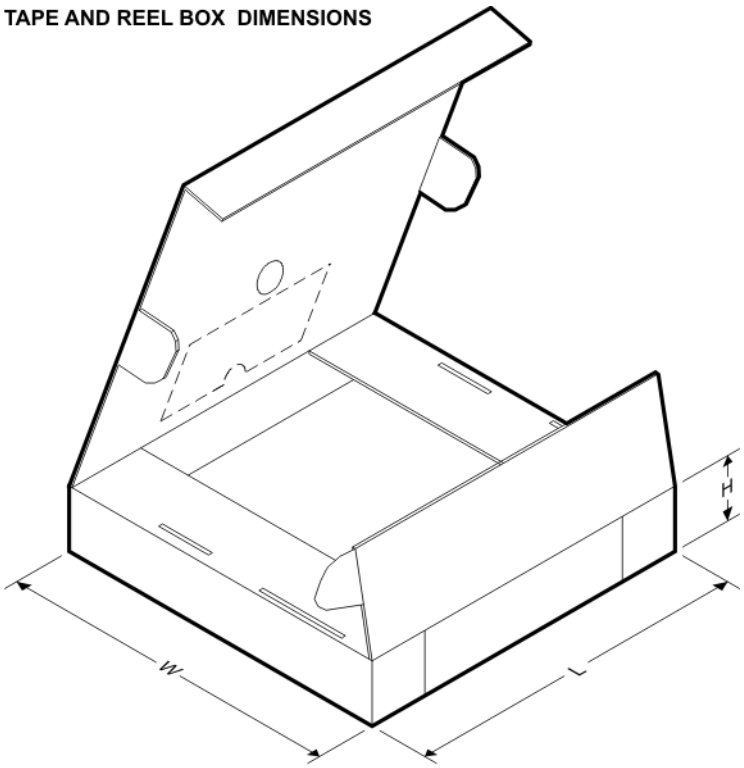
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92518HVQPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS92518QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92518HVQPWPRQ1	HTSSOP	PWP	24	2000	350.0	350.0	43.0
TPS92518QPWPRQ1	HTSSOP	PWP	24	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

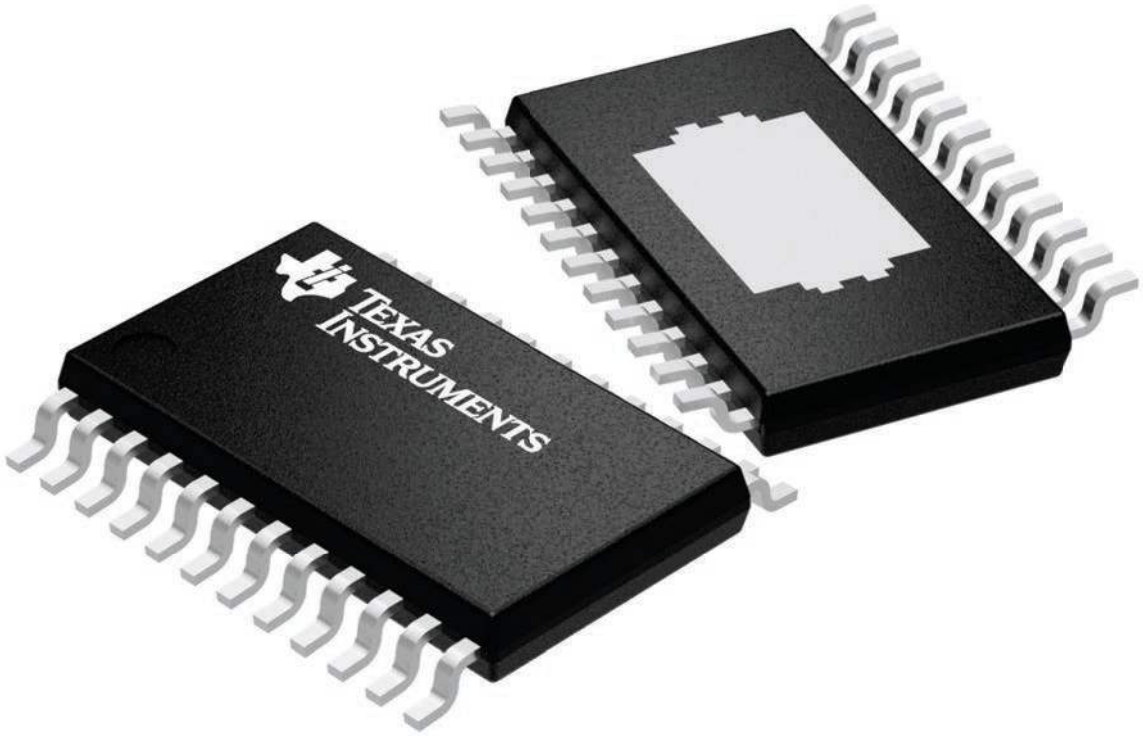
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



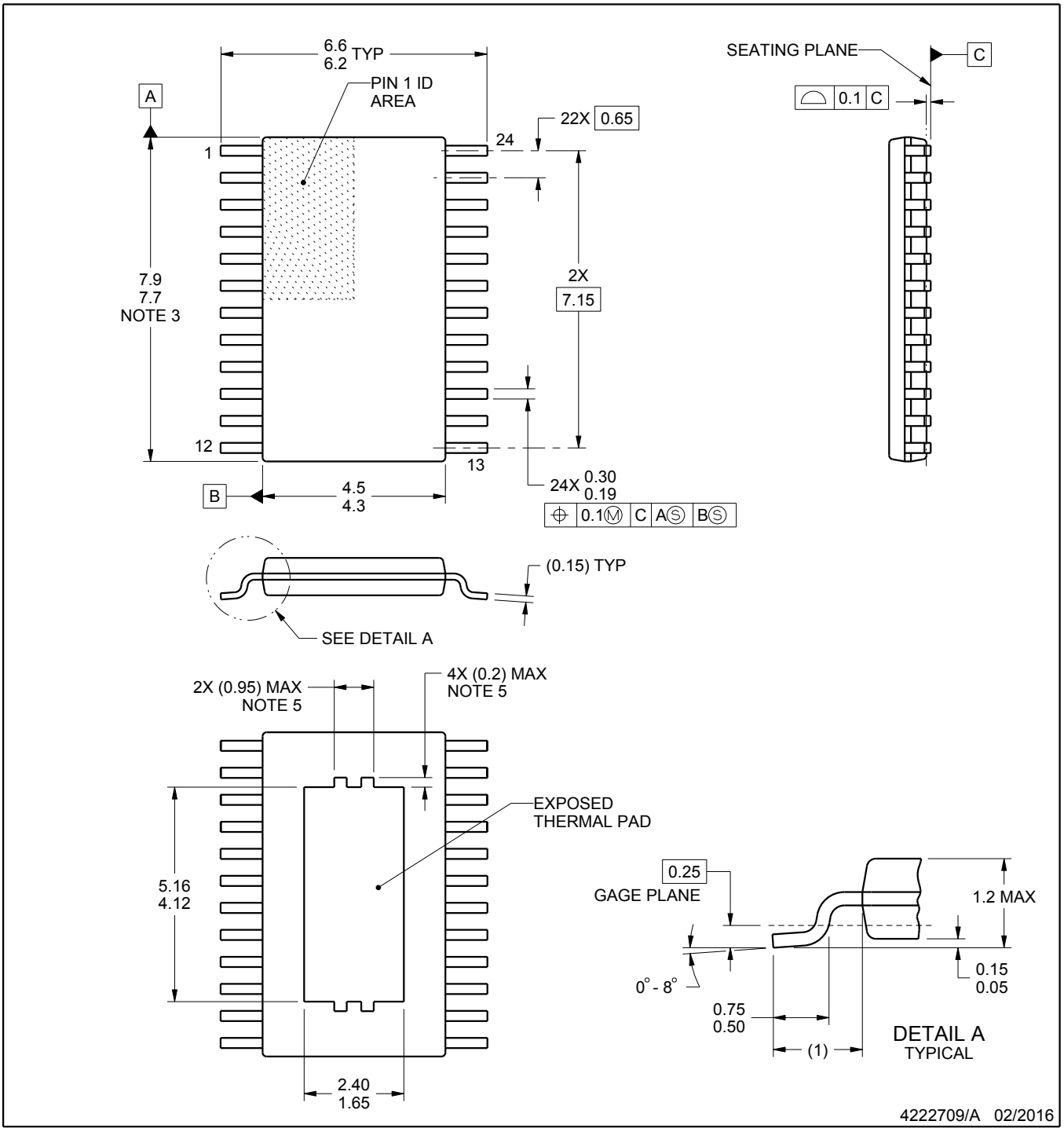
4224742/B

PACKAGE OUTLINE

PWP0024B

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

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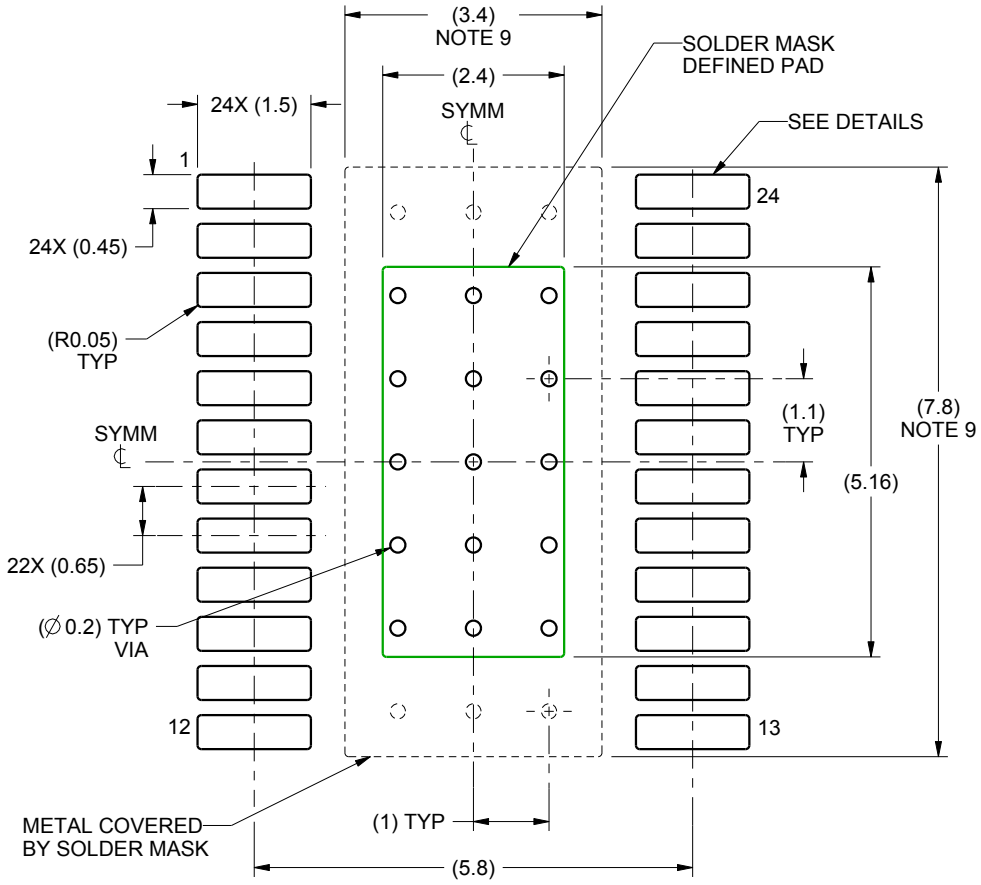
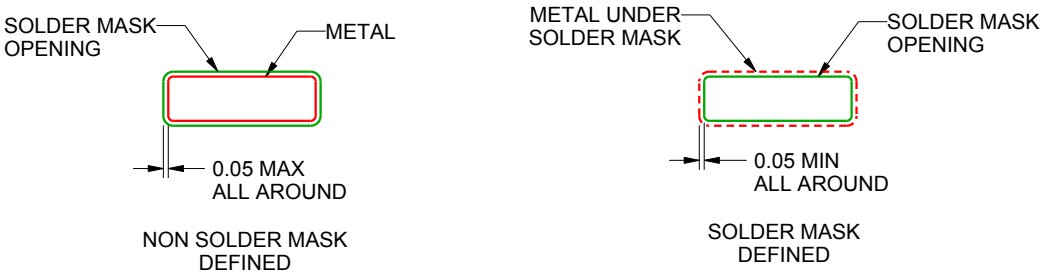
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may not be present and may vary.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
PADS 1-24

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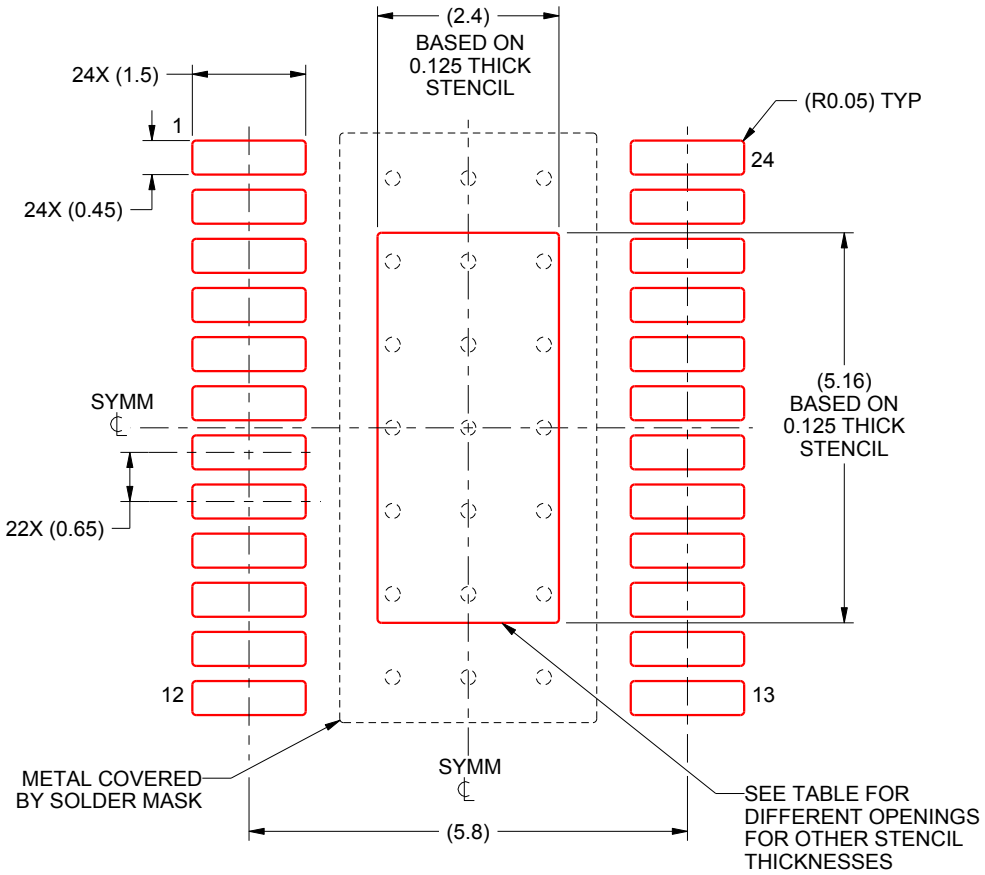
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.68 X 5.77
0.125	2.4 X 5.16 (SHOWN)
0.15	2.19 X 4.71
0.175	2.03 X 4.36

4222709/A 02/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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