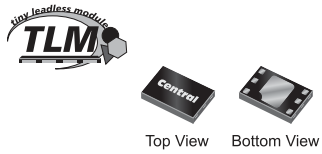
CTLSH1-40M621H

SURFACE MOUNT SILICON HIGH CURRENT, LOW V_F SCHOTTKY RECTIFIER



TLM621H CASE

• Device is ***Halogen Free*** by design

www.centralsemi.com

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLSH1-40M621H is a very low profile (0.4mm), low V_F Schottky rectifier in a small, thermally efficient, 1.5mm x 2mm Tiny Leadless Module (TLM) package.

MARKING CODE: CNE

APPLICATIONS:

- DC-DC Converters
- Reverse Battery Protection
- Battery powered devices including Cell Phones, PDAs, Digital Cameras, MP3 Players, etc.

FEATURES:

- High Current (I_F=1.0A)
- Low Forward Voltage Drop (V_F=0.55V MAX @ 1.0A)
- High Thermal Efficiency

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Peak Repetitive Reverse Voltage	V_{RRM}	40	V
Continuous Forward Current	I_F	1.0	A
Peak Repetitive Forward Current, tp≤1.0ms	I_{FRM}	3.5	A
Peak Forward Surge Current, tp=8.0ms	I_{FSM}	6.0	A
Power Dissipation (Note 1)	P_D	1.6	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance (Note 1)	Θ_{JA}	75	°C/W

ELECTRICAL CHARACTERISTICS: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_R	V_R=5.0V			10	μA
I_R	V_R=8.0V			20	μA
I_R	V_R=15V			50	μA
I_R	V_R=40V			0.2	mA
I_R	V_R=40V, T_A=100°C			20	mA
BV_R	I_R=100μA	40			V
V_F	I_F=10mA			0.30	V
V_F	I_F=100mA			0.40	V
V_F	I_F=500mA			0.50	V
V_F	I_F=1.0A			0.60	V
C_J	V_R=4.0V, f=1.0MHz		50		pF
t_{rr}	I_F=I_R=500mA, I_{rr}=50mA, R_L=50Ω		15		ns

Note 1: Mounted on a 4-layer JEDEC test board with one thermal via connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.

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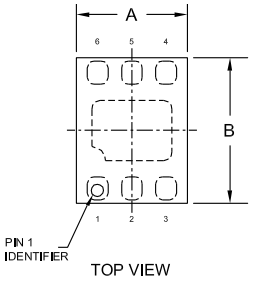
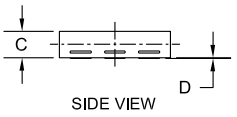
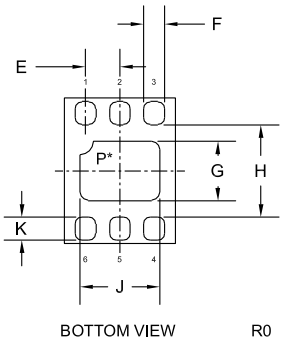
TLM621H CASE - MECHANICAL OUTLINE







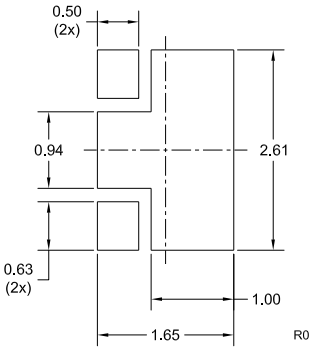
*Exposed pad P internally connected to pins 2, 3, 4, and 5.

DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.053	0.065	1.35	1.65
B	0.073	0.085	1.85	2.15
C	0.012	0.016	0.30	0.40
D	0.000	0.002	0.00	0.05
E	0.020		0.50	
F	0.008	0.012	0.20	0.30
G	0.027	0.035	0.69	0.89
H	0.053	0.057	1.35	1.45
J	0.039	0.047	0.99	1.19
K	0.011	0.015	0.28	0.38

TLM621H (REV:R0)

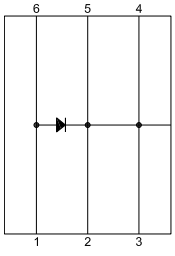
OPTIONAL MOUNTING PADS

(Dimensions in mm)



For standard mounting refer to TLM621H Package Details

PIN CONFIGURATION



LEAD CODE:

1) Anode
2) Cathode
3) Cathode
4) Cathode
5) Cathode
6) Anode

MARKING CODE: CNE

R5 (22-December 2015)

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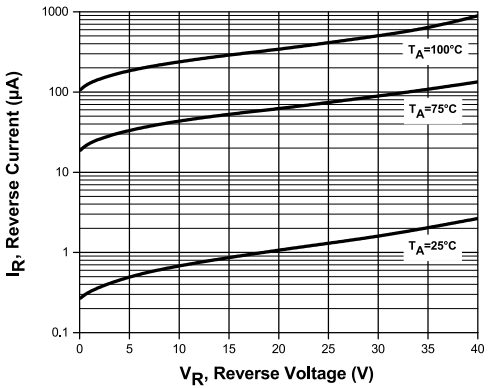
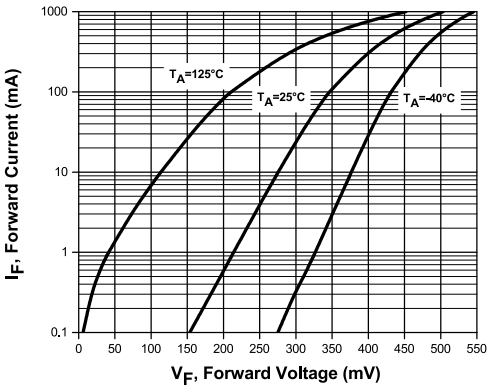
TYPICAL ELECTRICAL CHARACTERISTICS

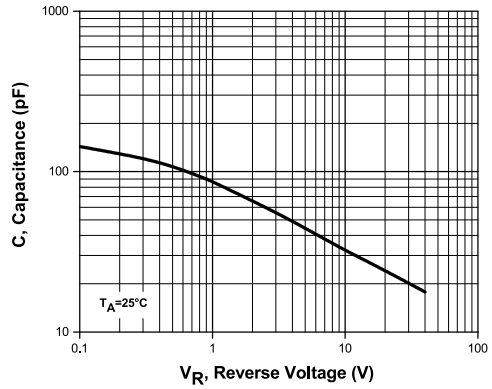
Leakage Current



Forward Voltage



Capacitance



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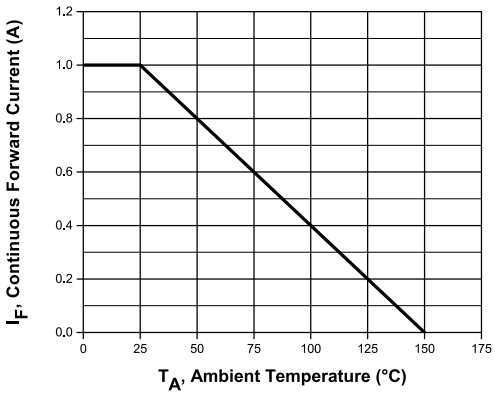
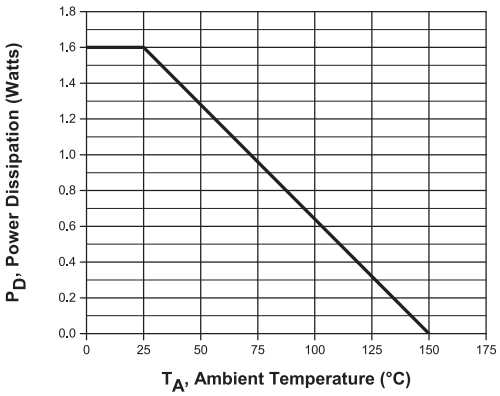
TYPICAL ELECTRICAL CHARACTERISTICS

Current Derating



Power Derating*



*Mounted on a 4-layer JEDEC test board with one thermal via connecting the exposed thermal pad to the first buried plane. PCB was constructed as per JEDEC standards JESD51-5 and JESD51-7.