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# FQP17N40

## N-Channel QFET® MOSFET

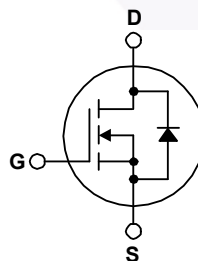
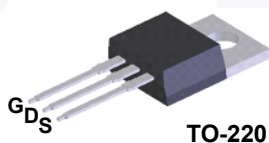
400 V, 16 A, 270 mΩ

### Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 16 A, 400 V,  $R_{DS(on)} = 270 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 8.0 \text{ A}$
- Low Gate Charge (Typ. 45 nC)
- Low Crss (Typ. 30 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP17N40	Unit
$V_{DSS}$	Drain-Source Voltage	400	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	16	A
		10.1	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	64	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1000	mJ
$I_{AR}$	Avalanche Current (Note 1)	16	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	17	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	170	W
		1.35	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQP17N40	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.74	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP17N40	FQP17N40	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	400	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.44	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 320\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.0\text{ A}$	--	0.21	0.27	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 8.0\text{ A}$	--	13	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1800	2300	pF
$C_{oss}$	Output Capacitance		--	270	350	pF
$C_{rss}$	Reverse Transfer Capacitance		--	30	40	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 200\text{ V}, I_D = 17.2\text{ A},$ $R_G = 25\ \Omega$	--	40	90	ns	
$t_r$	Turn-On Rise Time		--	185	380	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	90	190	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	105	220	ns
$Q_g$	Total Gate Charge	$V_{DS} = 320\text{ V}, I_D = 17.2\text{ A},$ $V_{GS} = 10\text{ V}$	--	45	60	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4)	--	11.4	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	21.7	--	nC

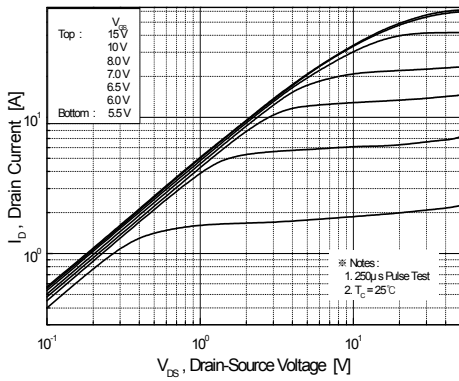
### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	16	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	64	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 16\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 17.2\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	290	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	2.5	--	$\mu\text{C}$

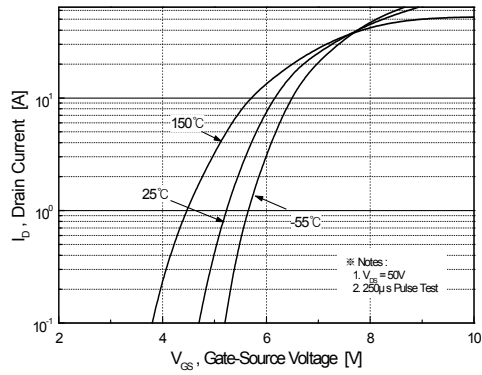
#### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2.  $L = 6.8\text{ mH}, I_{AS} = 16\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 17.2\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

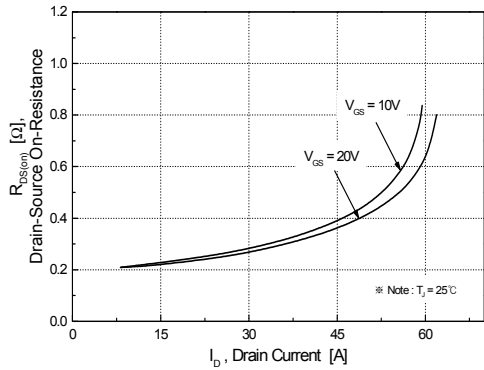
## Typical Characteristics



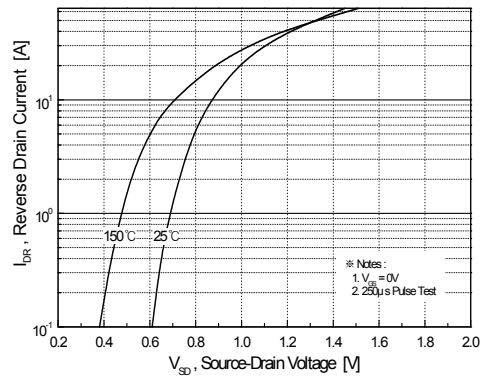
**Figure 1. On-Region Characteristics**



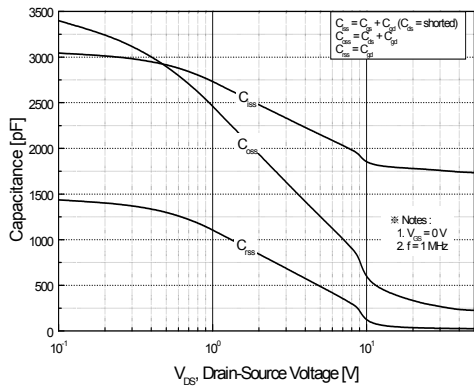
**Figure 2. Transfer Characteristics**



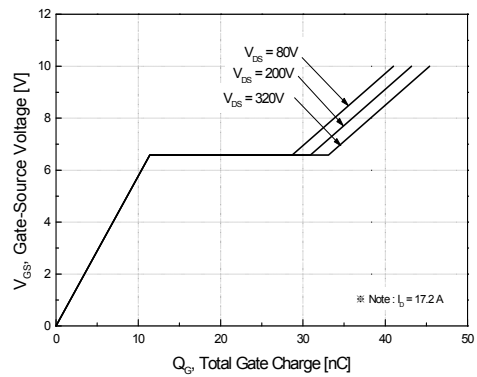
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

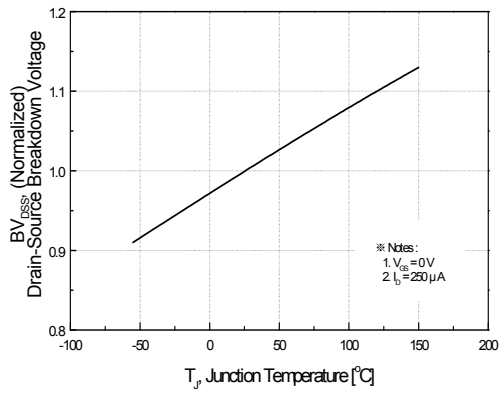


**Figure 5. Capacitance Characteristics**

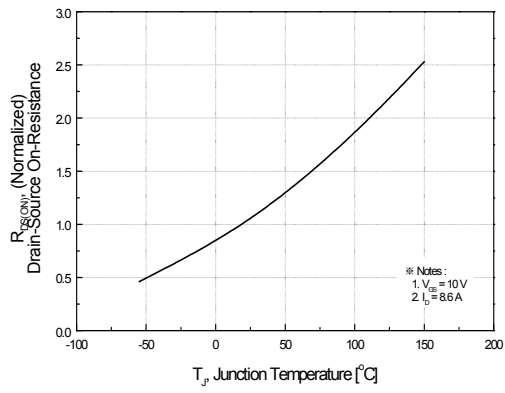


**Figure 6. Gate Charge Characteristics**

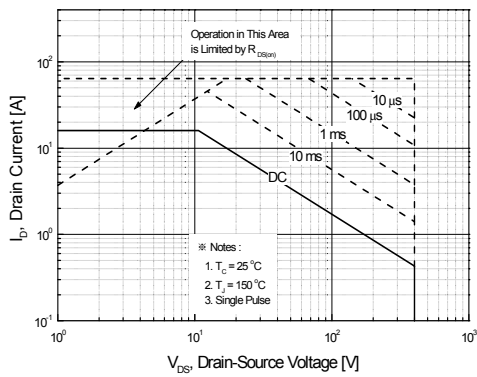
**Typical Characteristics** (continued)



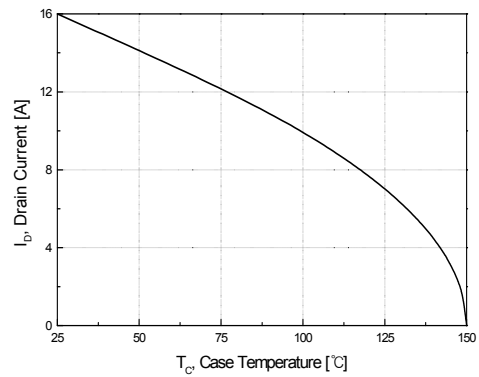
**Figure 7. Breakdown Voltage Variation vs. Temperature**



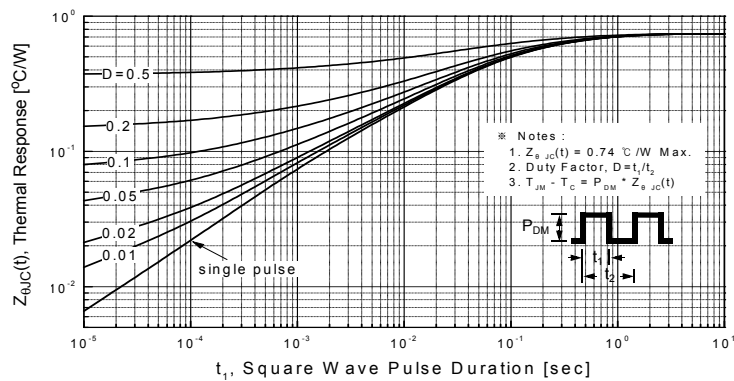
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

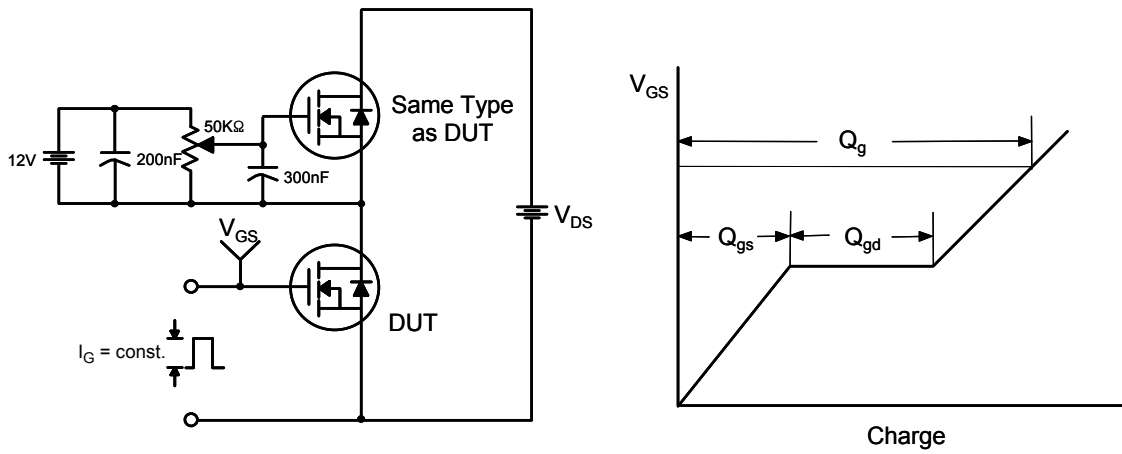


Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

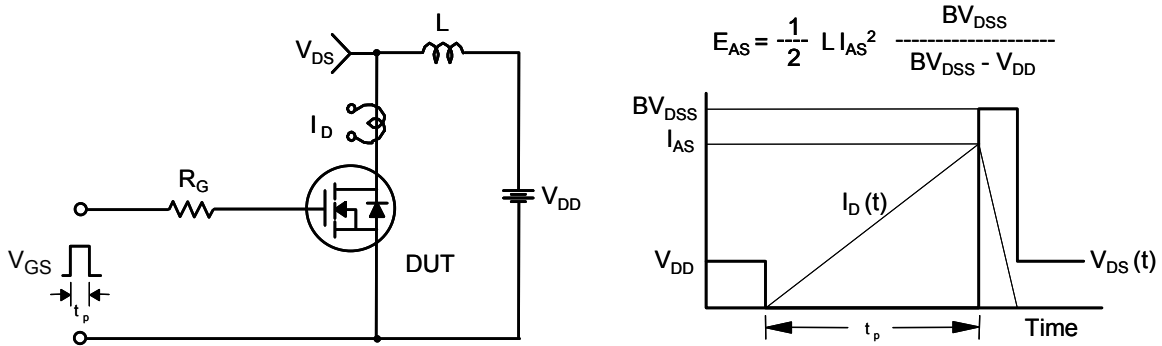


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

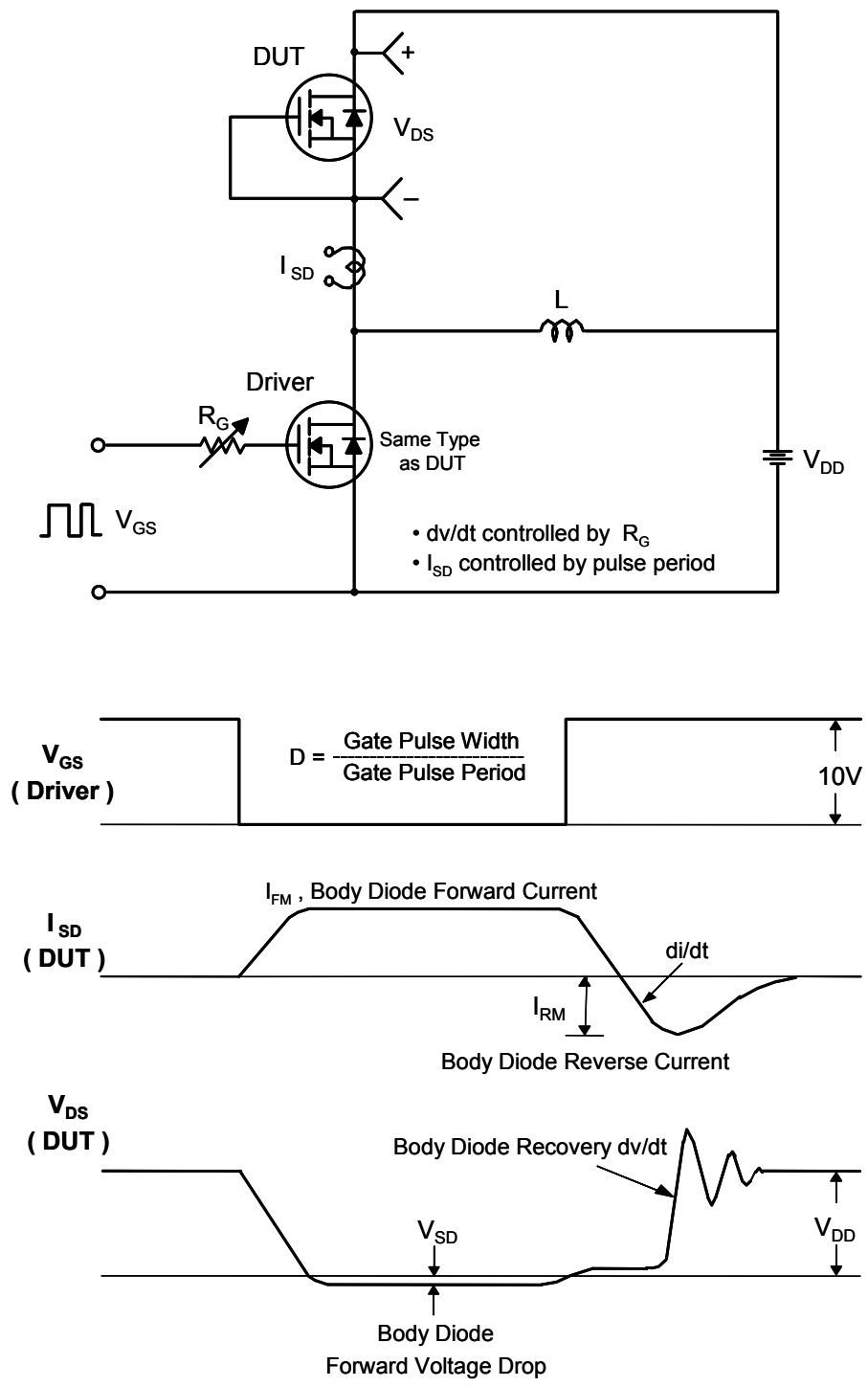
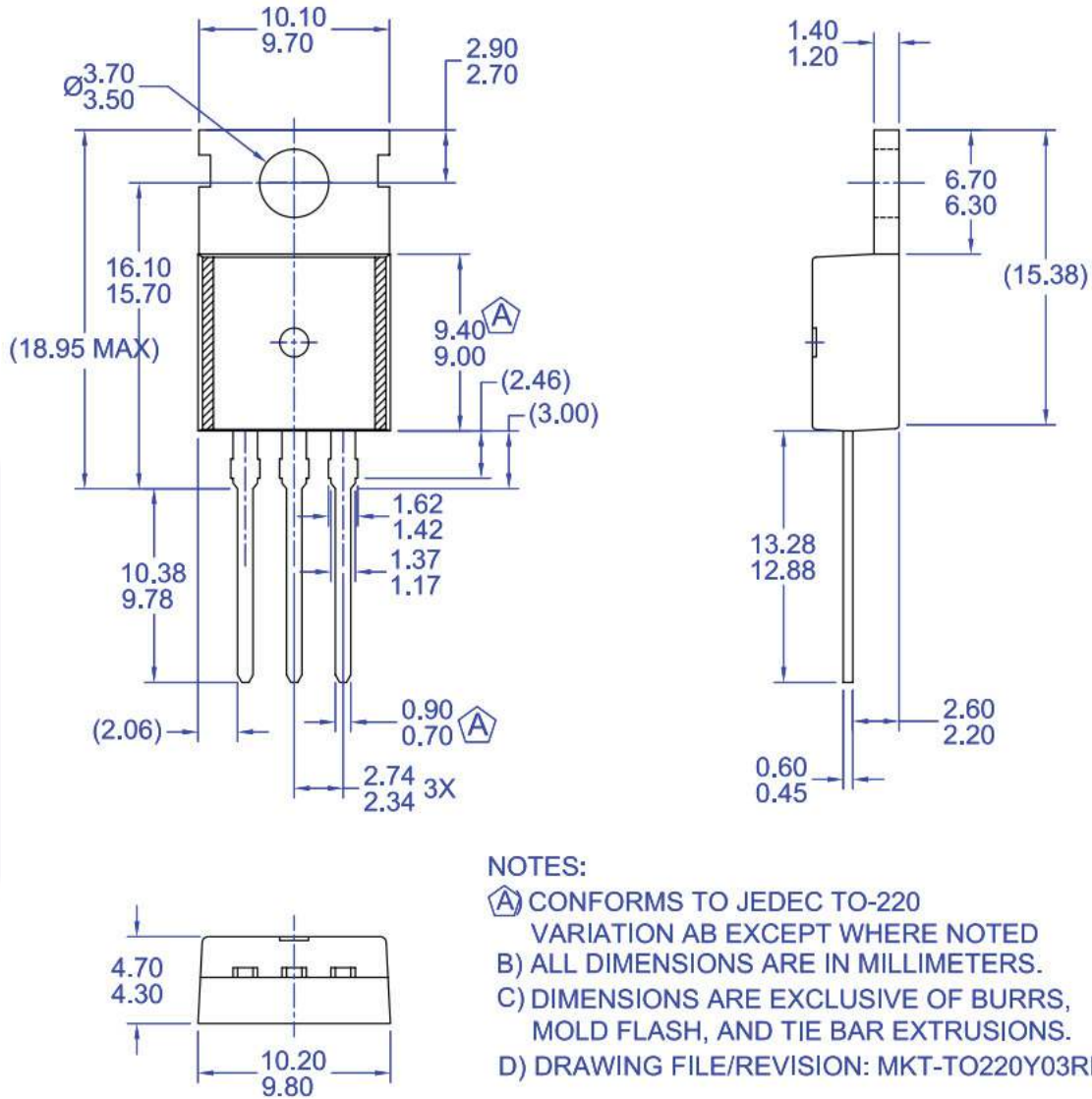


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB**

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