GS3481 Dual-Slew-Rate, Quad-Output Cable Driver with Pre-Emphasis

Key Features

- SMPTE ST424, SMPTE ST292 and SMPTE ST259 compliant
- Four positive single-ended coaxial-cable-driving outputs configured in pairs
  - selectable slew rates
  - adjustable output swing from 400mVpp to 2400mVpp
  - independent ENABLE controls for each output
- Programmable pre-emphasis for each output
  - pre-emphasis programmable to +9dB in 1dB increments
  - independent selection for each output
- Supports DVB-ASI at 270Mb/s
- Wide common-mode range input buffer:
  - 100mV sensitivity
  - supports DC-coupling to industry-standard differential logic
  - on-chip 100Ω differential data input termination
- The device may be pin configured or for more flexibility, a GSPI serial interface is provided. Status information can also be read from the device using the serial interface
- Input signal trace equalization
- Robust signal presence function
- Power supply operation: 123mW, four outputs, 800mV swing with no pre-emphasis or termination loading (2.5V supply)
- Excellent output eye quality
- Standard JEDEC logic control and status signal levels
- GSPI serial interface for advanced features and programmability
- Operating temperature range: -40°C to +85°C
- Small-footprint QFN package (4mm x 4mm)
  - new four-output pin out
- Pb-free and RoHS compliant

Applications

- SMPTE ST424, SMPTE ST292 and SMPTE ST259 coaxial cable serial digital interfaces

Description

The GS3481 is a high-speed BiCMOS integrated circuit designed to drive one to four 75Ω coaxial cables, and is Gennum's most advanced cable driver, offering a comprehensive feature set for today's most demanding applications.

The GS3481 can drive data rates from DC up to 2.97Gb/s, and provides two selectable slew rates in order to achieve compliance for SMPTE ST424, ST292 and ST259.

The device provides four single-ended positive outputs, which are suitable for driving polarity-dependant signals such as DVB-ASI in addition to polarity-independent signals such as SMPTE ST259, ST292 and ST424 SDI signals.

The GS3481 is the industry's only cable driver featuring output pre-emphasis. With up to 9dB (adjustable in 1dB increments) of output pre-emphasis, the GS3481 is ideal for use in long-reach applications where moving the SMPTE compliance point from the board connector to a point further downstream is required.

The GS3481 features the industry's largest output swing. Utilizing an external bias resistor, the single-ended output swing is adjustable from 400mVpp to 2400mVpp. High output swing can be utilized to compensate for losses that occur after the cable driver output.

The GS3481 accepts industry-standard differential input levels including LVPECL and CML.

Input trace equalization compensates for up to 10 inches of FR4 trace loss. This feature can be enabled or disabled using the GSPI host interface.

Each output can also be powered-down, leaving the serial data outputs in a high-impedance state.

A GSPI serial interface is provided for configuration and control. Status information can also be read from the device using the serial interface.

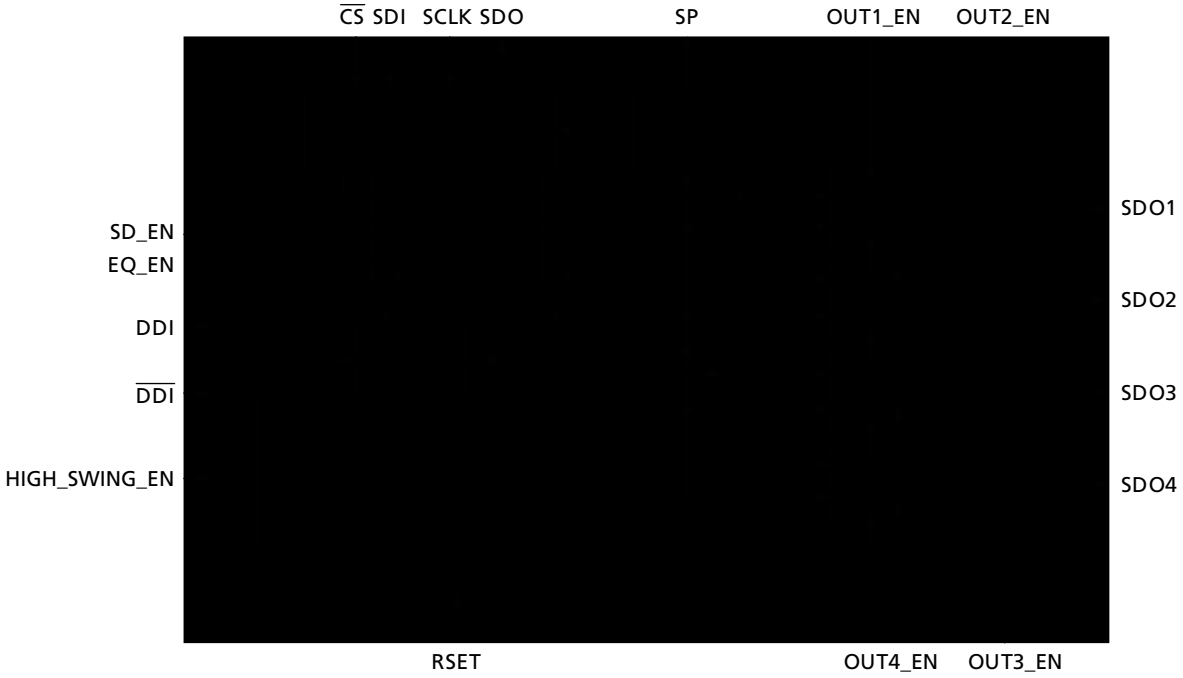
A signal presence function (pin SP) indicates whether an active signal is present at the output of the GS3481, which can be used to put the device in a low-power mode. The device typically draws 35mW when in this mode.

Independent output enabling for each of the four output signals provides very flexible configuration and control of the device.

The GS3481 can be powered from either a 3.3V or a 2.5V supply.

Power consumption is typically 123mW with four outputs enabled (no pre-emphasis or termination loading), using a 2.5V power supply.

The GS3481 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant. This component and all homogeneous subcomponents are RoHS compliant.



GS3481 Functional Block Diagram

Contents

1. Pin Out

1.1 Pin Assignment

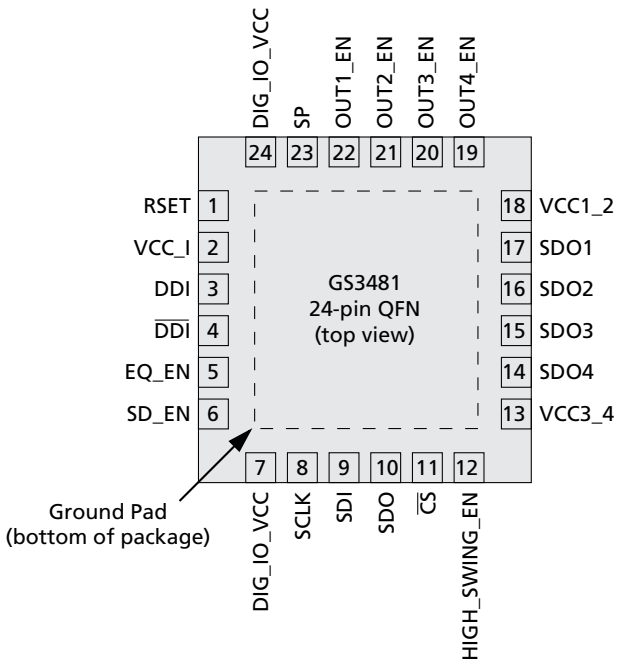


Figure 1-1: Pin Assignment

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
1	RSET	Input	External output amplitude control resistor connection.
2	VCC_I	Power	Most positive power supply for serial digital differential inputs and analog core. Connect to 3.3V or 2.5V.
3, 4	DDI, $\overline{DDI}$	Input	Serial Digital Differential Inputs.
5	EQ_EN	Input	Control signal input. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. When set LOW, trace equalization is turned OFF. When set HIGH, trace equalization is turned ON. **NOTE:** ***this pin must not be left floating.***

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
6	SD_EN	Input	Control signal input. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. When HIGH, the serial data outputs will meet the SMPTE ST 259 rise/fall time specification. When set LOW, the serial outputs will meet the SMPTE ST 292-1 and ST 424 rise/fall time specifications. **NOTE: *this pin must not be left floating.***
7, 24	DIG_IO_VCC	Power	Most positive power supply for control and status input and output signals. Connect to 3.3V, 2.5V or 1.8V.
8	SCLK	Input	GSPI host interface Clock signal input. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. Burst-mode clock for the GSPI serial host interface.
9	SDI	Input	GSPI host interface serial digital input signal. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. Digital data input for the GSPI host interface.
10	SDO	Output	GSPI host interface serial digital output signal. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. Digital data output for the GSPI host interface.
11	$\overline{CS}$	Input	GSPI host interface Chip Select (control signal input). Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. Active-low chip select for the GSPI host interface. When LOW, GSPI read or write operations are accepted by the device. When HIGH, GSPI read or write operations are ignored by the device.
12	HIGH_SWING _EN	Input	Control signal input. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. When set LOW, the SDO output swing (controlled by the RSET resistor) operates in the range 400mv ~ 1200mV. When set HIGH, the SDO output swing (controlled by the RSET resistor) operates in the range 1200mV to 2400mV). **NOTE: *this pin must not be left floating.***
13	VCC3_4	Power	Most positive power supply connection for output channels 3 and 4. Connect to 3.3V or 2.5V
14	SDO4	Output	Serial digital single-ended output 4.
15	SDO3	Output	Serial digital single-ended output 3.
16	SDO2	Output	Serial digital single-ended output 2.
17	SDO1	Output	Serial digital single-ended output 1.
18	VCC1_2	Power	Most positive power supply connection for output channels 1 and 2. Connect to 3.3V or 2.5V

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
19	OUT4_EN	Input	Control signal input. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. When set HIGH, the SDO4 pin will output a serial data signal. When set LOW, serial digital output 4 (SDO4) is set to high-impedance. **NOTE:** ***this pin must not be left floating***.
20	OUT3_EN	Input	Control signal input. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. When set HIGH, the SDO3 pin will output a serial data signal. When set LOW, serial digital output 3 (SDO3) is set to high-impedance. **NOTE:** ***this pin must not be left floating.***
21	OUT2_EN	Input	Control signal input. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. When set HIGH, the SDO2 pin will output a serial data signal. When set LOW, serial digital output 2 (SDO2) is set to high-impedance. **NOTE:** ***this pin must not be left floating.***
22	OUT1_EN	Input	Control signal input. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. When set HIGH, the SDO1 pin will output a serial data signal. When set LOW, serial digital output 1 (SDO1) is set to high-impedance. **NOTE:** ***this pin must not be left floating.***
23	SP	Output	Signal presence - status signal output. Signal levels are 3.3V, 2.5V and 1.8V LVCMOS/LVTTL compatible. Indicates the presence of a valid signal. When the SP pin is HIGH, a good input signal has been detected within the output stage driver. When LOW, the signal is invalid. This pin may be connected to the OUT[1:4]_EN pins to automatically power-down the device on loss of signal. **NOTE:** see **Section 4.5**.
–	Center Pad	Power	Connect to most negative power supply plane following the recommendations in Recommended PCB Footprint on page 33.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V_{DC} to 3.6V_{DC}
Input ESD Voltage	2kV
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V_{DC}
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

NOTE: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristic sections is not implied.

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage	V_{CC}	3.3V Typical	3.135	3.3	3.465	V	–
		2.5V Typical	2.375	2.5	2.625	V	–
Power Consumption (2.5V)	P_D	1 output enabled	–	115	143	mW	1
		2 outputs enabled	–	154	180	mW	1
		3 outputs enabled	–	192	218	mW	1
		4 outputs enabled	–	229	255	mW	1
		All outputs disabled	–	35	63	mW	1
		Power-down mode	–	–	21	mW	1
Power Consumption (3.3V)		1 output enabled	–	157	189	mW	1
		2 outputs enabled	–	206	238	mW	1
		3 outputs enabled	–	256	288	mW	1
		4 outputs enabled	–	306	337	mW	1
		All outputs disabled	–	50	83	mW	1
		Power-down mode	–	–	29	mW	1

Table 2-1: DC Electrical Characteristics (Continued)

V_{CC} = 3.3V ±5% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Current	I_S	1 output, V_{CC} = 2.5V	–	46	54.5	mA	1
		1 output, V_{CC} = 3.3V	–	47.5	55	mA	1
		2 outputs, V_{CC} = 2.5V	–	61.5	69	mA	1
		2 outputs, V_{CC} = 3.3V	–	62.5	69	mA	1
		3 outputs, V_{CC} = 2.5V	–	77	83.5	mA	1
		3 outputs, V_{CC} = 3.3V	–	77.5	83.5	mA	1
		4 outputs, V_{CC} = 2.5V	–	91.5	97.5	mA	1
		4 outputs, V_{CC} = 3.3V	–	93	97.5	mA	1
		No outputs, V_{CC} = 2.5V	–	14	24	mA	1
		No outputs, V_{CC} = 3.3V	–	15	24	mA	1
		Power-down mode, V_{CC} = 2.5V	–	–	8	mA	1
		Power-down mode, V_{CC} = 3.3V	–	–	8.1	mA	1
Output Voltage	V_{CMOUT}	Common mode	–	V_{TERM} - V_{OUT}	–	V	–
Input Voltage	V_{CMIN}	Common mode	1.4 + $\Delta V_{DDI}/2$	–	V_{CC} - $\Delta V_{DDI}/2$	V	–
SD_EN, EQ_EN Input	V_{IH}	I_{IH} <= 150µA	1.7	–	–	V	–
	V_{IL}	I_{IL} <= 150µA	–	–	0.8	V	–
OSP Drive Strength	–	–	2	–	–	mA	–

NOTES:

1. Power consumed in the GS3481 with no pre-emphasis and 800mVppd output swing.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5% or 2.5V ±5%; T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{SDO}	–	.27	–	2.97	Gb/s	1
Additive jitter	–	2.97Gb/s	–	10	–	ps_{p-p}	2
	–	1.485Gb/s	–	10	–	ps_{p-p}	2
	–	270Mb/s	–	30	–	ps_{p-p}	2
Rise/Fall time	t_r, t_f	SD_EN=0	–	–	135	ps	3
	t_r, t_f	SD_EN=1	400	–	800	ps	3
Mismatch in rise/fall time	$\triangle t_r$, $\triangle t_f$	HD/3G modes only	–	–	35	ps	–
Duty cycle distortion	–	SD_EN=0, 2.97Gb/s	–	10	–	ps	4, 5
	–	SD_EN=0, 1.485Gb/s	–	14	–	ps	4, 5
	–	SD_EN=1	–	35	–	ps	4, 5
Overshoot	–	SD_EN=0,	–	–	10	%	4
Output Return Loss	ORL	5MHz – 1.485GHz	17	19	–	dB	6
		1.485GHz – 2.97GHz	–	11	–	dB	6
Output Voltage Swing	V_{OUT}	R_{SET} = 750Ω	750	800	850	mV_{p-p}	4
Input Voltage Swing	$\triangle V_{DDI}$	Guaranteed functional.	100	–	250	mV_{p-pd}	–
		Guaranteed to meet all published specifications.	250		2200	mV_{p-pd}	–
Output Enable Delay	–	–	–	–	100	ns	–
Output Disable Delay	–	–	–	–	80	ns	–

NOTES:

1. The input coupling capacitor must be set accordingly for lower data rates.
2. Turning on input trace equalization will reduce jitter in most applications.
3. Rise/Fall time measured between 20% and 80% applies to 800mV output swing only.
4. Single-ended into a 75Ω external load.
5. Calculated as the actual positive bit-width compared to the expected positive bit-width using a 1010 pattern.
6. ORL depends on board design. The GS3481 achieves this specification on Gennum's evaluation boards.

3. Input/Output Circuits

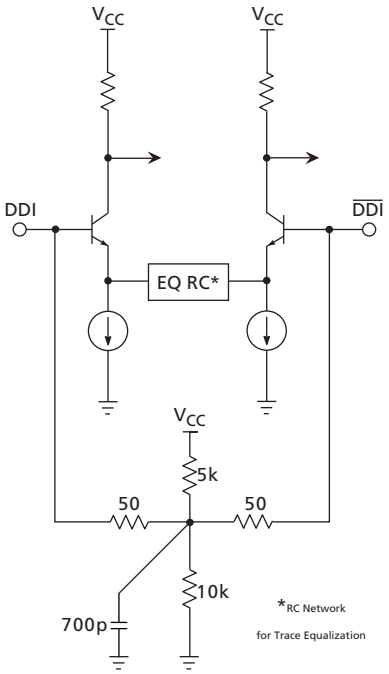


Figure 3-1: Differential Input Stage (DDI, $\overline{DDI}$)

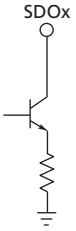


Figure 3-2: Single-Ended Output Stage (SDO[1:4])

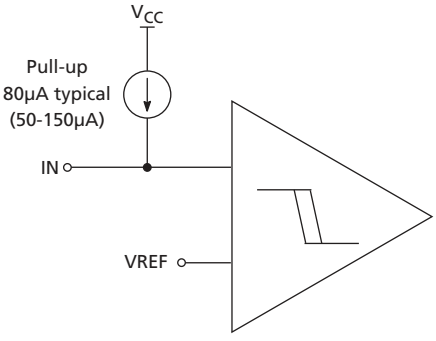


Figure 3-3: Control Input (HIGH_SWING_ENABLE, EQ_EN, SD_EN, OUT[1:4]_EN)

4. Detailed Description

4.1 Serial Data Input

The GS3481 features a differential input buffer with on-chip 100Ω differential termination.

The serial data input signal is connected to the DDI and $\overline{\text{DDI}}$ input pins of the device.

Input signals can be single-ended or differential, DC or AC-coupled.

The serial data input buffer is capable of operation with any binary coded signal that meets the input signal level requirements, in the range of DC to at least 2.97Gb/s.

The input circuit is self-biasing to allow for simple AC or DC-coupling of input signals to the device.

4.2 Input Trace Equalization

The GS3481 features fixed trace-equalization to compensate for PCB trace dielectric losses.

NOTE: This feature is not available in SD mode, and therefore trace-equalization must be disabled when operating in this mode.

The trace-equalization has two settings, OFF (0) and ON (1). ON invokes a typical 3dB gain value at 1.5GHz. This value is optimized for compensating the high-frequency losses associated with approximately 10 inches of 5-mil stripline in FR4 material.

Table 4-1: Input Trace-Equalization

EQ_EN	Function
0	Trace Equalization OFF
1	Typical 3dB Trace Equalization

4.3 Serial Data Output

The GS3481 features quad current-mode single-ended output drivers capable of driving up to 2400mVpp single-ended into a 1m length of 75Ω cable terminated at both ends.

The output signal amplitude or swing is user configurable using an external RSET resistor.

The SDO[1:4] pins of the device provide the serial data outputs.

4.3.1 Slew Rate Selection (Rise/Fall Time Requirement)

The GS3481 supports two user-selectable output slew rates.

Control of the slew rate is determined by the setting of the SD_EN input pin.

Table 4-2: Slew Rate Selection

SD_EN	Rise/Fall Time
0	SMPTE 424M & 292M compliant
1	SMPTE 259M compliant

4.4 Output Enable

The GS3481 supports an output enable function for each serial data single-ended output.

Control of this function is determined by the setting of the OUT[1:4]_EN control pins.

When asserted HIGH, the SDO[1:4] output drivers are functional. When asserted LOW, the SDO[1:4] output drivers are powered-down.

Table 4-3: Output Enable

OUT1_EN	SDO1	OUT2_EN	SDO2	OUT3_EN	SDO3	OUT4_EN	SDO4
0	Powered-down	0	Powered-down	0	Powered-down	0	Powered-down
1	Operational	1	Operational	1	Operational	1	Operational

When all of the output enables are driven LOW simultaneously, the device is placed in a low-power mode.

4.5 Signal Presence Indicator (SP)

The GS3481 supports a signal presence indicator function.

The signal presence pin (SP) is an active-high output that indicates when a valid output signal has been detected at the pre-driver output.

The signal presence function measures signal-edge energy to indicate that the pre-driver to the serial data outputs is toggling.

Table 4-4: Signal Presence Indicator

Pre-Driver Output	SP Pin
Valid signal present	1
No valid signal present	0

NOTE: The signal presence indicator will not function at data rates below ~25Mb/s.

4.6 Output Amplitude (RSET)

The output signal amplitude (or swing) of all four outputs is user-configurable using a single external RSET resistor.

It is possible to adjust the serial digital output signal amplitude from the nominal value defined by the 750Ω RSET resistor value, in the range 400mVpp to at least 2400mVpp, by increasing or decreasing the RSET resistor value accordingly.

One of two output swing ranges can be selected: HIGH SWING range and LOW SWING range. Selection of the output swing range can be achieved by either pin configuration or by host interface configuration.

By default, pin selection of the output swing range is selected.

When operating in the LOW SWING range, the RSET resistor controls the output swing in the range of 400mV to 1200mV.

When operating in the HIGH SWING range, the RSET resistor controls the output swing in the range of 1200mV to at least 2400mV, as defined in Section 4.3.

NOTE: Care should be taken when considering layout of the RSET resistor. Please refer to Section 5.1 for more details.

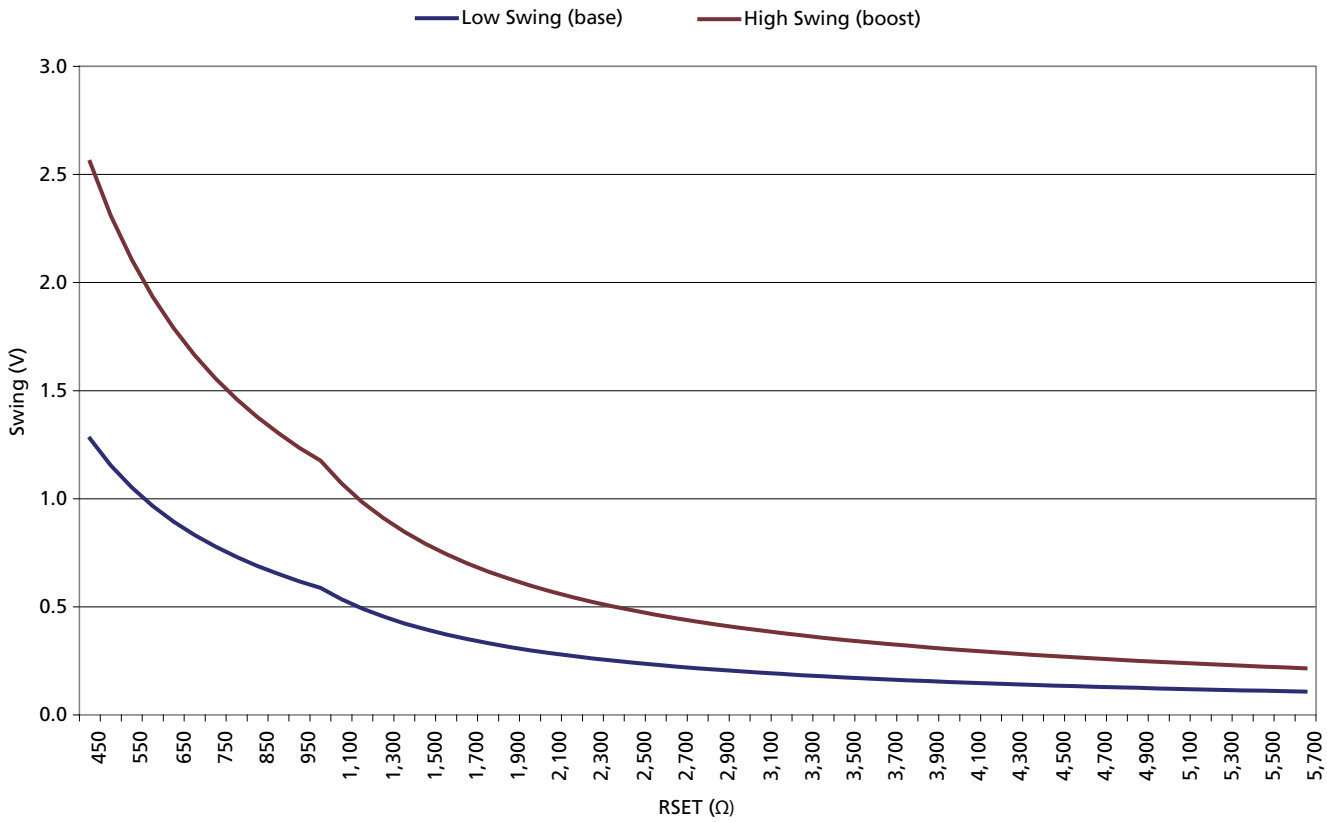


Figure 4-1: V_{OUT} vs. RSET

In order to determine the best starting value for RSET, the following formula should be used:

Rset = 8*(Rtrm/VoutppSE)

Where ***VoutppSE*** is in Volts, and both resistances are in Ω.

Rtrm is the value of the termination resistors, which should be equal to the characteristic impedance of the cable, and is typically 75Ω.

The cable must be short (≤1m), and terminated at both ends for the formula to be valid.

Example: For a 75Ω cable, Rtrm = 75Ω (at both ends), VoutppSE = 800mV

Rset = 8*(75/0.8) = 750Ω

This formula is not valid for long, unterminated, or improperly terminated cables.

This formula should be considered as a starting point, and actual swing values may vary based on layout. Also, for large output swings (>1040mV), smaller RSET values may be required in order to achieve the desired output swing level at HD and 3G data rates.

Table 4-5: Typical RSET Values

RSET (Ω)	Base Output Swing (mV)	Boost Output Swing (mV)
375	1200	2400
750	800	1600
1500	400	800

***NOTE:** In order to generate output swings greater than 1040mV, VCC_TERM must be connected to a 3.3V supply.

4.7 Host Interface

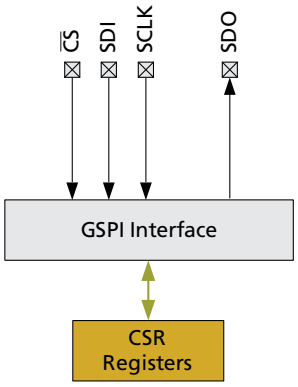


Figure 4-2: GSPI Interface Functional Block Diagram

All communication between the GS3481 and the application host processor takes place using the Gennum Serial Peripheral Interface (GSPI).

It is possible to configure all applicable functional blocks of the GS3481 using the GSPI interface.

It is possible to read the operational status of all applicable functional blocks of the GS3481 using the GSPI interface.

It is possible to implement single word read and write operations using the GSPI interface.

The GSPI interface also provides an “auto-increment” feature, which allows multiple sequential read or write operations to take place between the application host processor and the GS3481.

Multiple GS3481 devices can be connected in a daisy-chain configuration, which is backwards and forwards compatible with other GSPI enabled devices, allowing a single connection between the application host processor and a virtually unlimited number of GSPI enabled devices.

For backwards compatibility with existing GSPI enabled devices such as serializers (GS2972), deserializers (GS2971), timing products (GS4911), and the GX32xx crosspoint etc, a non-clocked “loop-through” mode of operation is provided. In this configuration, The SDO pin is a non-clocked loop-through of the SDI pin, and may be connected to the SDI pin of another device, allowing multiple devices to be connected to the GSPI chain. Any data transitions detected on the SDI pin are passed to the SDO pin, regardless of the setting of the $\overline{CS}$ pin.

For backwards compatibility with the GS2985 reclocker, a “bus-through” mode of operation is provided. In this configuration, The SDO pin will be high-impedance whenever the $\overline{CS}$ pin is HIGH, allowing the output of the GS3481 to be wire-or'd with the SDO pin of multiple GS2985 devices connected in daisy-chain mode. It should be noted however that the GS2985 daisy-chain and the GS3481 daisy-chain must be operated from separate chip selects.

In addition, the GS3481 features a “unit address” function, allowing up to 32 devices to be connected on a single chip select with each device being assigned a unique address to differentiate configuration and monitoring of connected devices.

The GS3481 host interface also features a “broadcast all” addressing mode and auto-increment addressing for both read and write operations.

The GS3481 may, therefore, be connected to the application host processor in a number of different point-to-point or bus interface structures, as shown in Figure 4-3.

It should be noted that the physical interface to the application host processor may be via GPIO pins on an embedded microprocessor system or sub system. It may also be via an FPGA device or through other discrete logic implementations.

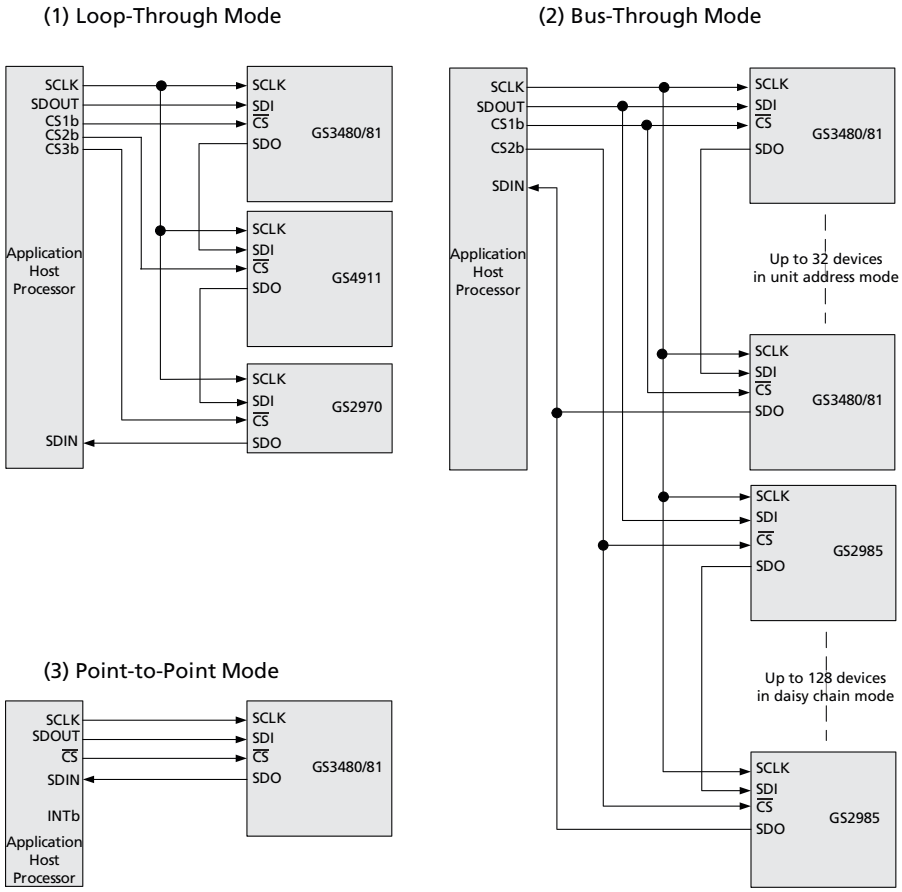


Figure 4-3: GSPI Connections to Application Host Processor

4.7.1 Gennum Serial Peripheral Interface (GSPI)

The Gennum Serial Peripheral Interface (GSPI), comprises a serial data input signal (SDI pin), serial data output signal (SDO pin), an active-low chip select ($\overline{CS}$ pin), and a burst clock (SCLK pin).

The SCLK, SDI, and $\overline{CS}$ signals are provided by the application interface.

All read or write access to the device is initiated and terminated by the application host processor and direct address accesses using the GSPI interface require the following process steps:

1. A 16-bit command/address word is written to the device.
2. One or more 16-bit data read or write operations are performed.

4.7.1.1 $\overline{CS}$ Pin

The Chip Select pin ($\overline{CS}$) is an active-low signal provided by the host controller to the GS3481.

The high-to-low transition of this pin marks the start of serial communication to the GS3481.

The low-to-high transition of this pin marks the end of serial communication to the GS3481.

In loop-though configuration mode or in point-to-point configuration mode, each device is provided with a separate unique chip select signal from the host controller.

In bus-through (unit address) mode, up to 32 devices may be connected on a single chip select.

Only those devices whose unit address matches the unit address in the GSPI command word respond to serial data provided by the host controller.

4.7.1.2 SDI Pin

The SDI pin is the serial digital input pin of the GS3481.

16-bit command and data words from the host controller or from the SDO pin of other devices connected in loop-though or bus-through configuration, are shifted into the device on the rising edge of SCLK when the $\overline{CS}$ pin is low.

4.7.1.3 SDO Pin

The SDO pin is the serial digital output of the GS3481.

All data transfers from the GS3481 to the host controller or to the SDI pin of other connected devices in loop-though or bus-through configuration, occur on this pin.

By default at power up or after system reset, the SDO pin provides a non-clocked loop-through of the SDI pin, allowing multiple devices to be connected in loop-through configuration. Data present on the SDI pin passes to the SDO pin regardless of the setting of the $\overline{CS}$ pin.

For read access in loop-through mode, the SDO pin is used to output the data read from the internal CSR when $\overline{CS}$ is LOW. Data is shifted out of the device on the falling edge of SCLK.

It is possible to enable/disable the loop-through connection by configuration of internal CSR register bits. When disabled, any data appearing at the SDI pin will not appear at the SDO pin and the SDO pin is HIGH when the loop-through mode is disabled. Disabling

the loop-through connection is required when configuring the unit address for up to 32 connected devices.

The time to enable/disable the loop-through connection from assertion of the register bit is less than the inter command delay as defined by the parameter t_{cmd} (2 SCLK cycles).

This is shown in Figure 4-4 below.

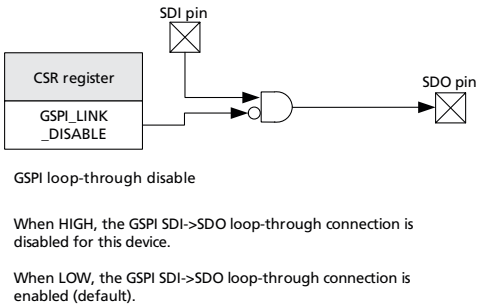


Figure 4-4: Loop-through Mode Disable

It is also possible to disconnect the loop-though connection and force the SDO pin to go high-impedance by configuration of internal CSR register bits (bus-through mode).

When configured for bus-through mode, the SDO pin will be high-impedance when the $\overline{CS}$ pin is HIGH.

When the $\overline{CS}$ pin is LOW, the SDO pin will follow the SDI pin for all command words and all data words in write operations.

The SDO pin will output data from internal CSR registers for all read operations.

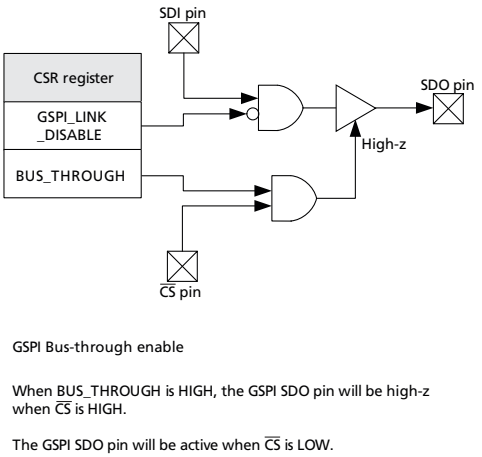


Figure 4-5: Bus-through Configuration Enable

4.7.1.4 SCLK Pin

The SCLK pin is the serial data shift clock input to the device provided by the host controller.

Serial data is clocked into the device SDI pin on the rising edge of SCLK.

Serial data is clocked out of the device on the SDO pin on the falling edge of SCLK (read operation).

The maximum interface clock rate is 75MHz.

4.7.2 Command Word Description

All GSPI accesses are a minimum of 16 bits in length and the start of each access is indicated by the high-to-low transition of the chip select ($\overline{CS}$) pin of the GS3481.

The format of the command word and data words are shown in Figure 4-6.

A high-to-low transition on the device chip select pin signifies the start of a new GSPI host interface access. Data received immediately following this high-to-low transition will be interpreted as a new command word.

4.7.2.1 R/W bit - B15 Command Word

This bit indicates a read or write operation.

When HIGH, a read operation is in progress and data is read from the register specified by the ADDRESS field of the command word.

When this bit is LOW, a write operation is in progress and data is written to the register specified by the ADDRESS field of the command word.

4.7.2.2 B'CAST ALL - B14 Command Word

This bit is used in write operations to configure all devices connected in loop-through and bus-through configuration with a single command.

When HIGH, the data word is written to the register specified by the ADDRESS field of the command word, regardless of the setting of the UNIT ADDRESS field of the command word. All connected devices write the data word to the specified ADDRESS.

When this bit is LOW, a normal write operation is in progress, and only those devices that have a unit address that matches the UNIT ADDRESS field of the command word write the data to the specific register specified by the ADDRESS field of the command word.

4.7.2.3 EMEM - B13 Command Word

When HIGH, the extended address mode is enabled such that the data word following the command word provides an additional 16 bits of address (address space = 23 bits).

When LOW, address space is defined from the ADDRESS field of the command word (address space = 7 bits).

4.7.2.4 AUTOINC - B12 Command Word

When HIGH, auto-increment read or write access is required.

In auto increment mode, the device automatically increments the register address for each contiguous read or write accesses, starting from the base address defined in the ADDRESS field of the command word.

The internal address is incremented for each 16-bit read or write access until a low-to-high transition on the $\overline{CS}$ pin is detected.

When LOW, single read or write access is required.

4.7.2.5 UNIT ADDRESS - B11:B7 Command Word

The 5 bits of the UNIT ADDRESS field of the command word are used to select one of 32 devices connected on a single chip select in loop-through or bus-through mode.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed unit address of the device.

By default, all devices have a unit address of 0h.

4.7.2.6 ADDRESS - B6:B0 Command Word

The 7 bits of the ADDRESS FIELD are used to select one of 128 specific register addresses in the device in single read or write access mode, or to set the base address for read or write accesses in auto increment mode.

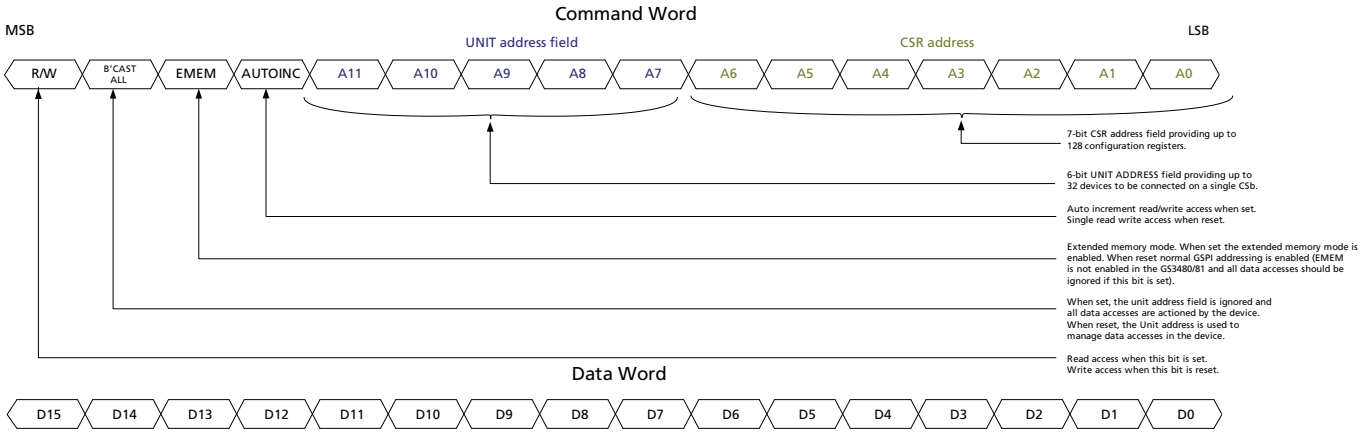


Figure 4-6: Command and Data Word Format

4.7.3 GSPI Timing – Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 4-7 to Figure 4-11.

In this mode, one data word is read from/written to the device per access. Each access is a minimum of 32-bits long, consisting of a command word and a single data word. The read or write cycle begins with a high-to-low transition of the $\overline{CS}$ pin. The read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 75MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of two SCLK clock cycles.

For read access, the time from the last bit of the command word to the start of the data output, as defined by t_{delay}, is no less than four SCLK clock cycles.

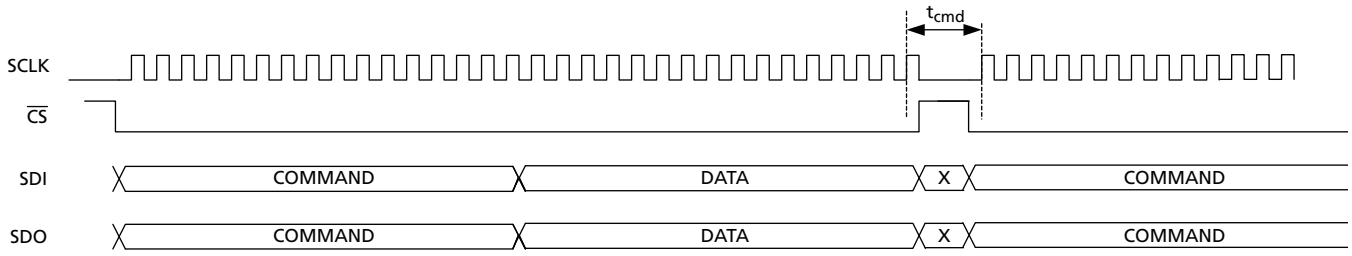


Figure 4-7: GSPI Write Timing – Single Write Access Loop-through Configuration

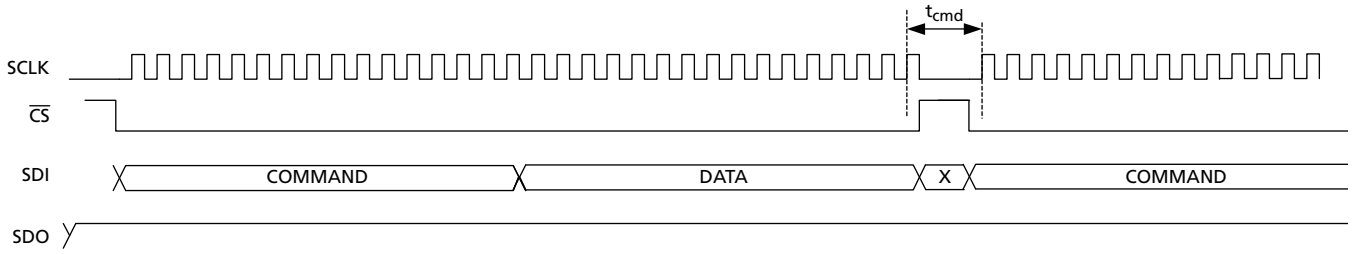


Figure 4-8: GSPI Write Timing – Single Write Access Loop-though Link Disable Configuration

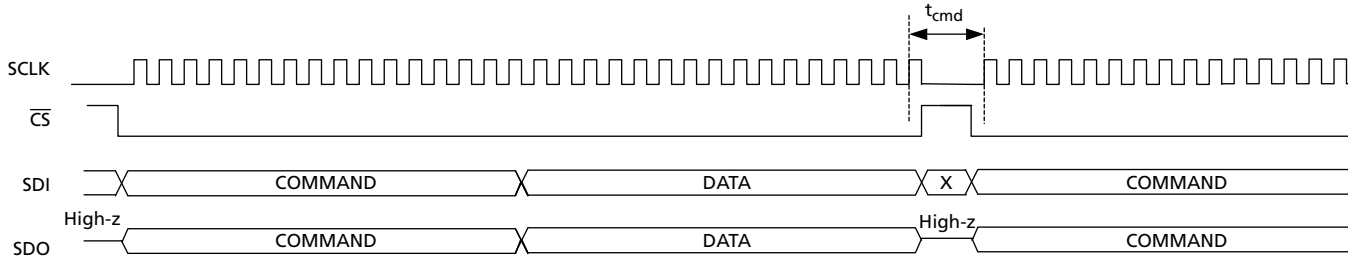


Figure 4-9: GSPI Write Timing – Single Write Access Bus-through Configuration

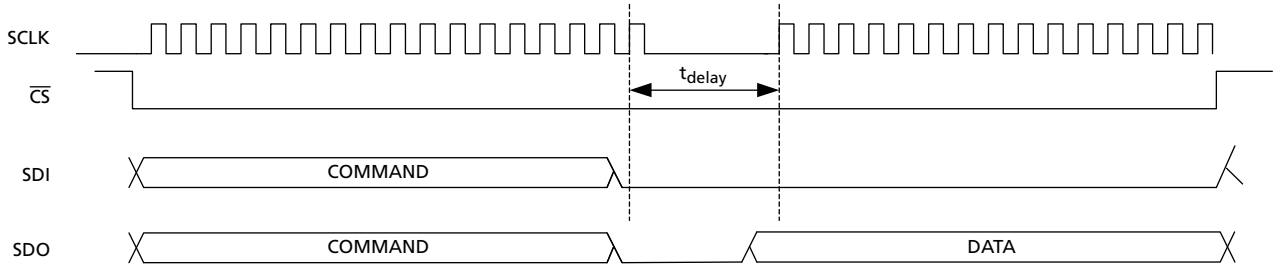


Figure 4-10: GSPI Read Timing – Single Read Access Loop-through Configuration

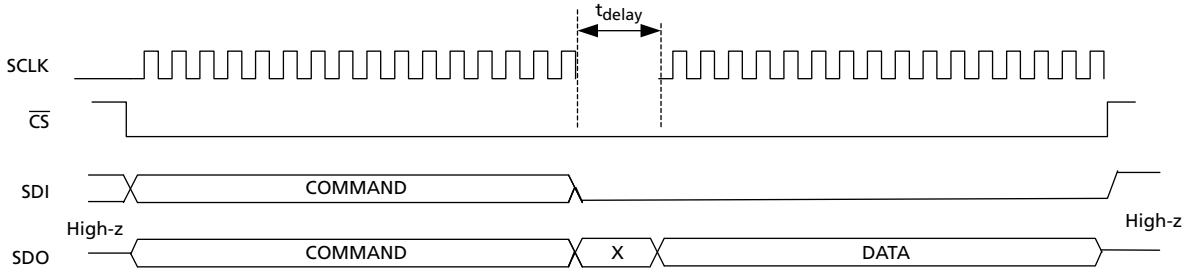


Figure 4-11: GSPI Read Timing – Single Read Access Bus-through Configuration

4.7.4 GSPI Timing – Auto-increment Read/Write Access

Auto-increment read/write access timing for the GSPI interface is shown in Figure 4-12 to Figure 4-16.

Auto-increment mode is initiated by the setting of the AUTOINC bit of the command word.

In this mode, multiple data words can be read from/written to the device per access. Each access is initiated by a high-to-low transition of the $\overline{CS}$ pin, and consists of a command word and one or more data words. Internal addressing is automatically incremented after the first read or write data word, and continues to increment until the read or write access is terminated by a low-to-high transition of the $\overline{CS}$ pin.

The maximum interface clock rate is 75MHz and the inter-command delay time indicated in the diagram as t_{cmd}, is a minimum of two SCLK clock cycles.

For read access, the time from the last bit of the first command word to the start of the data output of the first data word as defined by t_{delay}, should be no less than four SCLK cycles. All subsequent read data accesses will not be subject to this delay in auto-increment read mode.

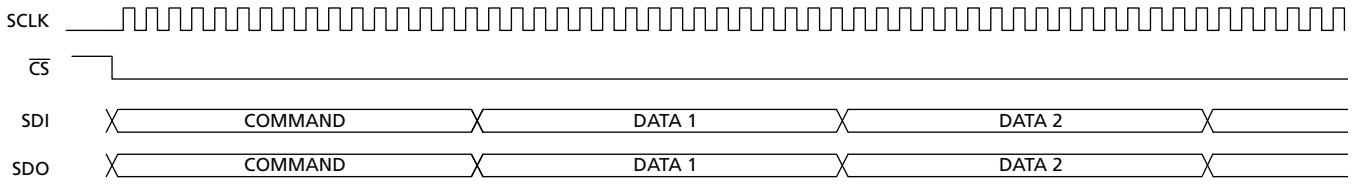


Figure 4-12: GSPI Write Timing – Auto Increment Loop-through Configuration

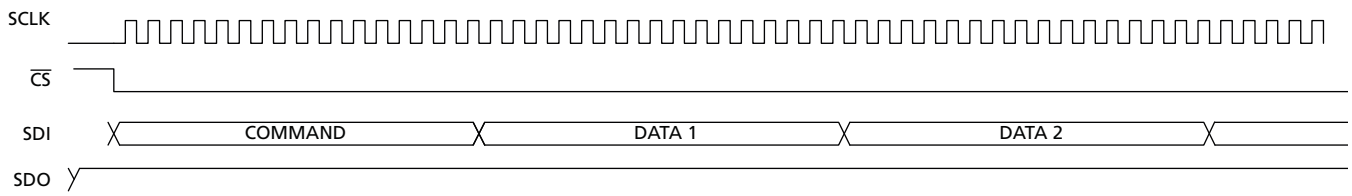


Figure 4-13: GSPI Write Timing – Auto Increment Loop-through Link Disable Configuration

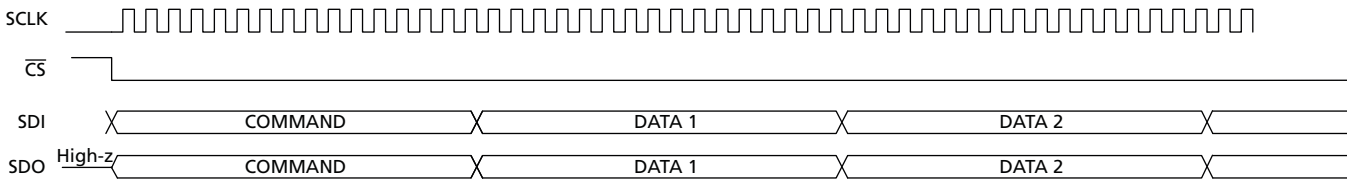


Figure 4-14: GSPI Write Timing – Auto Increment Bus-through Configuration

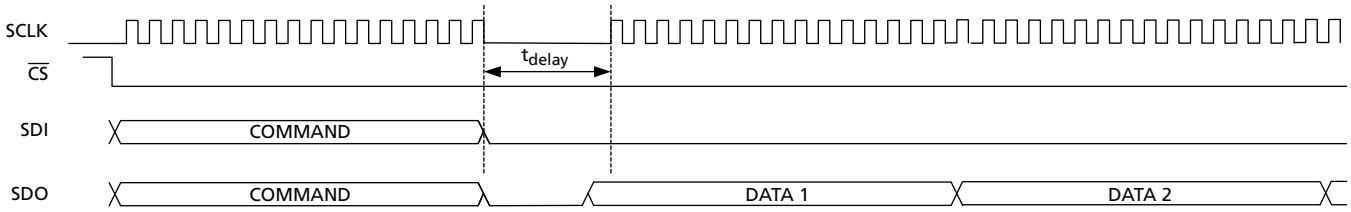


Figure 4-15: GSPI Read Timing – Auto Increment Read Loop-through Configuration

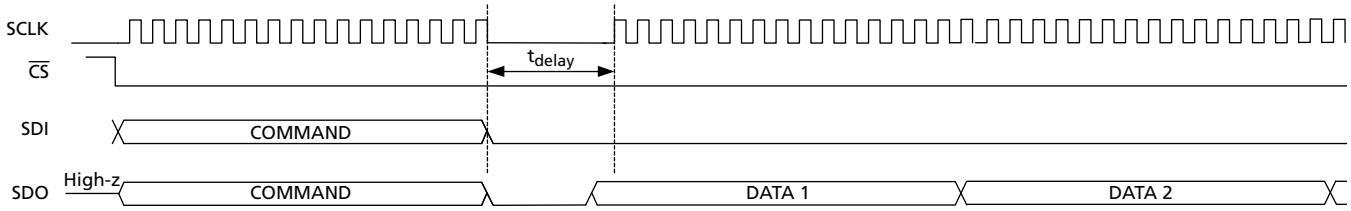


Figure 4-16: GSPI Read Timing – Auto Increment Read Bus-through Configuration

4.7.5 GSPI Mission Mode Operation

By default at power up or after system reset, the GS3481 enters the normal mission mode of operation in which all communication with the application host interface via GSPI, and is managed by the application host processor.

The default host interface configuration mode is loop-through configuration and the internal unit address is set to 0.

To aid understanding of the functional description, Figure 4-17 shows a functional block diagram of the CSR map for the GS3481:

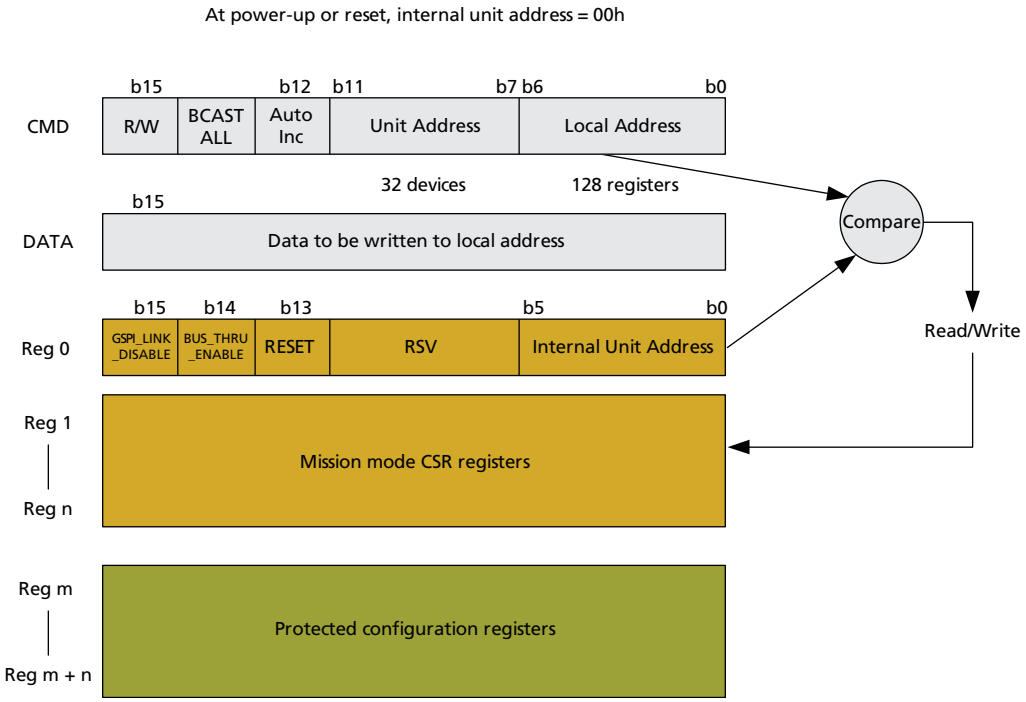


Figure 4-17: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the mission mode CSR registers via the GSPI, are as follows:

1. Set CMD word for write access to the local address for registers 1~n; set write access; set auto increment; set the unit address to match the configured internal unit address which by default will be zero.
2. Write data word to be written to the first CSR registers.
3. Write data word to be written to the next CSR register in auto increment mode, etc.

Read access is the same as the above except in step (1) the CMD word is set for read access.

NOTE: the unit address field of the command word is only required if unit-addressing is employed in loop-though or bus-though configuration. For backwards compatibility with existing GSPI enabled devices, this field should be reserved (set to 0).

4.7.6 Unit Addressing

Multiple (up to 32) devices that implement GSPI can be connected to a common bus in either loop-through or bus-through configuration.

To ensure that each connected device can be uniquely addressed, an individual unit address must be programmed by the host controller as part of the system initialization process.

It should be noted that by default at power up or after system reset, the default unit address of each device is set to 0h and the SDI->SDO non-clocked loop-through for each device is enabled.

The steps required to set-up the unit address are as follows:

1. Write to unit address 0 selecting CSR 0 (local address = 0), with the GSPI_LINK_DISABLE bit set and the INTERNAL UNIT ADDRESS field set to 0. This opens the SDI->SDO non-clocked loop-through for all devices.

   All connected devices receive this command (by default the unit address of all devices is 0), and the loop-through connection will be open for all connected devices.

2. Write to unit address 0 selecting CSR 0 (local address = 0), with the GSPI_LINK_DISABLE bit reset and the INTERNAL UNIT ADDRESS field set to the required unit address (for example: address 1).

   This sets the unit address of the first device in the daisy-chain to 1 and closes the loop-through connection on the first device. No other device in the link will receive this command because the SDI->SDO link is open.

3. Write to unit address 0 selecting CSR 0 (local address = 0), with the GSPI_LINK_DISABLE bit reset and the INTERNAL UNIT ADDRESS field set to the required unit address for the next device in the chain (for example: address 2).

   This sets the unit address of the second device in the daisy-chain to 2 and closes the loop-through connection on the second device. Note that because the unit address field of the command word is 0h, the first device in the chain (with a local unit address of 1), does not respond to the data.

4. Continue with step 3 until all devices in the have a configured local unit address.

Once configured, devices will only respond to commands that have a matching unit address.

It should be noted that although the loop-though and bus-though configurations are compatible with previous generation GSPI enabled devices (backwards and forwards compatibility), all devices capable of unit address configuration must be grouped together on a single chip select and be connected in a contiguous interface. For correct operation, it is not possible to intersperse unit addressable parts with older generation GSPI devices.

4.8 CSR Register Map

Register Name	Address	Bit Slice	Description	R/W Access	Reset Value
CONTROL_REGISTER	0	15:7	RSVD: Reserved.	R/W	0
		6:6	GSPI_LINK_DISABLE: GSPI loop-through disable. When HIGH, the GSPI SDI->SDO loop-through connection is disabled for this device. When LOW, the GSPI SDI->SDO loop-through connection is enabled.	R/W	0
		5:5	BUS_THROUGH_ENABLE: GSPI bus-through mode enable. When HIGH, the GSPI bus-through mode is enabled such that the SDO pin is high-z when $\overline{CS}$ is HIGH, and follows the SDI pin when $\overline{CS}$ is LOW (command word or write operation), or outputs data for read operation. When LOW, the GSPI loop-though mode is enabled such that SDO is a non-clocked loop through of the SDI pin, or outputs data when $\overline{CS}$ is low (read operation).	R/W	0
		4:0	UNIT_ADDRESS: device address programmed by application. Sets the unit address of the device in the range 0 to 31.	R/W	0
SET_IO	1	15:15	POWER_DOWN: device power-down. When operating in host interface control mode, setting this bit HIGH sets the device into power-down mode. When LOW, normal operation of the device is enabled.	R/W	0
		14:14	BALANCE: balance mode enable/disable. Setting this bit HIGH enables the balance mode of operation. When LOW, normal device operation is selected. This register bit is ignored when operating in pin control mode.	R/W	0
		13:13	HIGH_SWING_HOST_ENABLE: high-swing enable pin/host control. When HIGH, the high swing enable/disable setting follows the HIGH_SWING_ENABLE register bit. When LOW, the high swing enable/disable setting follows the HIGH_SWING_EN pin.	R/W	0

Register Name	Address	Bit Slice	Description	R/W Access	Reset Value
SET_IO	1	12:12	HIGH_SWING_ENABLE: high-swing enable. When operating in host interface control mode, setting this bit LOW disables the high-swing mode (more than 1200mV). When HIGH, high-swing mode is enabled (output of the four channels can be more than 1200mV). This register bit is ignored when operating in pin control mode. **NOTE**: host interface or pin control mode for this bit is determined by the setting of the HS_HOST_ENABLE bit.	R/W	0
		11:11	EQ_HOST_ENABLE: Trace EQ pin/host control. When HIGH, the input trace eq enable/disable setting follows the EQ_ENABLE register bit. When LOW, the input trace eq enable/disable setting follows the EQ_EN pin.	R/W	0
		10:10	EQ_ENABLE: Trace EQ on/off. When operating in host interface control mode, setting this bit HIGH enables the input trace EQ with a fixed gain of +3dB. When LOW, the input trace EQ is off. This register bit is ignored when operating in pin control mode. **NOTE**: host interface or pin control mode for this bit is determined by the setting of the EQ_HOST_ENABLE bit.	R/W	0
		9:9	SD/$\overline{\text{HD}}$_HOST_ENABLE: SD/$\overline{\text{HD}}$ pin/host control. When HIGH, the SDO output slew rate setting follows the SD/$\overline{\text{HD}}$ register bit. When LOW, the SDO output slew rate setting follows the SD/$\overline{\text{HD}}$ pin.	R/W	0
		8:8	SD/$\overline{\text{HD}}$: SD/HD Slew Rate control. When operating in host interface control mode, setting this bit HIGH selects SD slew rate for SDO outputs 1 through 4. When LOW, HD slew rate is selected. This register bit is ignored when operating in pin control mode. **NOTE**: host interface or pin control mode for this bit is determined by the setting of the SD/$\overline{\text{HD}}$_HOST_ENABLE bit.	R/W	0
		7:7	SDO4_HOST_ENABLE: SDO output 4 pin/host control. When HIGH, the SDO output 4 enable/disable setting follows the SDO4_ENABLE register bit. When LOW, the SDO output 4 enable/disable setting follows the OUT4_EN pin.	R/W	0

Register Name	Address	Bit Slice	Description	R/W Access	Reset Value
SET_IO	1	6:6	SDO4_ENABLE: SDO output 4 enable. When operating in host interface control mode, setting this bit LOW disables SDO output 4. When HIGH, SDO output 4 is enabled. This register bit is ignored when operating in pin control mode. **NOTE**: host interface or pin control mode for this bit is determined by the setting of the SDO4_HOST_ENABLE bit.	R/W	0
		5:5	SDO3_HOST_ENABLE: SDO output 3 pin/host control. When HIGH, the SDO output 3 enable/disable setting follows the OUT3_ENABLE register bit. When LOW, the SDO output 3 enable/disable setting follows the OUT3_EN pin.	R/W	0
		4:4	SDO3_ENABLE: SDO output 3 enable. When operating in host interface control mode, setting this bit LOW disables SDO output 3. When HIGH, SDO output 3 is enabled. This register bit is ignored when operating in pin control mode. **NOTE**: host interface or pin control mode for this bit is determined by the setting of the SDO3_HOST_ENABLE bit.	R/W	0
		3:3	SDO2_HOST_ENABLE: SDO output 2 pin/host control. When HIGH, the SDO output 2 enable/disable setting follows the SDO2_ENABLE register bit. When LOW, the SDO output 2 enable/disable setting follows the OUT2_EN pin.	R/W	0
		2:2	SDO2_ENABLE: SDO output 2 enable. When operating in host interface control mode, setting this bit LOW disables SDO output 2. When HIGH, SDO output 2 is enabled. This register bit is ignored when operating in pin control mode. **NOTE**: host interface or pin control mode for this bit is determined by the setting of the SDO2_HOST_ENABLE bit.	R/W	0
		1:1	SDO1_HOST_ENABLE: SDO output 1 pin/host control. When HIGH, the SDO output 1 enable/disable setting follows the SDO1_ENABLE register bit. When LOW, the SDO output 1 enable/disable setting follows the OUT1_EN pin.	R/W	0

Register Name	Address	Bit Slice	Description	R/W Access	Reset Value
SET_IO	1	0:0	SDO1_ENABLE: SDO output 1 enable. When operating in host interface control mode, setting this bit HIGH enables SDO output 1. When HIGH, SDO output 1 is enabled. This register bit is ignored when operating in pin control mode. **NOTE**: host interface or pin control mode for this bit is determined by the setting of the SDO1_HOST_ENABLE bit	R/W	0
OUTPUT _PREEMPHASIS _SET	2	15:8	RSVD: Reserved	R/W	0
		7:4	SDO3_4_PRE_EMPHASIS: SDO output 3 and output 4 pre-emphasis control. Sets the amount of pre-emphasis applied to SDO outputs 3 and 4 in the range 0dB to +9dB. 0h = 0dB (pre-emphasis off) 1h = 1dB 2h = 2dB 3h = 3dB 4h = 4dB 5h = 5dB 6h = 6dB 7h = 7dB 8h = 8dB 9h = 9dB All other values = 9dB	R/W	0
		3:0	SDO1_2_PRE_EMPHASIS: SDO output 1 and output 2 pre-emphasis control. Sets the amount of pre-emphasis applied to SDO outputs 1 and 2 in the range 0dB to +9dB. 0h = 0dB (pre-emphasis off) 1h = 1dB 2h = 2dB 3h = 3dB 4h = 4dB 5h = 5dB 6h = 6dB 7h = 7dB 8h = 8dB 9h = 9dB All other values = 9dB	R/W	0

Register Name	Address	Bit Slice	Description	R/W Access	Reset Value
FINE_CONTROLS	3	11:8	RSVD: Reserved	—	0
		7:4	SDO3_4_SWING_TRIM: SDO output 3 & 4 swing control. Provides a fine trim of the output swing for SDO outputs 3 and 4 in the range of -15% to +20% of nominal (set by the RSET resistor). x000b = 0% (no offset) x001b = 5% x010b = 10% x011b = 15% x100b to x111b = 20% Bit 3 of the SDO3_4_TRIM value is a sign bit. When LOW, all trim values provide positive adjustment. When HIGH, all trim values provide negative adjustment.	R/W	0
		3:0	SDO1_2_SWING_TRIM: SDO output 1 & 2 swing control. Provides a fine trim of the output swing for SDO outputs 1 and 2 in the range of -15% to +20% of nominal (set by the RSET resistor). x000b = 0% (no offset) x001b = 5% x010b = 10% x011b = 15% x100b to x111b = 20% Bit 3 of the SDO1_2_TRIM value is a sign bit. When LOW, all trim values provide positive adjustment. When HIGH, all trim values provide negative adjustment.	R/W	0

Register Name	Address	Bit Slice	Description	R/W Access	Reset Value
INPUT_PRESENT	4	15:4	RSVD: Reserved	—	0
		3:3	SDO4_SIGNAL_PRESENT: output signal presence status signal. When HIGH, a valid input signal is present and output 4 is enabled. When LOW, either the input signal is invalid or SDO output 4 is disabled.	RO	0
		2:2	SDO3_SIGNAL_PRESENT: output signal presence status signal. When HIGH, a valid input signal is present and output 3 is enabled. When LOW, either the input signal is invalid or SDO output 3 is disabled.	RO	0
		1:1	SDO2_SIGNAL_PRESENT: output signal presence status signal. When HIGH, a valid input signal is present and output 2 is enabled. When LOW, either the input signal is invalid or SDO output 2 is disabled.	RO	0
		0:0	SDO1_SIGNAL_PRESENT: output signal presence status signal. When HIGH, a valid input signal is present and output 1 is enabled. When LOW, either the input signal is invalid or SDO output 1 is disabled.	RO	0

5. Application Information

5.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV.

An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance
- Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high-speed traces
- High-speed traces are round-curved (rather than 45° or 90° angles) to minimize impedance variations due to change of PCB trace width

NOTE: For more recommendations on Trace Lengths, ORL Inductor Values and other PCB Layout Considerations, please refer to Gennum's SDI Design Guide (Doc ID 55280).

5.2 Typical Application Circuit

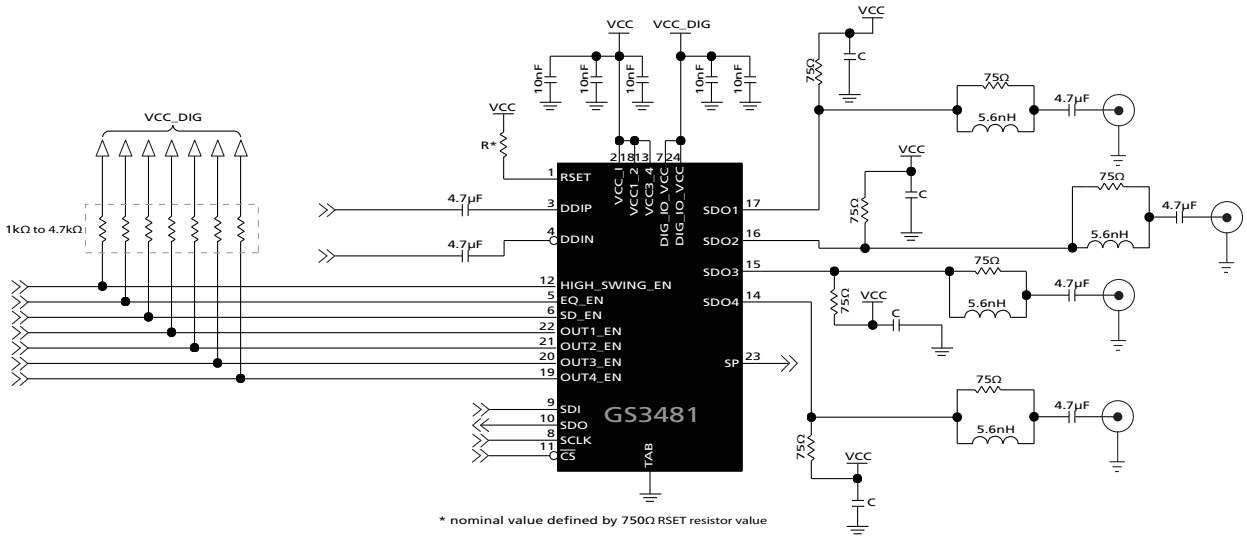
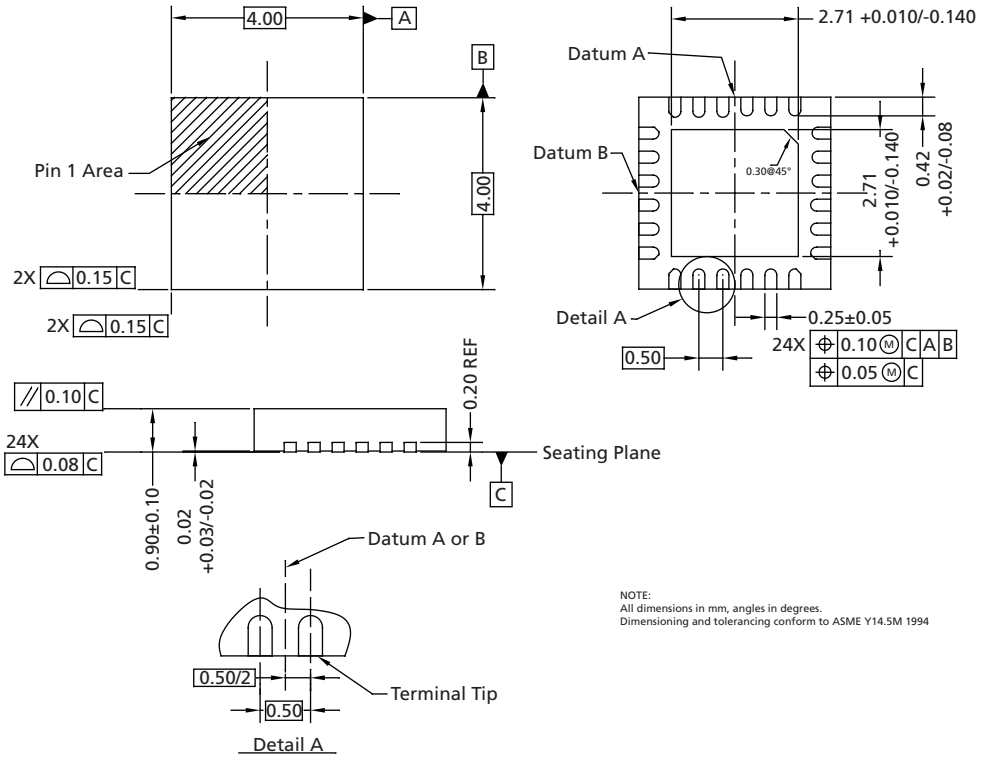


Figure 5-1: GS3481 Typical Application Circuit

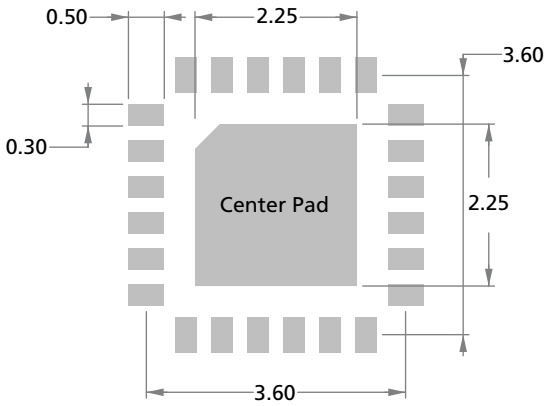
6. Package & Ordering Information

6.1 Package Dimensions



NOTE:
All dimensions in mm, angles in degrees.
Dimensioning and tolerancing conform to ASME Y14.5M 1994

6.2 Recommended PCB Footprint



NOTE:
All dimensions in mm

The Center Pad should be connected to the most negative power supply plane (VEE) by a minimum of five vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.3 Packaging Data

Parameter	Value
Package type/dimensions/pad pitch	24-pin QFN/4mm x 4mm/0.5mm pitch
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, Ψ	11.0°C/W
Pb-free and RoHS compliant, Halogen-free	Yes

6.4 Solder Reflow Profile

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 6-1.

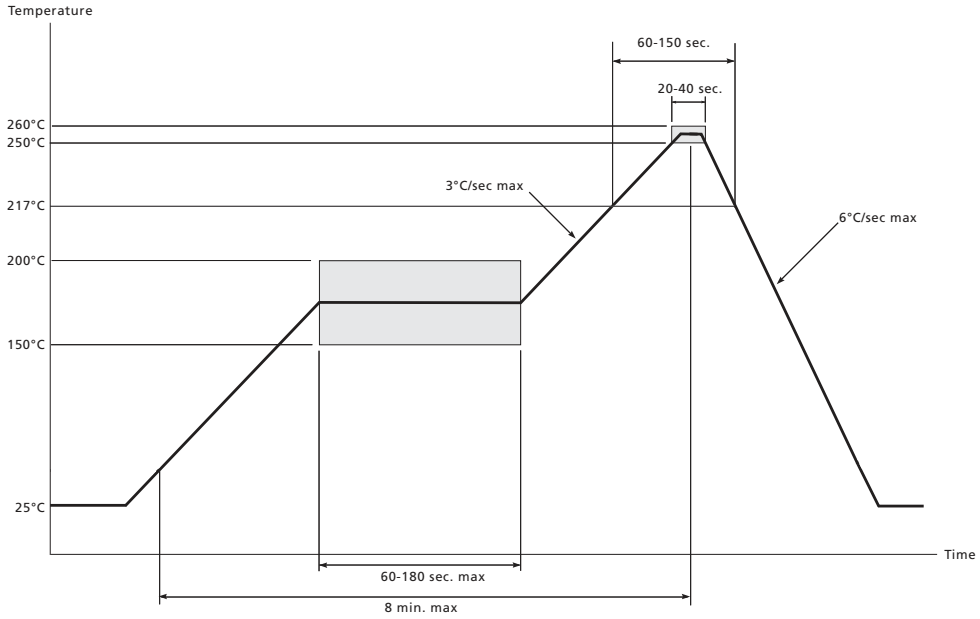
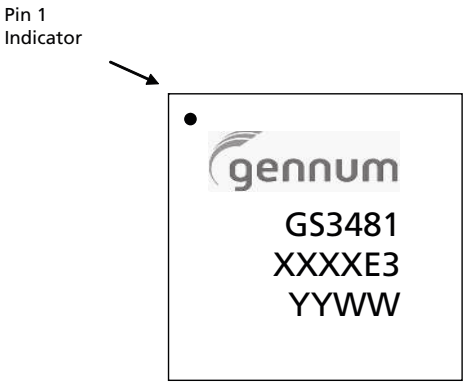


Figure 6-1: Maximum Pb-free Solder Reflow Profile

6.5 Marking Diagrams



Instructions:	
GS3481	Package Mark
XXXX	Last 4 digits (excluding decimal) of SAP Batch Assembly (FIN) as listed on Packing Slip
E3	Pb-free & Green indicator
YYWW	Date Code

6.6 Ordering Information

Part Number	Package	Temperature Range
GS3481-INE3	24-pin QFN	-40°C to 85°C
GS3481-INTE3	24-pin QFN (250pc Reel)	-40°C to 85°C
GS3481-INTE3Z	24-pin QFN (2,500pc Reel)	-40°C to 85°C

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
A	156761	—	August 2011	New document.

DOCUMENT IDENTIFICATION
ADVANCE INFORMATION NOTE
The product is in a development phase and specifications are subject to change without notice. Gennum reserves the right to remove the product at any time. Listing the product does not constitute an offer for sale.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

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