11.90 GHz to 18.30 GHz Quadband VCO

Data Sheet **HMC8362**

FEATURES

- Set of 4 narrow-band VCOs with consistent sensitivity vs. frequency
- RF and tuning ports common to all 4 VCOs
- RF output operates from fundamental oscillators with no subharmonic oscillations
- Up to 8 dBm RF output power
- Power mute capability
- No external resonator required
- 40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

- Electronic test and measurement
- Industrial and medical instrumentation
- Point to point and multipoint radios
- Aerospace and defense
- Wireless communication infrastructure

FUNCTIONAL BLOCK DIAGRAM

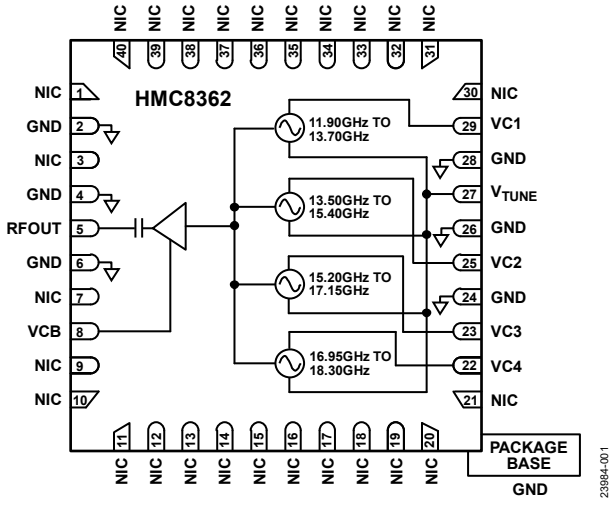

Figure 1.

GENERAL DESCRIPTION

The HMC8362 is a gallium arsenide (GaAs), quadband, monolithic microwave integrated circuit (MMIC), voltage controlled oscillator (VCO) designed to offer wideband capabilities without compromising on phase noise performance. The device integrates four independent, narrow-band VCOs with overlapping frequency bands, operating at a fundamental frequency range of 11.90 GHz to 18.30 GHz. The consistent tuning sensitivity across all frequency bands simplifies the synthesizer loop filter design.

The tuning port is common to all VCO cores for a simpler design of the phase-locked loop (PLL) feedback path. The HMC8362 also offers a low typical current consumption of 72 mA for power sensitive applications.

The HMC8362 integrates resonators, negative resistance devices, and varactor diodes. The monolithic structure of the oscillator offers very low phase noise, optimal temperature stability, and is immune to vibration and process variation.

The four VCOs are packaged in a single, 6 mm × 6 mm, surface-mount lead frame chip scale package (LFCSP), and require no external matching components.

Combined with a high frequency, high performance phase-locked loop (PLL), the ADF41513, the HMC8362 offers a complete RF or microwave frequency generation solution.

Rev. A
Document Feedback

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REVISION HISTORY

9/2020—Revision A: Initial Version

SPECIFICATIONS

T_A = −40°C to +85°C, Band 1 to Band 4 supply voltage (V_{CC}) = 5 V, buffer supply voltage (V_{CB}) = 5 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF OUTPUT CHARACTERISTICS					
Frequency (f_{OUT})					
Band 1	11.90		13.70	GHz	
Band 2	13.50		15.40	GHz	
Band 3	15.20		17.15	GHz	
Band 4	16.95		18.30	GHz	
Output Power (P_{OUT})					
Band 1	−4	+1.9	+8	dBm	
Band 2	−4	+0.8	+8	dBm	
Band 3	−4	+3	+8	dBm	
Band 4	−4	+1.8	+8	dBm	
P_{OUT} with Buffer Amplifier Muted					Measured at V_{CB} = 0 V
Band 1		−27		dBm	
Band 2		−20		dBm	
Band 3		−25		dBm	
Band 4		−30		dBm	
Tuning Sensitivity					
Band 1		226		MHz/V	
Band 2		246		MHz/V	
Band 3		272		MHz/V	
Band 4		291		MHz/V	
Frequency Drift Rate					Drift specifications are not de-embedded to remove contribution from the evaluation board
Band 1		1.7		MHz/°C	
Band 2		2		MHz/°C	
Band 3		2.4		MHz/°C	
Band 4		2.6		MHz/°C	
Harmonic Content					Worst measured value at typical
Second Harmonic		12		dBc	
Third Harmonic		30		dBc	
Frequency Pulling		0.5		MHz p-p	Worst measured value at typical
Frequency Pushing		30		MHz/V	Worst measured value at typical
Output Return Loss		8		dB	Worst measured value at typical
POWER SUPPLIES					
Supply Voltage	4.75	5.0	5.25	V	
Supply Current (I_{CC})					
Band 1		63		mA	
Band 2		63		mA	
Band 3		67		mA	
Band 4		67		mA	
Buffer Amplifier		9		mA	
Total Supply Current		72	95	mA	Total supply current is for the output buffer and one VCO band; only one VCO band must be powered at a time
Tuning Voltage	1.0		13.5	V	
Tuning Port Leakage Current			60	µA	V_{TUNE} = 13.5 V, where the maximum tune port leakage current is measured

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SINGLE SIDEBAND PHASE NOISE					
Band 1					
10 kHz		−74		dBc/Hz	
100 kHz		−101		dBc/Hz	
1 MHz		−128		dBc/Hz	
Band 2					
10 kHz		−71		dBc/Hz	
100 kHz		−99		dBc/Hz	
1 MHz		−126		dBc/Hz	
Band 3					
10 kHz		−69		dBc/Hz	
100 kHz		−96		dBc/Hz	
1 MHz		−124		dBc/Hz	
Band 4					
10 kHz		−66		dBc/Hz	
100 kHz		−94		dBc/Hz	
1 MHz		−122		dBc/Hz	

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_{C1} to V_{C4}, V_{CB}[1]	5.5 V dc
V_{TUNE}	0 V to 15 V
Temperature	
Operating	−40°C to +85°C
Storage	−65°C to +150°C
Maximum Junction to Maintain 1 Million Hours Mean Time to Failure (MTTF)	135°C
Peak Reflow (Moisture Sensitivity Level (MSL) 3 Rating)	260°C

[1] Only one VCO band must be powered at a time. V_{C1} to V_{C4} are the Band 1 to Band 4 supply voltages on the VC1 to VC4 pins, respectively.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
HCP-40-1	27.50	17.96	°C/W

[1] The thermal impedance simulated values are based on the JESD51 standard using 2S2P on FR4 with four standard JEDEC vias (0.3 mm diameter, 0.025 mm plating, and 1.2 mm pitch).

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for HMC8362

Table 4. HMC8362, 40-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1A
CDM	±1000	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

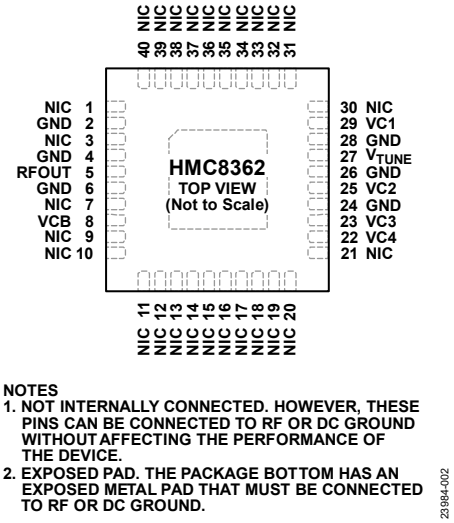

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 7, 9 to 21, 30 to 40	NIC	Not Internally Connected. However, these pins can be connected to RF or dc ground without affecting the performance of the device.
2, 4, 6, 24, 26, 28	GND	Ground. The GND pins must be connected to RF or dc ground.
5	RFOUT	RF Output. The RFOUT pin is ac-coupled, and maintaining a voltage standing wave ratio (VSWR) load of ≤2.0:1 across frequency is recommended.
8	VCB	Buffer Supply Voltage.
22	VC4	Band 4 Supply Voltage.
23	VC3	Band 3 Supply Voltage.
25	VC2	Band 2 Supply Voltage.
27	V_{TUNE}	Control Voltage and Modulation Input. The modulation bandwidth is dependent on the drive source impedance.
29	VC1	Band 1 Supply Voltage.
	EP	Exposed Pad. The package bottom has an exposed metal pad that must be connected to RF or dc ground.

INTERFACE SCHEMATICS

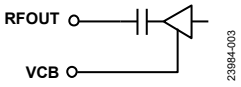

Figure 3. RFOUT and VCB Interface Schematic

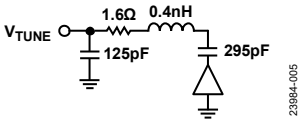

Figure 5. V_{TUNE} Interface Schematic

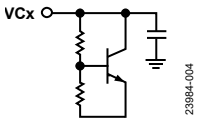

Figure 4. VC1 to VC4 Interface Schematic

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

BAND 1: 11.90 GHz TO 13.70 GHz, V_{CC} = 5 V

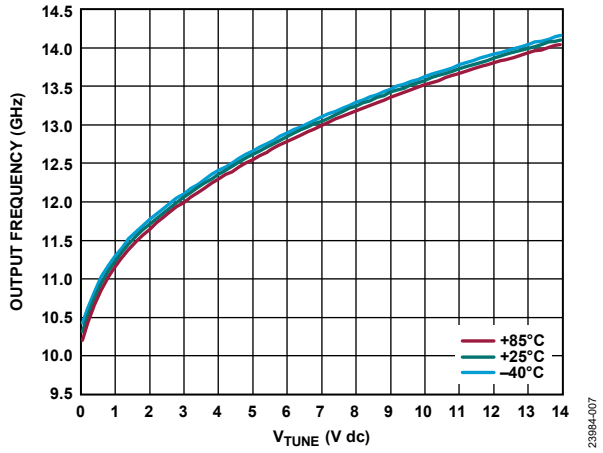

Figure 7. Output Frequency vs. V_{TUNE} for Various Temperatures

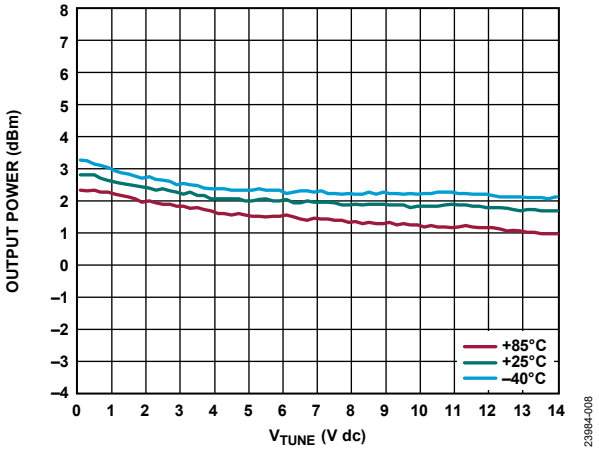

Figure 10. Output Power vs. V_{TUNE} for Various Temperatures

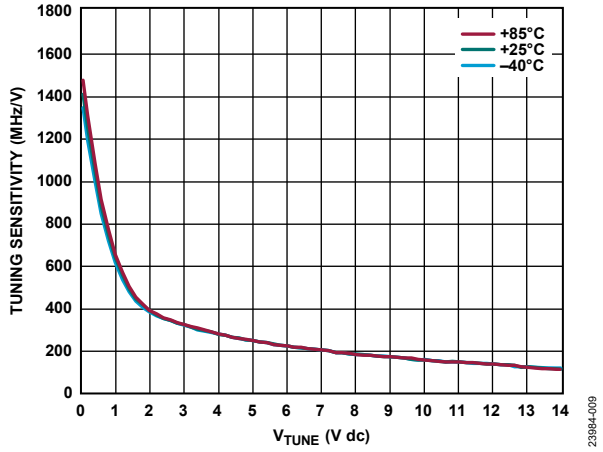

Figure 8. Tuning Sensitivity vs. V_{TUNE} for Various Temperatures

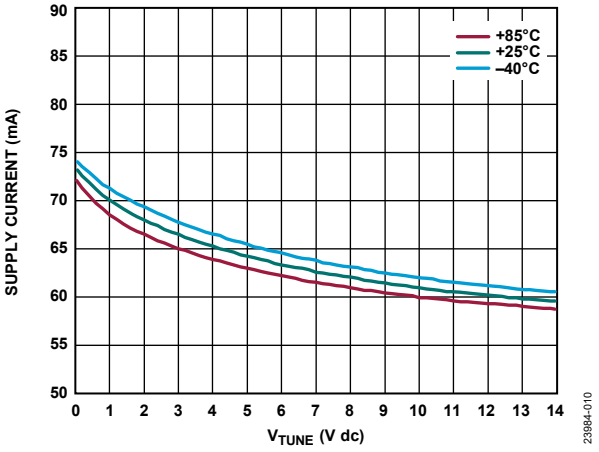

Figure 11. Supply Current vs. V_{TUNE} for Various Temperatures

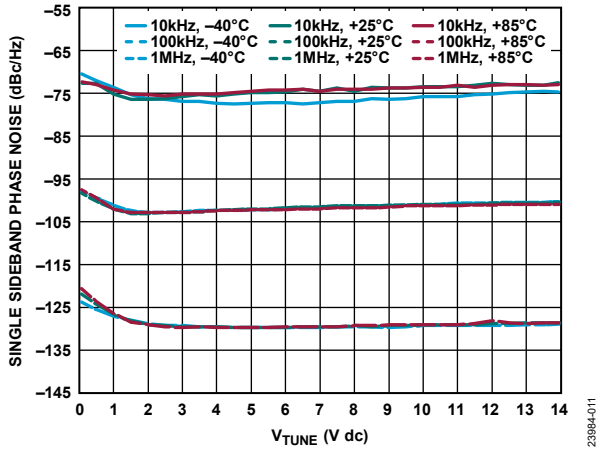

Figure 9. Single Sideband Phase Noise vs. V_{TUNE} for Various Temperatures and Frequencies

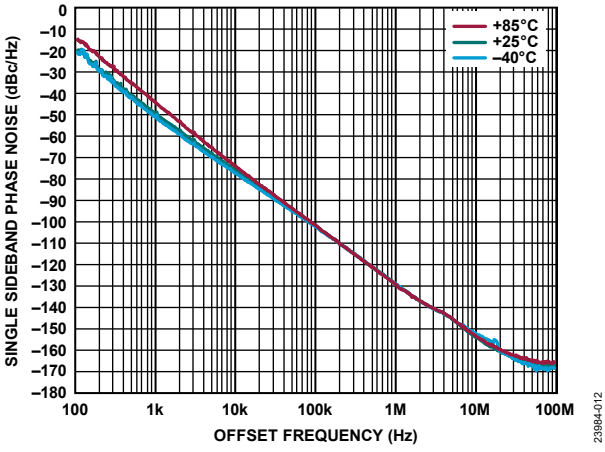

Figure 12. Single Sideband Phase Noise vs. Offset Frequency for Various Temperatures at V_{TUNE} = 5 V

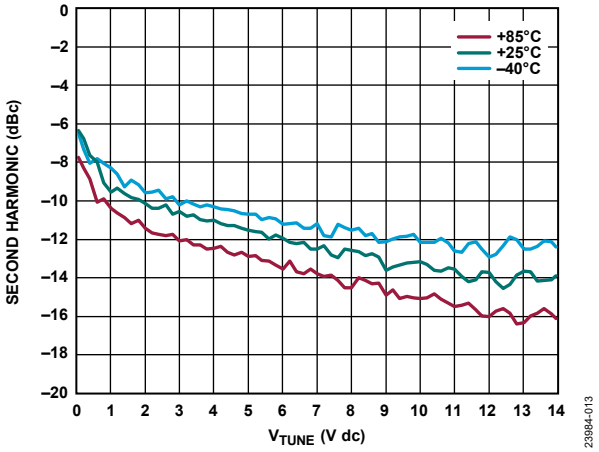

Figure 13. Second Harmonic vs. V_{TUNE} for Various Temperatures

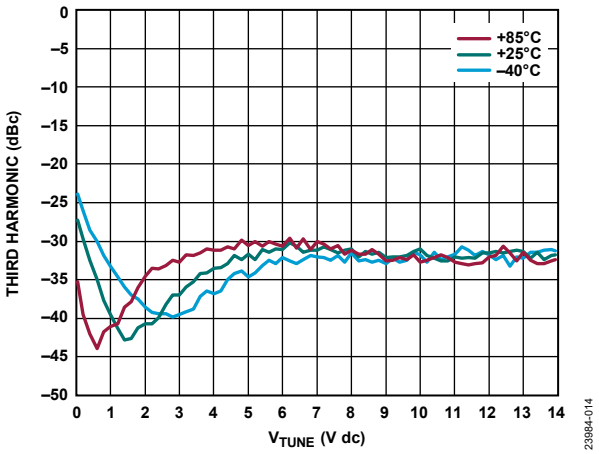

Figure 14. Third Harmonic vs. V_{TUNE} for Various Temperatures

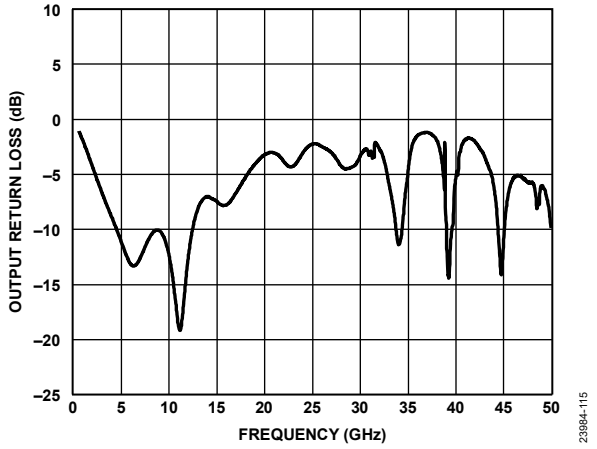

Figure 15. Output Return Loss vs. Frequency at V_{TUNE} = 7.25 V, V_{CB} = 5 V, T_A = 25°C

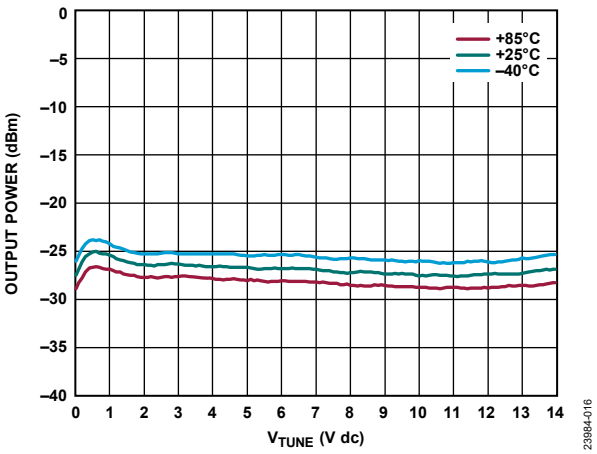

Figure 16. Output Power vs. V_{TUNE} at V_{CB} = 0 V for Various Temperatures

BAND 2: 13.50 GHz TO 15.40 GHz, V_{CC} = 5 V

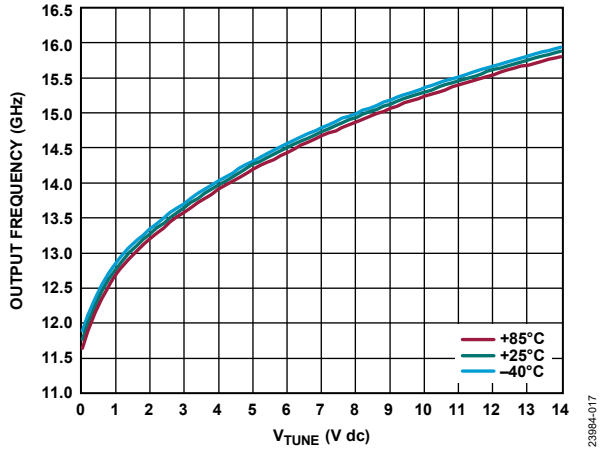

Figure 17. Output Frequency vs. V_{TUNE} for Various Temperatures

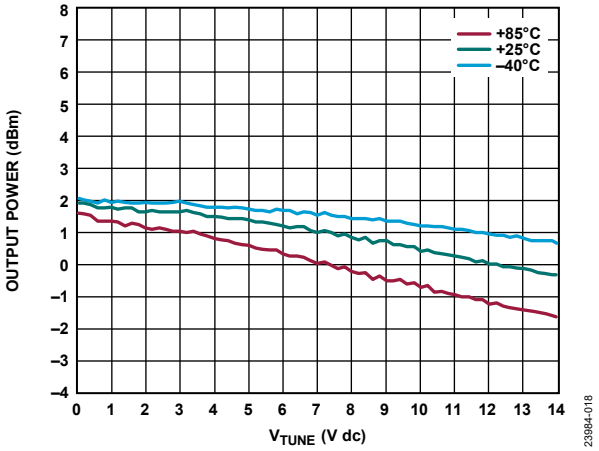

Figure 20. Output Power vs. V_{TUNE} for Various Temperatures

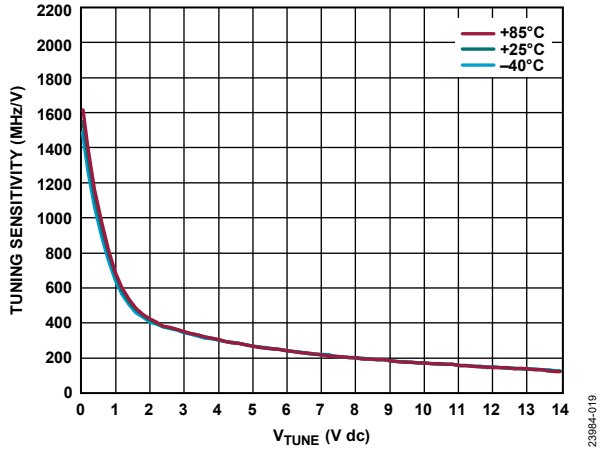

Figure 18. Tuning Sensitivity vs. V_{TUNE} for Various Temperatures

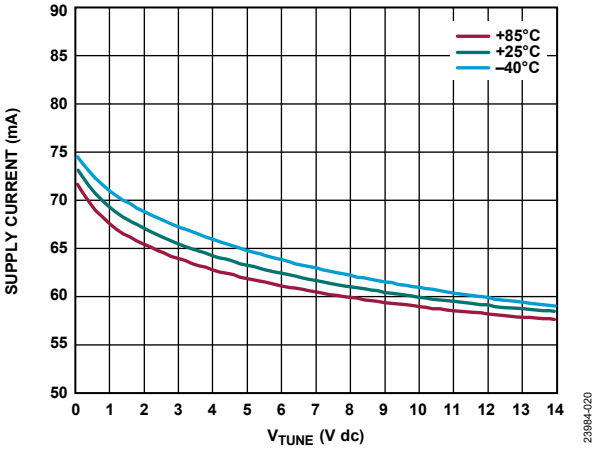

Figure 21. Supply Current vs. V_{TUNE} for Various Temperatures

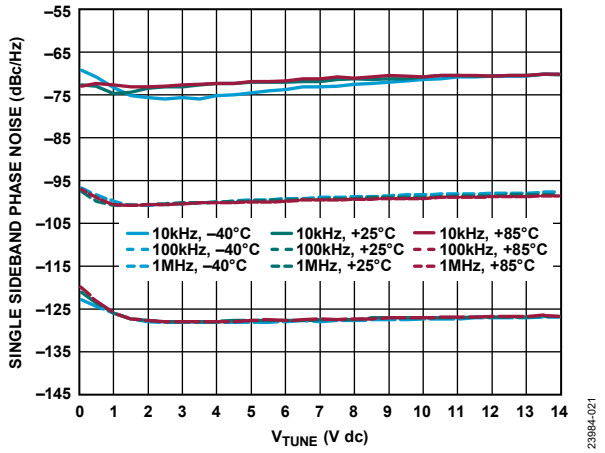

Figure 19. Single Sideband Phase Noise vs. V_{TUNE} for Various Temperatures and Frequencies

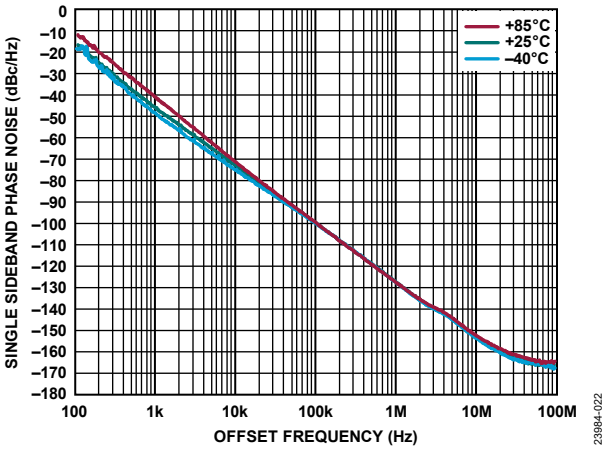

Figure 22. Single Sideband Phase Noise vs. Offset Frequency for Various Temperatures at V_{TUNE} = 5 V

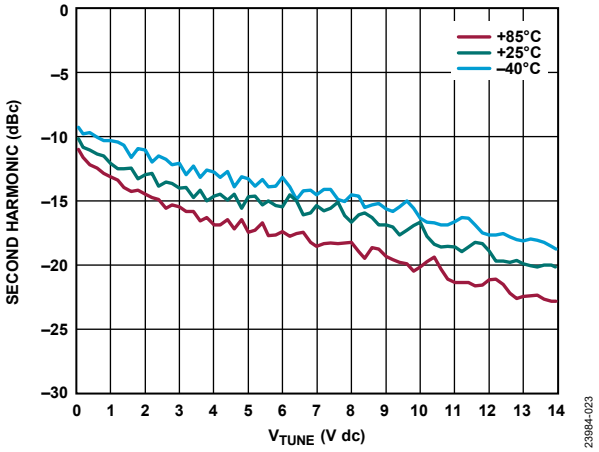

Figure 23. Second Harmonic vs. V_{TUNE} for Various Temperatures

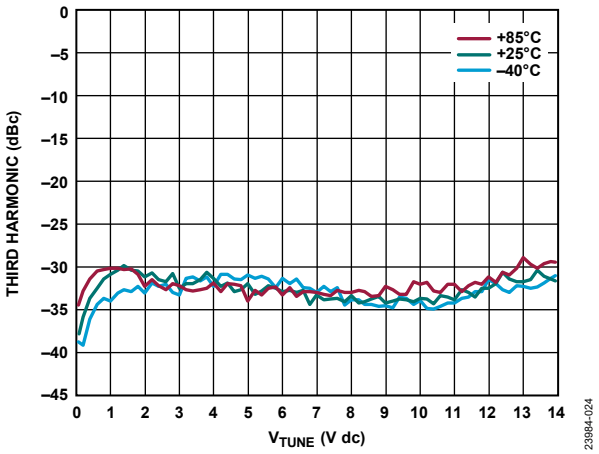

Figure 24. Third Harmonic vs. V_{TUNE} for Various Temperatures

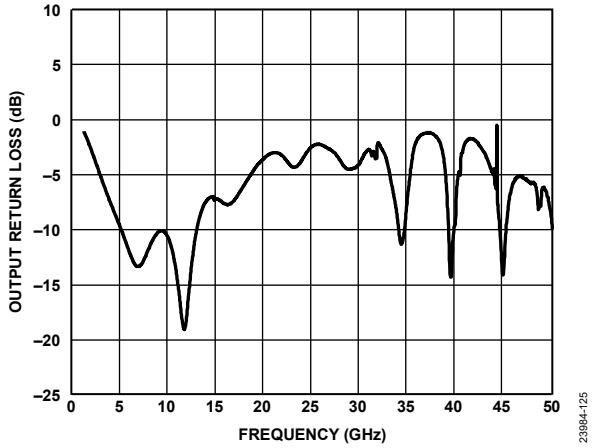

Figure 25. Output Return Loss vs. Frequency at V_{TUNE} = 7.25 V, V_{CB} = 5 V, T_A = 25°C

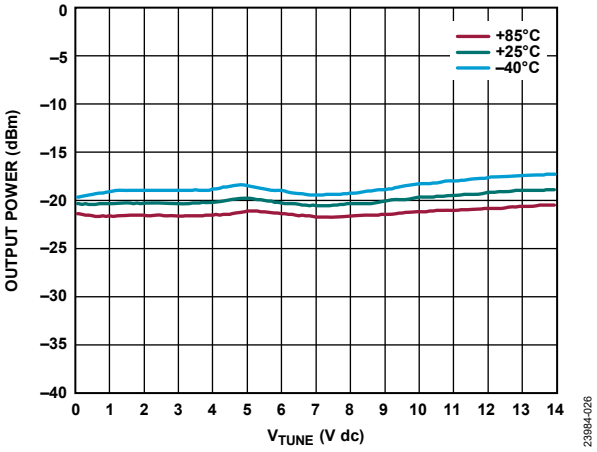

Figure 26. Output Power vs. V_{TUNE} at V_{CB} = 0 V for Various Temperatures

BAND 3: 15.20 GHz TO 17.15 GHz, V_{CC} = 5 V

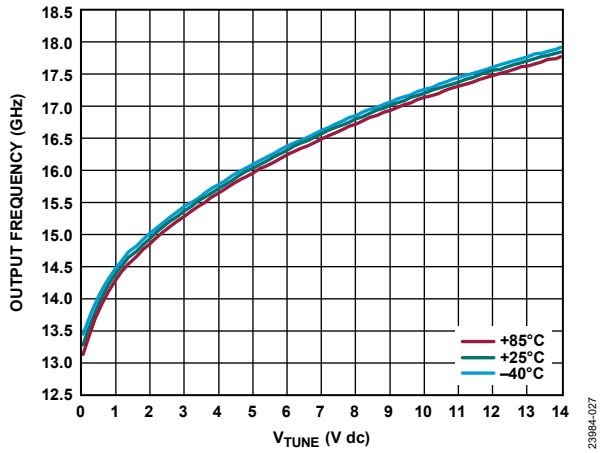

Figure 27. Output Frequency vs. V_{TUNE} for Various Temperatures

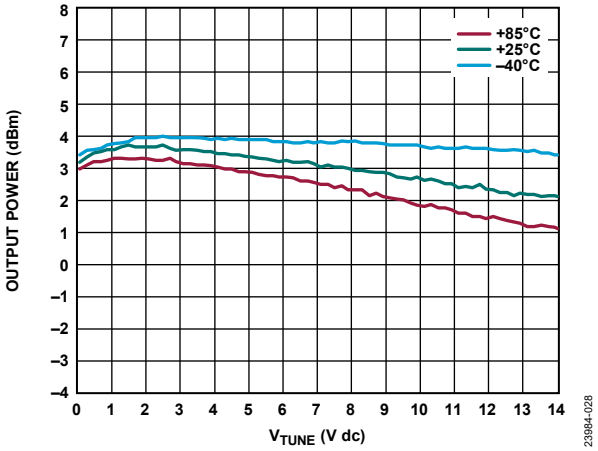

Figure 30. Output Power vs. V_{TUNE} for Various Temperatures

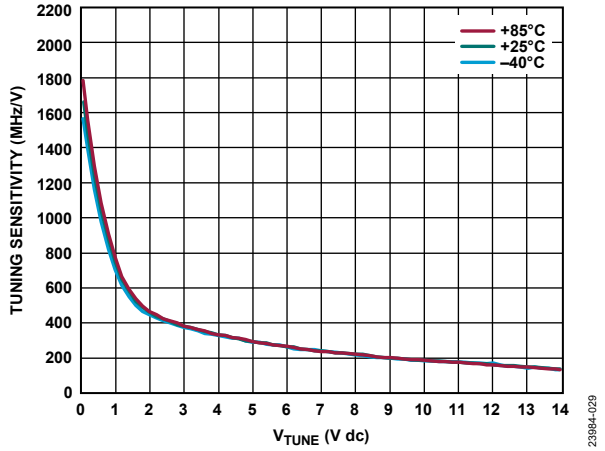

Figure 28. Tuning Sensitivity vs. V_{TUNE} for Various Temperatures

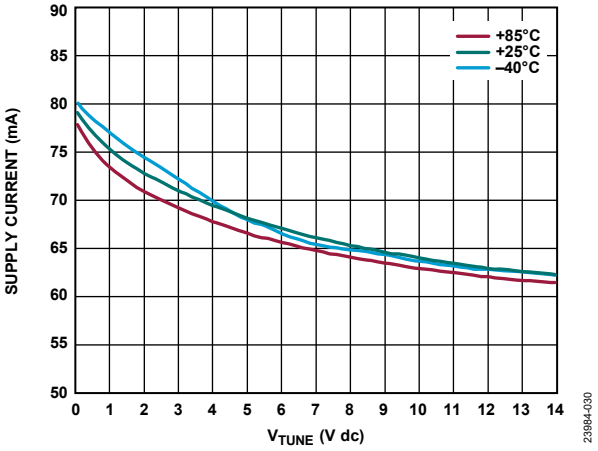

Figure 31. Supply Current vs. V_{TUNE} for Various Temperatures

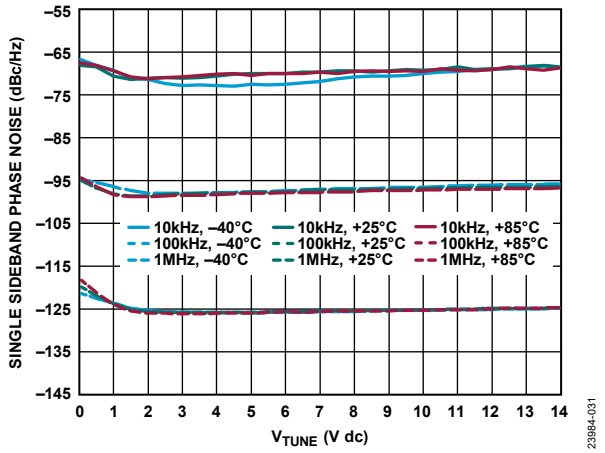

Figure 29. Single Sideband Phase Noise vs. V_{TUNE} for Various Temperatures and Frequencies

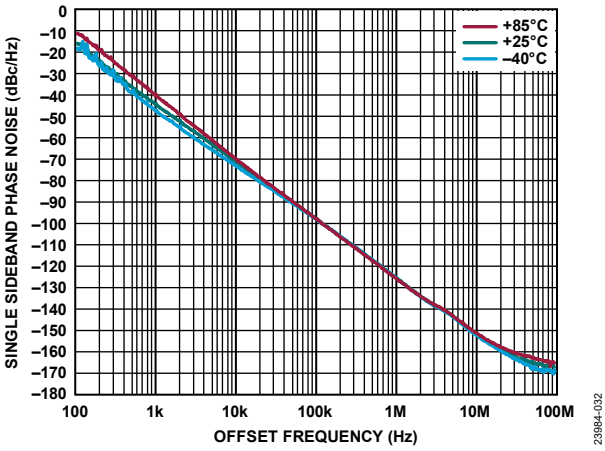

Figure 32. Single Sideband Phase Noise vs. Offset Frequency for Various Temperatures at V_{TUNE} = 5 V

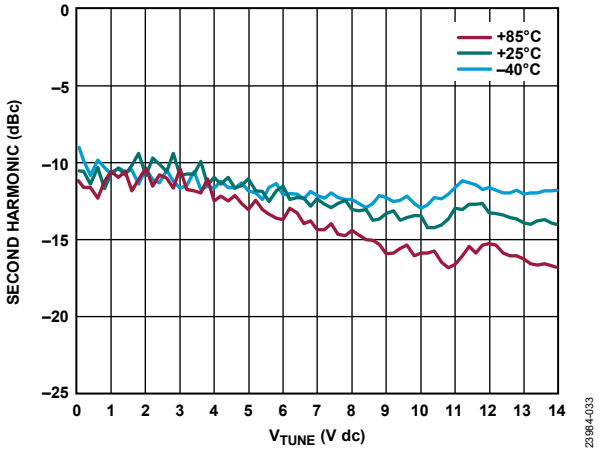

Figure 33. Second Harmonic vs. V_{TUNE} for Various Temperatures

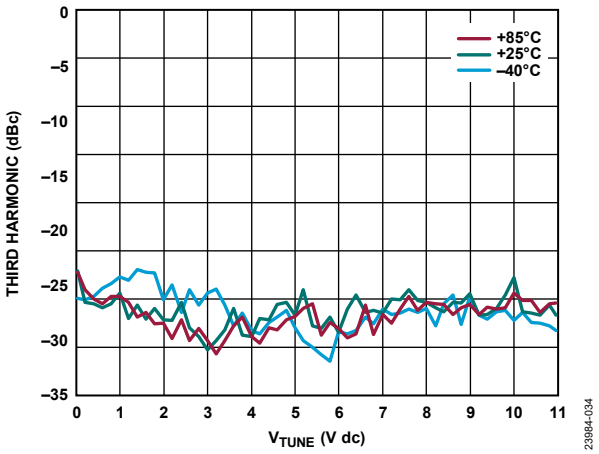

Figure 34. Third Harmonic vs. V_{TUNE} for Various Temperatures, (Measurement Up to 6.5 V Only Due to Equipment Limitation)

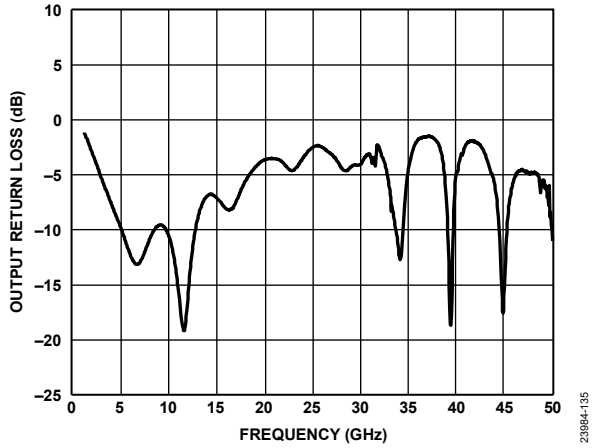

Figure 35. Output Return Loss vs. Frequency at V_{TUNE} = 7.25 V, V_{CC} = 5 V, V_{CB} = 5 V, T = 25°C

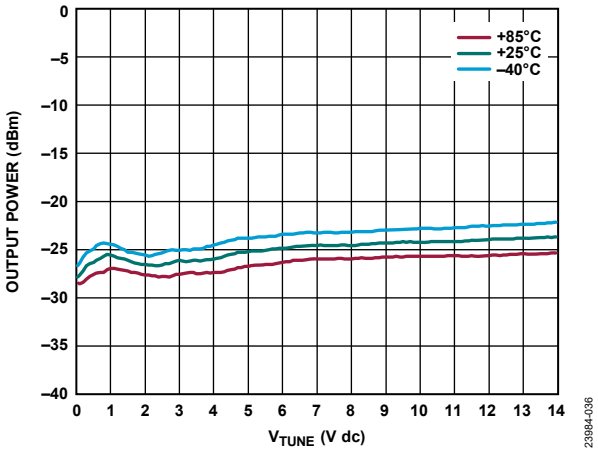

Figure 36. Output Power vs. V_{TUNE} at V_{CB} = 0 V for Various Temperatures

BAND 4: 16.95 GHz TO 18.30 GHz, V_{CC} = 5 V

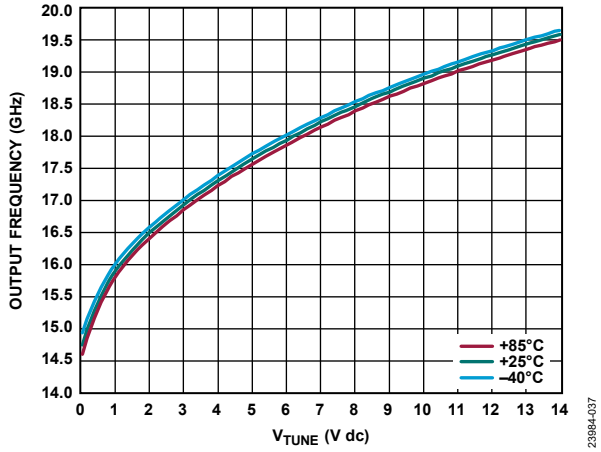

Figure 37. Output Frequency vs. V_{TUNE} for Various Temperatures

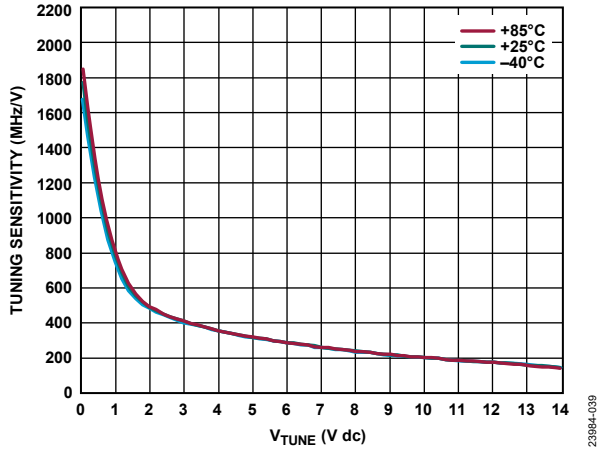

Figure 38. Tuning Sensitivity vs. V_{TUNE} for Various Temperatures

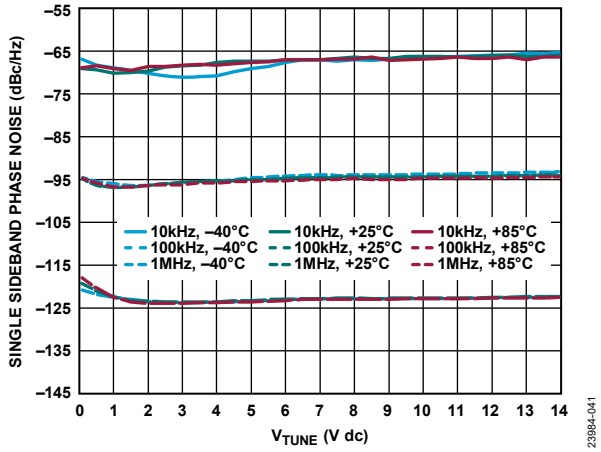

Figure 39. Single Sideband Phase Noise vs. V_{TUNE} for Various Temperatures and Frequencies

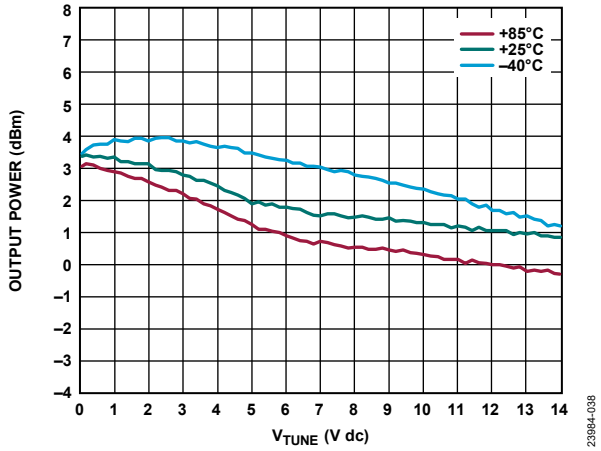

Figure 40. Output Power vs. V_{TUNE} for Various Temperatures

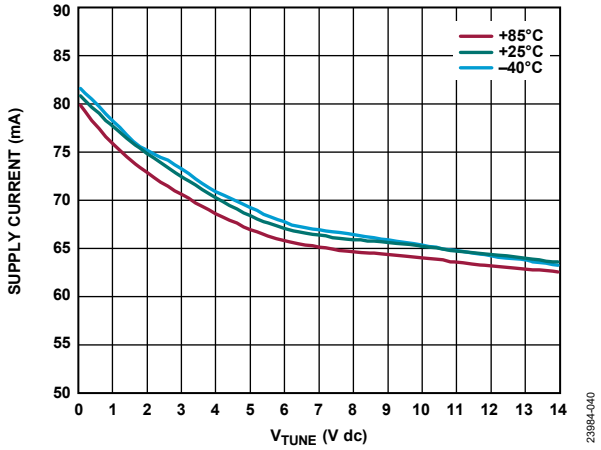

Figure 41. Supply Current vs. V_{TUNE} for Various Temperatures

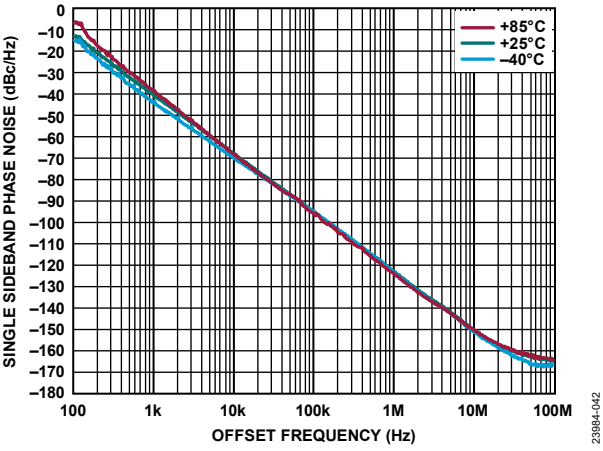

Figure 42. Single Sideband Phase Noise vs. Offset Frequency for Various Temperatures at V_{TUNE} = 5 V

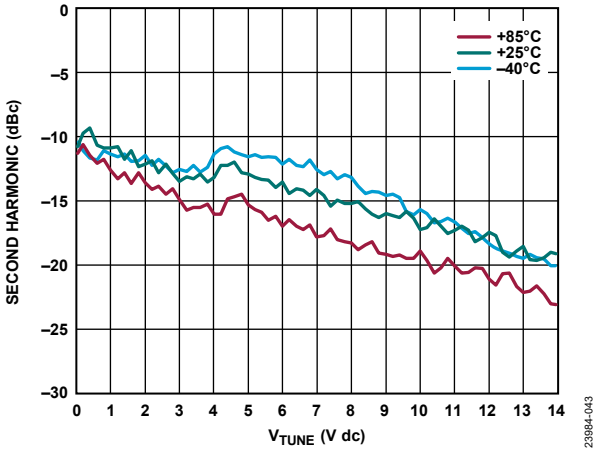

Figure 43. Second Harmonic vs. V_{TUNE} for Various Temperatures

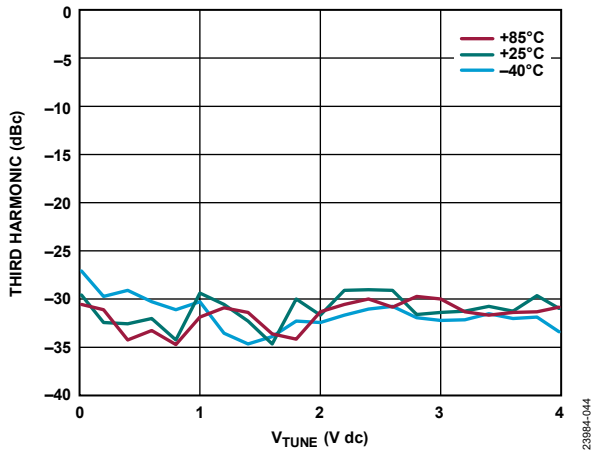

Figure 44. Third Harmonic vs. V_{TUNE} for Various Temperatures (Measurement Up to 6.5 V Only Due to Equipment Limitation)

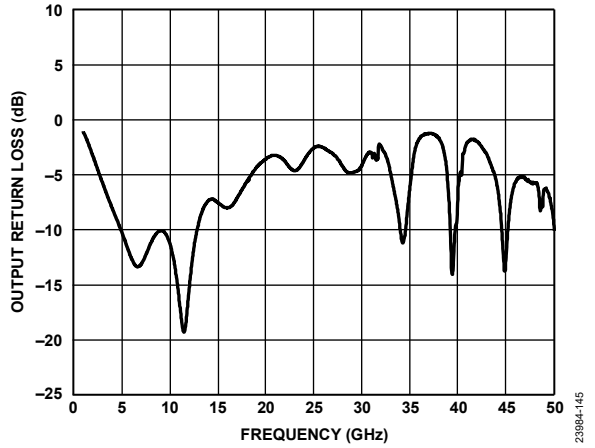

Figure 45. Output Return Loss vs. Frequency at V_{TUNE} = 7.25 V, V_{CB} = 5 V, T_A = 25°C

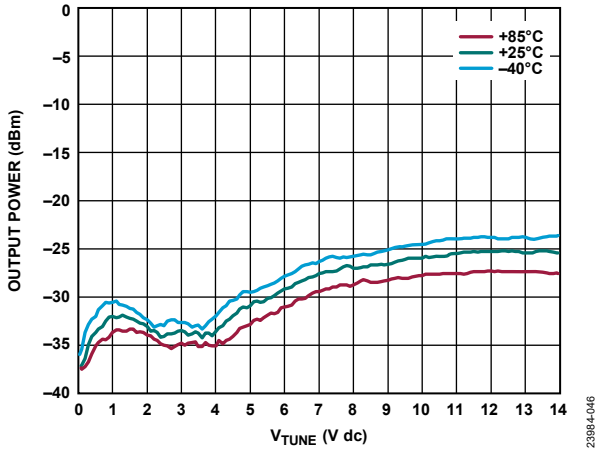

Figure 46. Output Power vs. V_{TUNE} at V_{CB} = 0 V for Various Temperatures

THEORY OF OPERATION

The HMC8362 consists of four fundamental VCOs with overlapping frequency ranges to ensure continuous frequency coverage from 11.90 GHz to 18.30 GHz over all conditions.

Using four oscillators instead of a single oscillator to span the frequency range reduces the percent bandwidth and tuning sensitivity of each oscillator, improving phase noise performance. Tuning sensitivity flatness across the frequency range is also improved and simplifies the loop filter design in synthesizer applications. The tuning sensitivity is similar across the four VCO cores, which means that the loop bandwidth and phase margin of the loop filter vary less overall vs. a single oscillator solution.

The four oscillators share a common tune port, which means that even though the active devices in the unused VCO cores are not being biased, the resonant tanks of all four VCO cores are in parallel and being tuned simultaneously. A single buffer amplifier is also shared by all four VCOs.

The upper circuitry of the buffer amplifier is biased by VCB (Pin 8). The lower portion of the buffer amplifier or VCB remains off and very little current flows until one of the VCO cores is enabled.

The lower circuitry of the buffer amplifier is enabled when the RF signal of any one of the four VCOs arrives at its input. If VCB is biased and any VCO core is enabled, current flows through the buffer amplifier and the RF signal propagates to RFOUT (Pin 5).

The buffer amplifier is designed to support only one VCO at a time. Avoid enabling more than one oscillator at a time because multiple oscillators stress the buffer amplifier enough to reduce its long-term operating life.

APPLICATIONS INFORMATION

The HMC8362 serves as the local oscillator (LO) in microwave synthesizer applications. The primary applications for this device are point to point and multipoint radios, military radars, test and measurement, industrial and medical equipment, and wireless communication infrastructure. The low phase noise allows higher orders of modulation and offers improved bit error rates in communication systems. Stable loop filter design is easily achieved due to the linear, monotonic tuning sensitivity across the four-VCO core, and higher output power minimizes the gain required to drive subsequent stages. The cascode output buffer amplifier stage guarantees stability over a wide range of output load conditions and improves the pulling performance of the VCO cores.

To achieve optimal performance of the VCO cores, including the lowest phase noise native to VCOs, high power supply rejection ratio (PSRR) and low dropout (LDO) regulators are recommended to minimize any spurious frequencies from the power supply, and to achieve the lowest phase noise native to the VCO. The ADM7150 and the LT3042 meet these requirements and are acceptable LDO regulators to use.

The wide frequency range of the VCO cores suggests the use of a low noise, PLL synthesizer, such as the ADF41513. The wide input bandwidth of the ADF41513 (1 GHz to 26.5 GHz) makes it an ideal synthesizer to be used with the HMC8362. The charge pump current can be varied up or down on the ADF41513 to compensate for VCO sensitivity variation. Many applications require actively switching between the four VCO cores as quickly as possible. Enabling more than one VCO core at a time is not recommended. Therefore, use of an appropriate 4:1 multiplexer such as the ADG1604 is recommended. The ADG1604 has low on resistance, the ability to operate with either 3 V or 5 V logic, and offers break before make switch sequencing. Alternatively, multiple ADG854 switches can also be used to enable and disable the VCO cores. Although this switch also includes a break before make delay, users must prevent the possibility of powering up more than one VCO core at a time. Regardless of which approach is used to control the VCO cores, an additional ADG854 can be used to control bias to the upper portion of the cascode amplifier circuitry for use in muting the RF output (RFOUT, Pin 5) if desired. Muting RFOUT suppresses the output power by approximately 20 dB across all cores) and does not impact long-term reliability when only one VCO core is powered up at a time.

It is important to follow optimal RF layout practices for the layout of the interconnecting circuit. Give first priority to the microwave power splitter network from the output buffer of the VCO cores to the RF input pin ($RF_{IN}A$) of the ADF41513. Give the next highest priority to the highly sensitive V_{TUNE} line with the first pole placed as close to the ADF41513 CP output pin as possible, and the final RC pole of the filter placed as close to the HMC8362 V_{TUNE} pin as possible. The wide tuning range of the HMC8362 requires the use of a high voltage, low noise, operational amplifier. The ADA4625-1 is acceptable to use for such applications.

The suggested PCB stackup consists of a high quality dielectric material, such as Rogers 4003. The transmission lines carrying the high frequency signal must be carefully controlled with 50 Ω characteristic impedances.

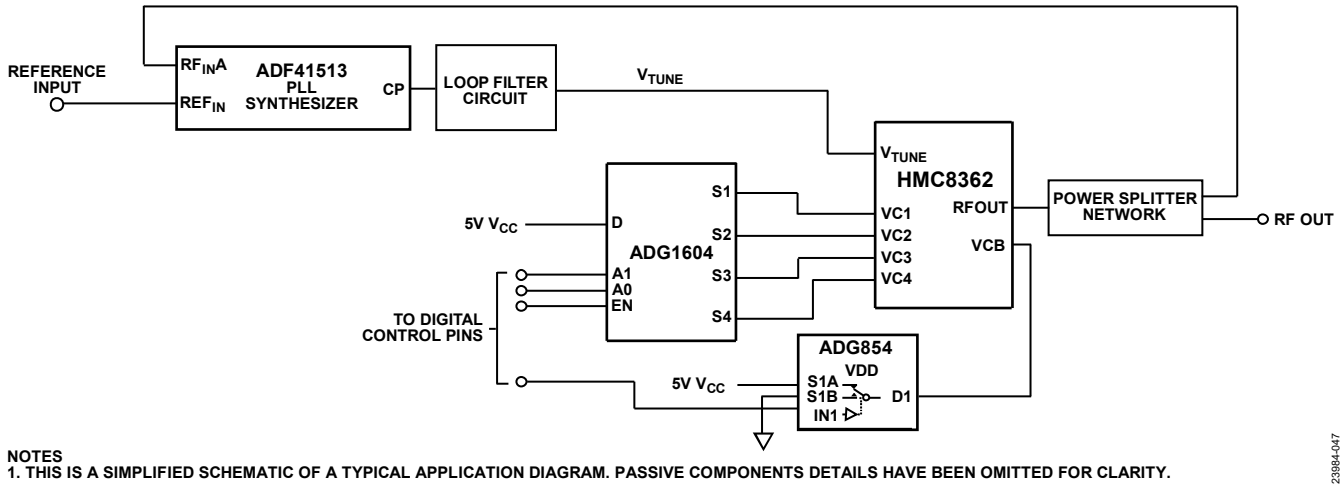

Figure 47. Typical Application Diagram

OUTLINE DIMENSIONS

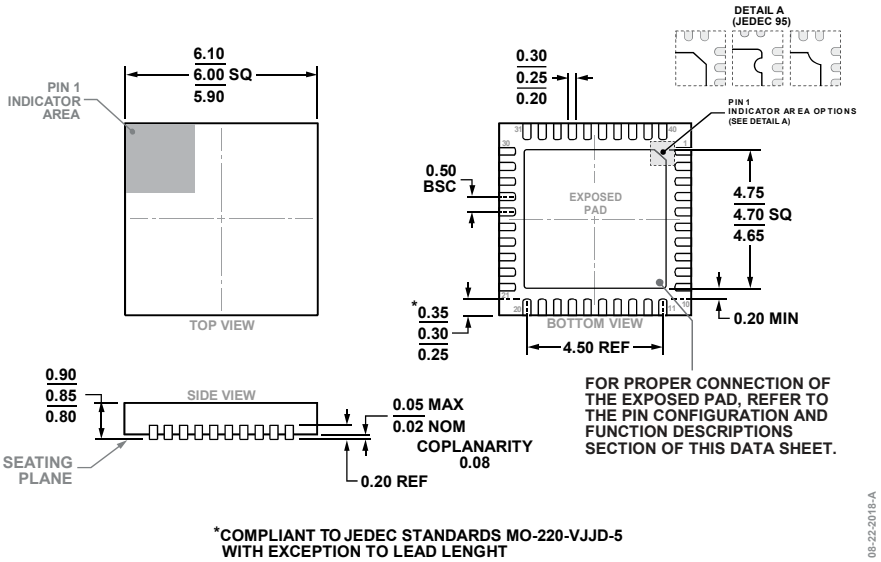

Figure 48. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.85 mm Package Height
(HCP-40-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	MSL Rating[2]	Package Description	Package Option	Ordering Quantity
HMC8362LP6GE	−40°C to +85°C	MSL3	40-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-40-1	
HMC8362LP6GETR	−40°C to +85°C	MSL3	40-Lead Lead Frame Chip Scale Package [LFCSP]	HCP-40-1	500
EV1HMC8362LP6G			Evaluation Board		

[1] All models are RoHS compliant.
[2] See the Absolute Maximum Ratings section.