

February 1994

## Multilevel Pipeline Registers

### Features

- Four 8-Bit Registers
- Hold, Transfer and Load Instructions
- Single 4-Stage or Dual-2 Stage Pipelining
- All Register Contents Available at Output
- Fully TTL Compatible
- Three-State Outputs
- High Speed, Low Power CMOS

### Applications

- Array Processor
- Digital Signal Processor
- A/D Buffer
- Telecommunication
- Byte Wide Shift Register
- Mainframe Computers

### Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE             |
|-------------|-------------------|---------------------|
| HSP9520CP   | 0°C to +70°C      | 24 Lead Plastic DIP |
| HSP9520CS   | 0°C to +70°C      | 24 Lead SOIC        |
| HSP9521CP   | 0°C to +70°C      | 24 Lead Plastic DIP |
| HSP9521CS   | 0°C to +70°C      | 24 Lead SOIC        |

### Description

These devices are multilevel pipeline registers implemented using a low power CMOS process. They are pin for pin compatible replacements for industry standard multilevel pipeline registers such as the L29C520 and L29C521. The HSP9520 and HSP9521 are direct replacements for the AM29520 and AM29521 and WS59520 and WS59521.

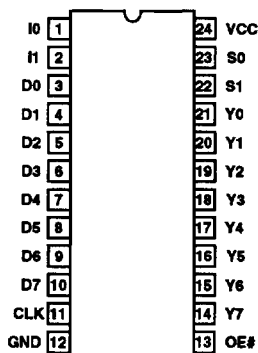
They consist of four 8-bit registers which are dual ported. They can be configured as a single four level pipeline or a dual two level pipeline. A single 8-bit input is provided, and the pipelining configuration is determined by the instruction code input to the I0 and I1 inputs (see instruction control).

The contents of any of the four registers is selectable at the multiplexed outputs through the use of the S0 and S1 multiplexer control inputs (see register select). The output is 8-bits wide and is three-stated through the use of the OE# input.

The HSP9520 and HSP9521 differ only in the way data is loaded into and between the registers in dual two-level operation. In the HSP9520 when data is loaded into the first level the existing data in the first level is moved to the second level. In the HSP9521 loading the first level simply causes the current data to be overwritten. Transfer of data to the second level is achieved using the single four level mode (I1, I0 = '0'). This instruction also causes the first level to be loaded. The HOLD instruction (I1, I0 = '1') provides a means of holding the contents of all registers.

### Pinout

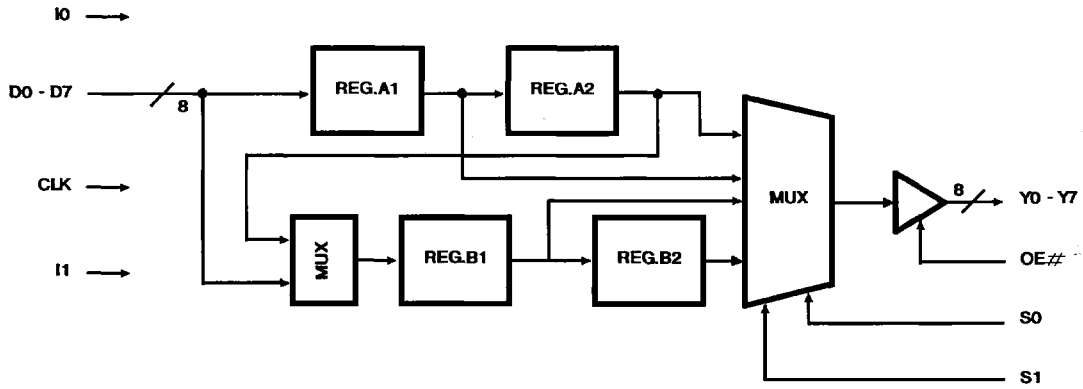
HSP9520, HSP9521 (24 PIN SOIC, NPDIP)  
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.  
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File Number 2811.4

**Block Diagram**



**Pin Descriptions**

| NAME   | DIP PIN | TYPE | DESCRIPTION   |
|--------|---------|------|---|
| VCC    | 24      |      | The +5V power supply pin. A 0.1µF capacitor between the VCC and GND pin is recommended.   |
| GND    | 12      |      | The device ground.  |
| CLK    | 11      | I    | Input Clock. Data is latched on the low to high transition of this clock signal. Input setup and hold times with respect to the clock must be met for proper operation.   |
| D0-7   | 3-10    | I    | Data Input Port. These inputs are used to supply the 8 bits of data which will be latched into the selected register on the next rising clock edge.   |
| Y0-7   | 21-14   | O    | Data Output Port. This 8-bit port provides the output data from the four internal registers. They are provided in a multiplexed fashion, and are controlled via the multiplexer control inputs (S0 and S1).   |
| I0, I1 | 1, 2    | I    | Instruction Control Inputs. These inputs are used to provide the instruction code which determines the internal register pipeline configuration. Refer to the Instruction Control Table for the specific codes and their associated configurations.                       |
| S0, S1 | 23, 22  | I    | Multiplexer Control Inputs. These inputs select which of the four internal registers' contents will be available at the output port. Refer to the Register Select Table for the codes to select each register.  |
| OE#    | 13      | I    | Output Enable. This input controls the state of the output port (Y0-Y7). A LOW on this control line enables the port for output. When OE# is HIGH, the output drivers are in the high impedance state. Internal latching or transfer of data is not affected by this pin. |

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SPECIAL  
FUNCTION

## Specifications HSP9520/HSP9521

### Absolute Maximum Ratings

|   |                              |
|---|------------------------------|
| Supply Voltage .....                            | +8.0V                        |
| Input or Output Voltage Applied .....           | GND -0.5V to $V_{CC} + 0.5V$ |
| Storage Temperature Range .....                 | -65°C to +150°C              |
| Junction Temperature .....                      | +150°C                       |
| Lead Temperature (Soldering, Ten Seconds) ..... | +300°C                       |

### Operating Conditions

|   |                                 |
|---|---------------------------------|
| Operating Voltage Range .....           | +4.75V to +5.25V                |
| Operating Temperature Range .....       | 0°C to +70°C                    |
| Reliability Information                 |                                 |
| $\theta_{ja}$ .....                     | 51.4°C/W (DIP), 77.0W/°C (SOIC) |
| $\theta_{jc}$ .....                     | 22.3°C/W (DIP), 23.2W/°C (SOIC) |
| Maximum Package Power Dissipation ..... | 1.5W (DIP), 1.0W (SOIC)         |

### D.C. Electrical Specifications ( $V_{CC} = 5.0V \pm 5\%$ , $T_A = 0^\circ C$ to $+70^\circ C$ )

| PARAMETER                      | SYMBOL     | MIN | MAX | UNITS   | TEST CONDITIONS  |
|--------------------------------|------------|-----|-----|---------|--|
| Logical One Input Voltage      | $V_{IH}$   | 2.0 | -   | V       | $V_{CC} = 5.25V$   |
| Logical Zero Input Voltage     | $V_{IL}$   | -   | 0.8 | V       | $V_{CC} = 4.75V$   |
| Output HIGH Voltage            | $V_{OH}$   | 2.4 | -   | V       | $I_{OH} = -6.5mA$ , $V_{CC} = 4.75V$   |
| Output LOW Voltage             | $V_{OL}$   | -   | 0.5 | V       | $I_{OL} = +20.0mA$ , $V_{CC} = 4.75V$  |
| Input Leakage Current          | $I_I$      | -10 | 10  | $\mu A$ | $V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$   |
| Output Leakage Current         | $I_O$      | -10 | 10  | $\mu A$ | $V_{OUT} = V_{CC}$ or GND<br>$V_{CC} = 5.25V$                                      |
| Standby Power Supply Current   | $I_{CCSB}$ | -   | 500 | $\mu A$ | $V_{IN} = V_{CC}$ or GND<br>$V_{CC} = 5.25V$ Outputs Open                          |
| Operating Power Supply Current | $I_{CCOP}$ | -   | 12  | mA      | $f = 5.0MHz$ , $V_{IN} = V_{CC}$ or GND<br>$V_{CC} = 5.25V$ , Outputs Open, Note 1 |

### Capacitance ( $T_A = +25^\circ C$ , Note 3)

| PARAMETER          | SYMBOL   | MIN | MAX | UNITS | TEST CONDITIONS  |
|--------------------|----------|-----|-----|-------|--|
| Input Capacitance  | $C_{IN}$ | -   | 12  | pF    | FREQ = 1 MHz, $V_{CC} =$ Open, all measurements are referenced to device ground. |
| Output Capacitance | $C_O$    | -   | 12  | pF    |  |

### A.C. Electrical Specifications ( $V_{CC} = 5.0V \pm 5\%$ , $T_A = 0^\circ C$ to $+70^\circ C$ , Note 2)

| PARAMETER                    | SYMBOL     | MIN | MAX | UNITS | TEST CONDITIONS (Note 2) |
|------------------------------|------------|-----|-----|-------|--------------------------|
| Clock to Data Out            | $T_{PD}$   | -   | 21  | ns    |                          |
| Mux Select to Data Out       | $T_{SELD}$ | -   | 20  | ns    |                          |
| Input Setup Time (D0-7/I0-7) | $T_S$      | 10  | -   | ns    |                          |
| Input Hold Time (D0-7/I0-7)  | $T_H$      | 3   | -   | ns    |                          |
| Output Enable Time           | $T_{ENA}$  | -   | 20  | ns    |                          |
| Output Disable Time          | $T_{DIS}$  | -   | 13  | ns    | Note 3                   |
| Clock Pulse Width            | $T_{PW}$   | 10  | -   | ns    |                          |

#### NOTES:

- Power supply current is proportional to frequency. Typical rating for  $I_{CCOP}$  is 2.4mA/MHz.
- A.C. Testing is performed as follows: Input levels: 0V and 3.0V, Timing reference levels = 1.5V, Input rise and fall times driven at 1ns/V, Output load  $C_L = 40pF$ .
- Controlled by design or process parameters and not directly tested. Characterized upon initial design and after major design and/or process changes.

Timing Waveform

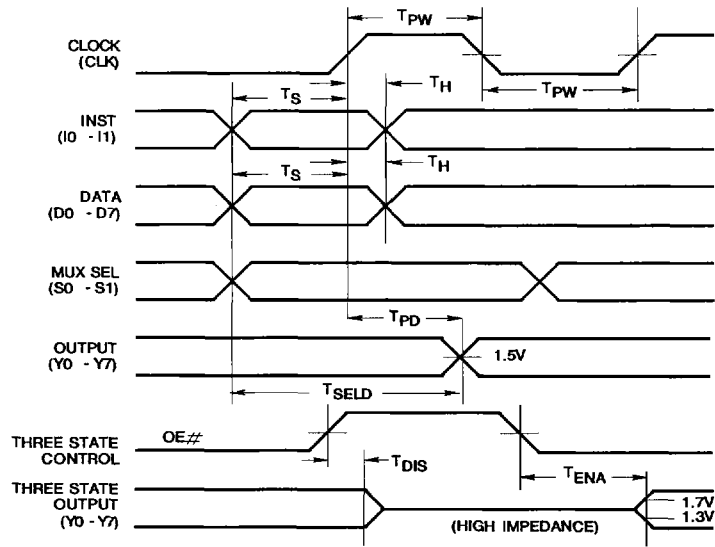


TABLE 1. INSTRUCTION CONTROL

| I1 | I0 | '9520              | '9521              |
|----|----|--------------------|--------------------|
| 0  | 0  |                    |                    |
| 0  | 1  |                    |                    |
| 1  | 0  |                    |                    |
| 1  | 1  | ALL REGISTERS HOLD | ALL REGISTERS HOLD |

TABLE 2. REGISTER SELECT

| S1 | S0 | '9520 OR '9521 |
|----|----|----------------|
| 0  | 0  | B2             |
| 0  | 1  | B1             |
| 1  | 0  | A2             |
| 1  | 1  | A1             |

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