TPS7A1601EVM-046

This user's guide describes operational use of theTPS7A1601EVM-046 evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7A1601, low-dropout (LDO) linear regulator. Included in this user's guide are setup instructions, a schematic diagram, layout and thermal guidelines, a bill of materials, and test results.

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PowerPAD is a trademark of Texas Instruments.

1 Introduction

The Texas Instruments TPS7A1601EVM-046 evaluation module helps design engineers to evaluate the operation and performance of the TPS7A16xx family of linear regulators for use in their own circuit applications. This particular EVM configuration contains a single linear regulator with internal thermal and current-limit shutdowns. The TPS7A1601 also has enable (disable), PG (Power Good), and user-programmable PG circuitry in an extremely small DGN (MSOP-8) PowerPAD™ package. The regulator, including external components, is capable of delivering up to 100 mA to the load depending on the input/output power dissipation across the part. The TPS7A16xx does not require an input capacitor, and the output capacitor only needs to be ≥ 2.2 μF (effective minimum) for stability; however, for conservative design practice accounting for widely varying noise environments and dynamic line/load conditions, a 1-μF input capacitor and a 0.01-μF feedforward capacitor have been used in the design.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7A1601EVM.

2.1 Input/Output Connectors and Jumper Descriptions

2.1.1 J1 – VIN

J1 is the input power supply voltage connector. Twist the positive input lead and ground return lead from the input power supply, and keep them as short as possible to minimize EMI transmission. Add additional bulk capacitance between J1 and J2 if the supply leads are greater than 6 inches. For example, an additional 47-μF electrolytic capacitor connected from J1 to ground can improve the transient response of the TPS7A1601, while eliminating unwanted ringing on the input due to long-wire connections.

2.1.2 J2 – GND

J2 is the ground-return connector for the input power supply.

2.1.3 J3 – GND

J3 is the output ground-return connector

2.1.4 J4 – VOUT

J4 is the regulated output voltage connector.

2.1.5 JP1 – EN

SP1 is the output enable. To enable the output, connect a jumper to short the ON pin 1 to the EN center pin 2. To disable the output, connect a jumper to short EN pin 2 to OFF pin 3.

2.1.6 J5 – PG

J5 is Power Good. If a jumper is installed across J5, the PG signal is pulled up to Vout and the signal can be monitored via TP1 (test point 1). The user can also pull up the signals themselves by connecting directly to pin 1 of J5. The maximum pullup voltage that can be used on the PG pin is 5.5 V.

2.1.7 J6– Input Diode Bypass

The EVM is populated with a 100-V, 300-mA protection diode on the input. This diode can be bypassed by connecting a jumper across J6.

2.2 Equipment Setup

- Turn off the input power supply after verifying that its output voltage is set to greater than 6 V (60 V maximum). Connect the positive voltage lead from input power supply to VIN at the J1 connector of the EVM. Connect the ground lead from the input power supply to GND at the J2 connector of the EVM.

- Connect a 0-A to 100-mA load between an OUT pin at connector J4, and a GND pin at connector J3.
- Disable the output by connecting the jumper on JP1 from the EN pin to the OFF pin.

3 Operation

- Turn on the input power supply. For initial operation, set the input power supply, VIN – J1, to 10 V
- Enable the output by reconnecting the jumper on JP1 from the EN pin to the ON pin.
- Vary the respective loads and VIN voltages as necessary for test purposes.

4 Test Results

This section provides typical performance waveforms for the TPS7A1601EVM-046 printed-circuit board.

4.1 Turnon Sequence

Figure 1 shows the turnon/off characteristic where VIN is preset to 10 V, the output drives full load, and the EN turnon is stepped to 10 V (C2, red). The output soft start (C1, yellow) shows a monotonic rise time of approximately 60 ms. The output voltage start-up ramp is not load dependant.

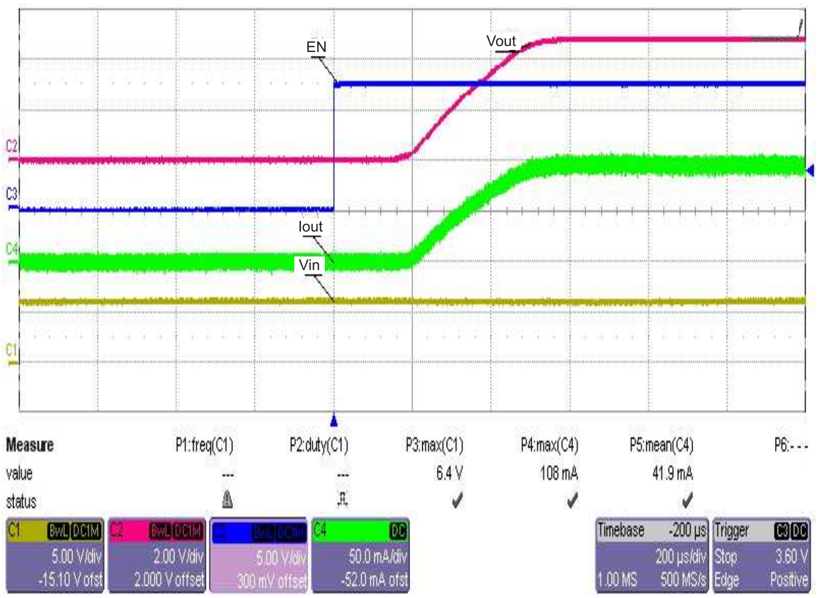

Figure 1. Turnon Sequence

4.2 Output Load Transient

Figure 2 shows the load transient response (OUT – C1, yellow) for a full-load step transient from 10 mA to 100 mA (C4, green). VIN is set at 10 V.

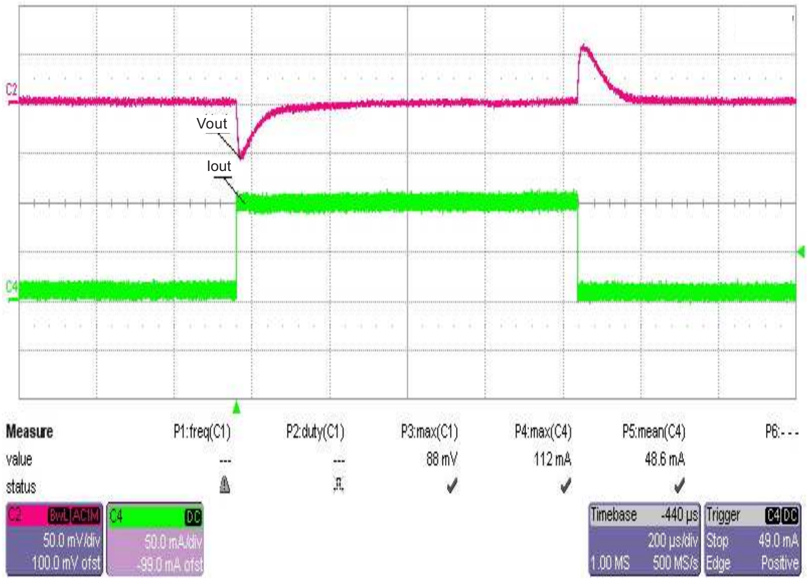

Figure 2. Load Step and Transient Response

4.3 Power Good

Figure 3 shows the operation of the Power Good (PG) output. Vin (6 V) is present and the chip is enabled (c1, gold) The PG output (C3, blue) goes HIGH approximately 1.5 ms after Vout (C2, red) goes into regulation.

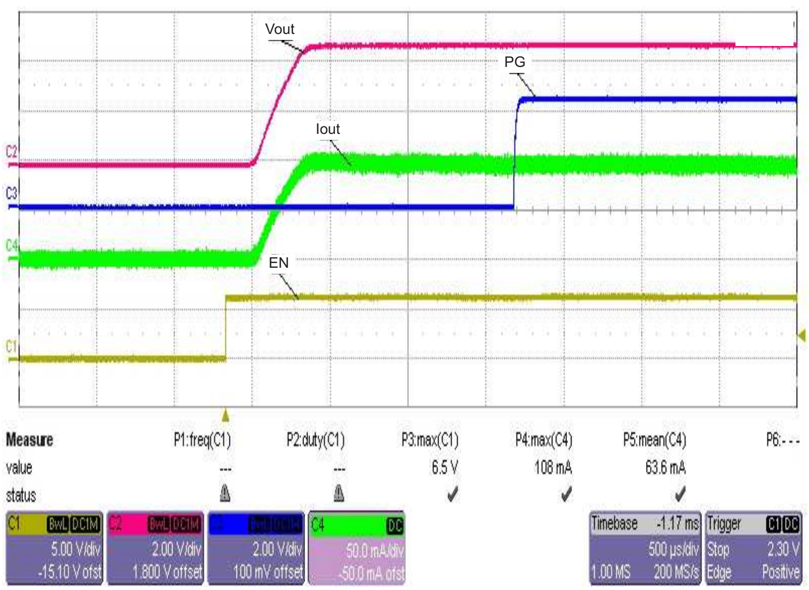

Figure 3. Power Good Operation

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key component of design for any power converter and is especially important when the power dissipation in the LDO regulator is high. Use the following formula to approximate the maximum power dissipation for the particular ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA}$$

Where T_J is the junction temperature, T_A is the ambient temperature, P_D is the power dissipation in the device (W), and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius. The maximum silicon junction temperature, T_J, must not be allowed to exceed 150°C. The layout design must use copper trace and plane areas effectively, as thermal sinks, in order not to allow T_J to exceed the absolute maximum rating under all temperature conditions and voltage conditions across the part.

The designer must consider carefully the thermal design of the PCB for optimal performance over temperature. For this EVM, Figure 5 shows that the PCB top GND plane has six, 6-mil, thermal via connections to the bottom-side copper GND plane to dissipate heat. The PCB is a two-layer board with 2-oz. copper on top and bottom layers. The DGN package drawing can be found at the Texas Instruments Web site in the product folder for the TPS7A16xx LDO linear regulator.

Table 1 repeats information from the Dissipation Ratings Table of the TPS7A16xx data sheet for comparison with the thermal resistance, θ_{JA}, calculated for this EVM layout to show the wide variation in thermal resistances for given copper areas. The High-K value is determined using a standard JEDEC High-K (2s2p) board having dimensions of 3-inch x 3-inch with 1-oz internal power and ground planes and 2-oz copper traces on top and bottom of the board.

Table 1. Thermal Resistance, θ_{JA}, and Maximum Power Dissipation

Board	Package	θ_{JA}	Max Dissipation without Derating (T_A = 25°C)	Max Dissipation without Derating (T_A = 70°C)
High-K	DGN	55.09°C/W	1.8 mW	998 mW
TPS7A1601EVM-046	DGN	38.89°C/W	2.57 W	1.41.W

The thermal resistance for the TPS7A1601EVM-046, θ_{JA}, is the measured value for this particular layout scheme. The maximum power dissipation is proportional to the volume of copper volume connected to the package.

6 Board Layout

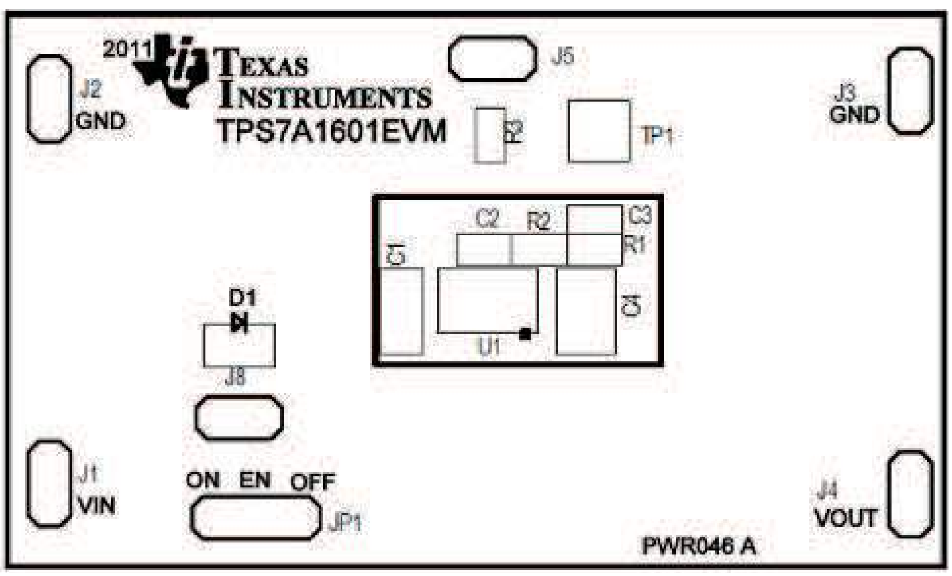

Figure 4. Top-Layer Silkscreen

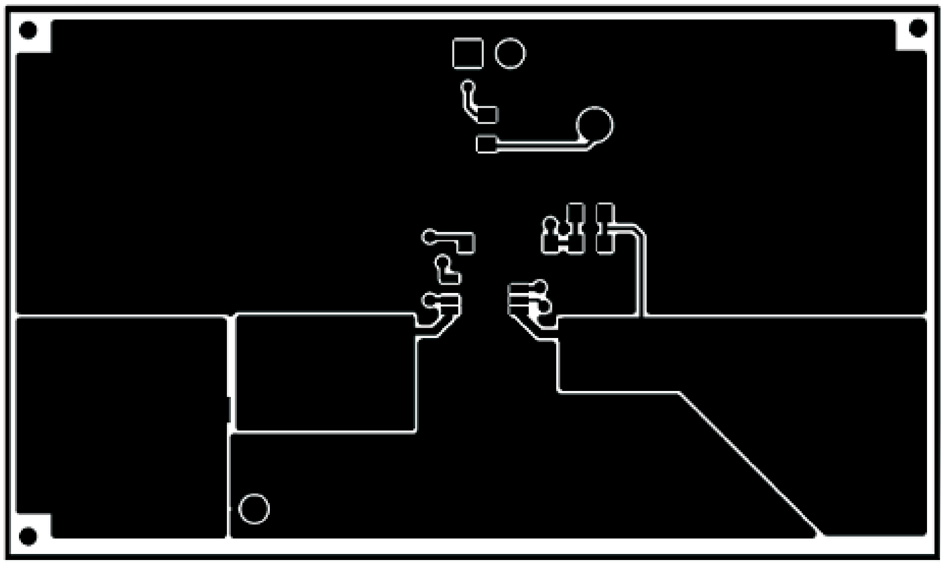

Figure 5. Top-Layer Routing

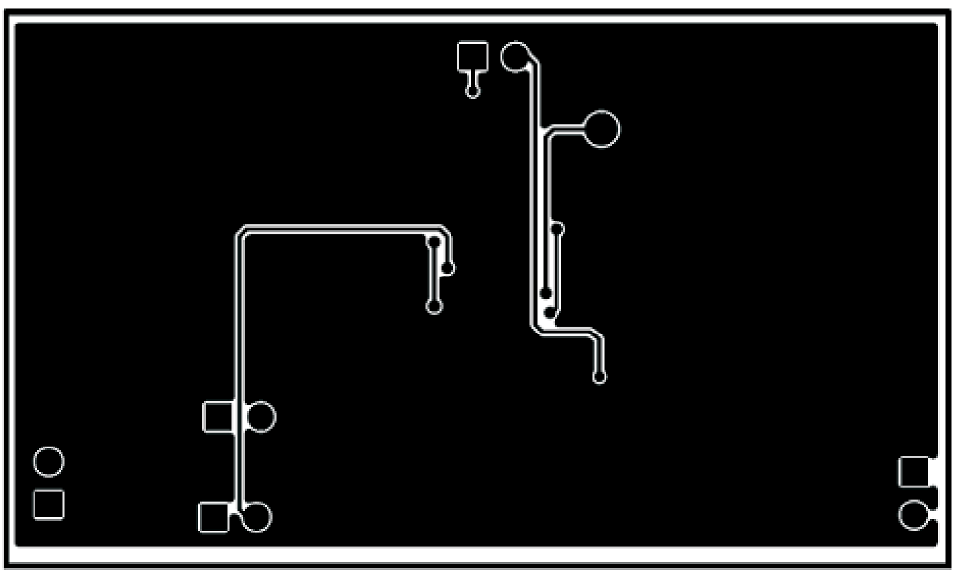

Figure 6. Bottom-Layer Routing

7 Schematic and Bill of Materials

7.1 Schematic

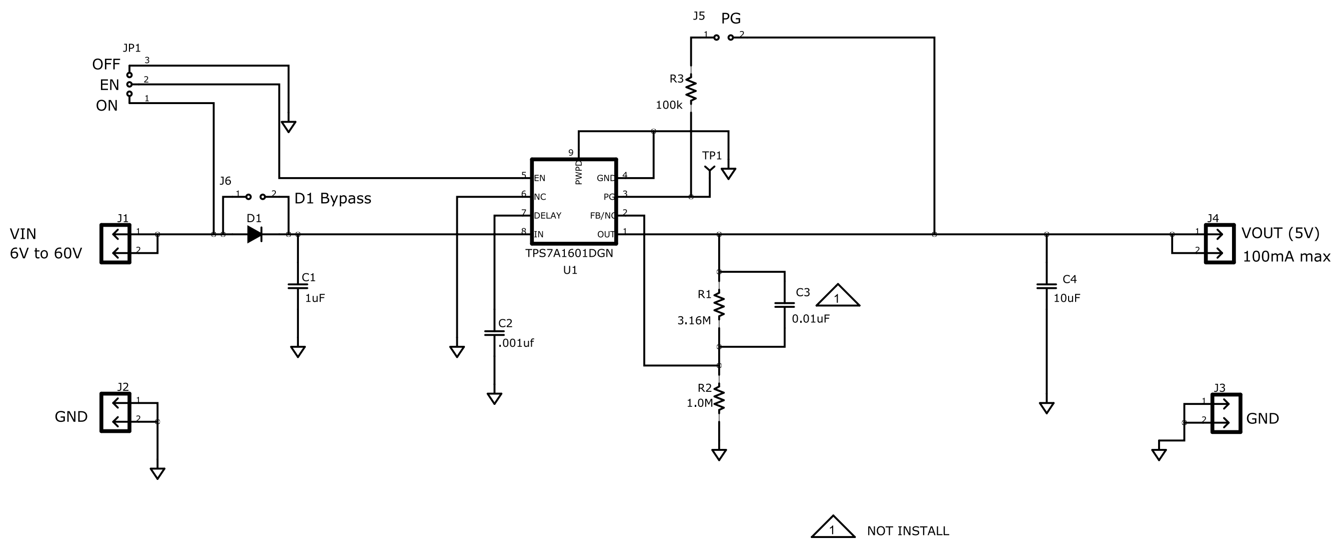

Figure 7. TPS7A1601EVM-046 Schematic

7.2 Bill of Materials

Table 2. TPS7A1601EVM-046 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	1.0uF	Capacitor, Ceramic, 100V, X7R, 10%	C1206	STD	STD
1	C2	0.001uF	Capacitor, Ceramic,100V	603	STD	STD
1	C3	0.01uF	Capacitor, Ceramic, Low Inductance, 50V, X7R, 10%	603	STD	STD
1	C4	10.0uF	Capacitor, Ceramic, 50V, X7R, 10%	1210	STD	STD
1	R1	3.16M	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	R2	1.0M	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	R3	100K	Resistor, Chip, 1/16W, 1%	603	STD	STD
1	D1	1N4148WS0	Diode, Small Signal, 300-mA, 100V	SOD-323	1N4148WS	Fairchild
2	J5, J8	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
4	J1–J4	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 inch x 2	PEC02SAAN	Sullins
1	JP1	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	U1	TPS7A1601DGN	IC, 60 V, 5 µA Iq LDO, 100mA Linear Regulator	HTSSOP	TPS7A1601DGN	TI
1	TP1	5000	Test Point, Red, Thru Hole Color Keyed	0.100 x 0.100 inch	5000	Keystone

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During normal operation, some circuit components may have case temperatures greater than 100° C. The EVM is designed to operate properly with certain components above 100° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user’s sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

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Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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This Class A or B digital apparatus complies with Canadian ICES-003.

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Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

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Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
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3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM’s electronic components and packing materials.

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