

Features

- Synchronizes to any Telecom ($N * 8 \text{ kHz}$) or any Synchronized Ethernet (SyncE) frequency.
- Generates any Telecom or SyncE frequency independent of the input frequency rate
- Uses proprietary DPLL technology to guarantee a stable synchronization path over any combination of input and output ratios and frequencies
- Provides input reference jitter filtering with programmable loop bandwidth in the range of 14 Hz to 896 Hz
- Supports two input references, each configurable as single ended LVCMOS (up to 177.5 MHz) or differential LVPECL (up to 750 MHz)
- Automatic hitless reference switching and stand-by mode on reference fail
- Digital PLL (DPLL) and high speed clock synthesis engine for generating high speed PHY clocks
- Provides four high performance differential LVPECL outputs with maximum speed up to 750 MHz with jitter below 0.7 psec RMS
- Provides 2 high performance single ended LVCMOS outputs with maximum speed of 177.5 MHz with jitter below 1.3 psec RMS

Ordering Information

ZL30158GGG	64 Pin LBG A	Trays
ZL30158GGG2	64 Pin LBG A*	Trays

*Pb Free Tin/Silver/Copper
-40°C to +85°C

- Operates from a single crystal resonator or crystal oscillator
- Configurable using a simple SPI/I²C interface

Applications

- Clock Generation for Physical Line Interface:
 - Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
 - SONET/SDH, OC-192/OC-48
 - 100 BaseX, GE, Fibre channel
- Clock Generation and Distribution for back plane Interface:
 - TDM, Telecom Bus, Utopia, SBI
 - XAUI

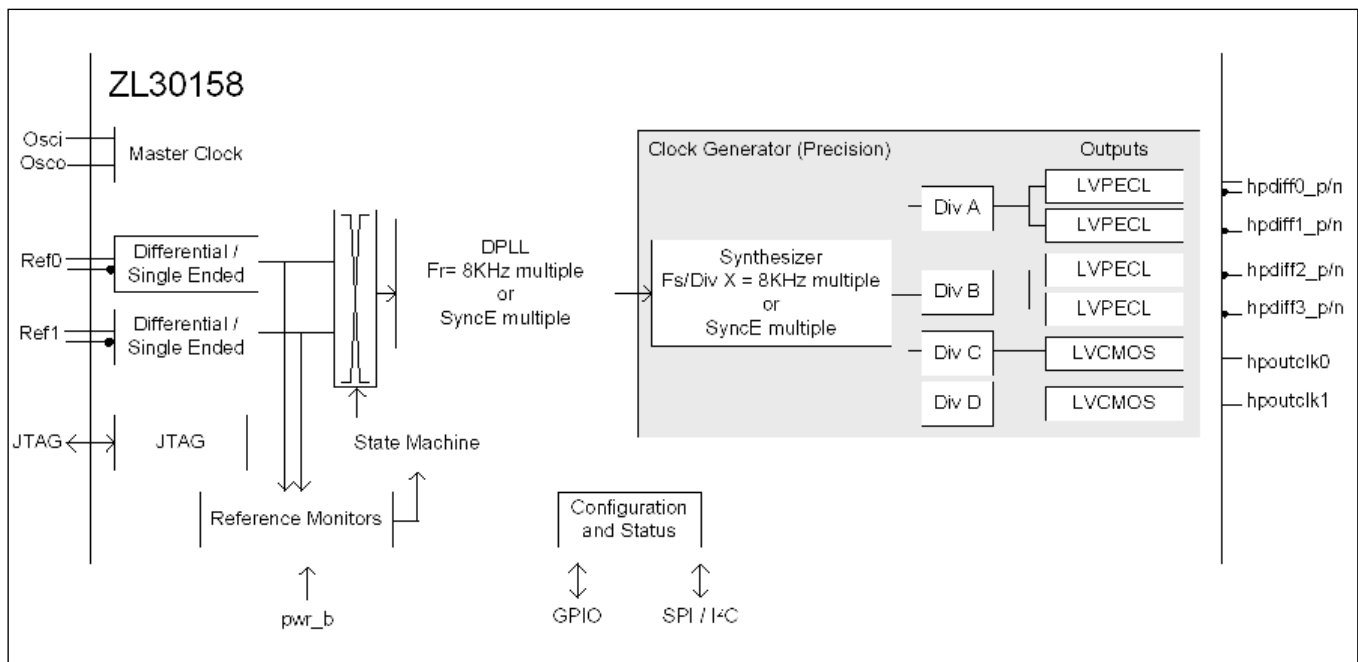
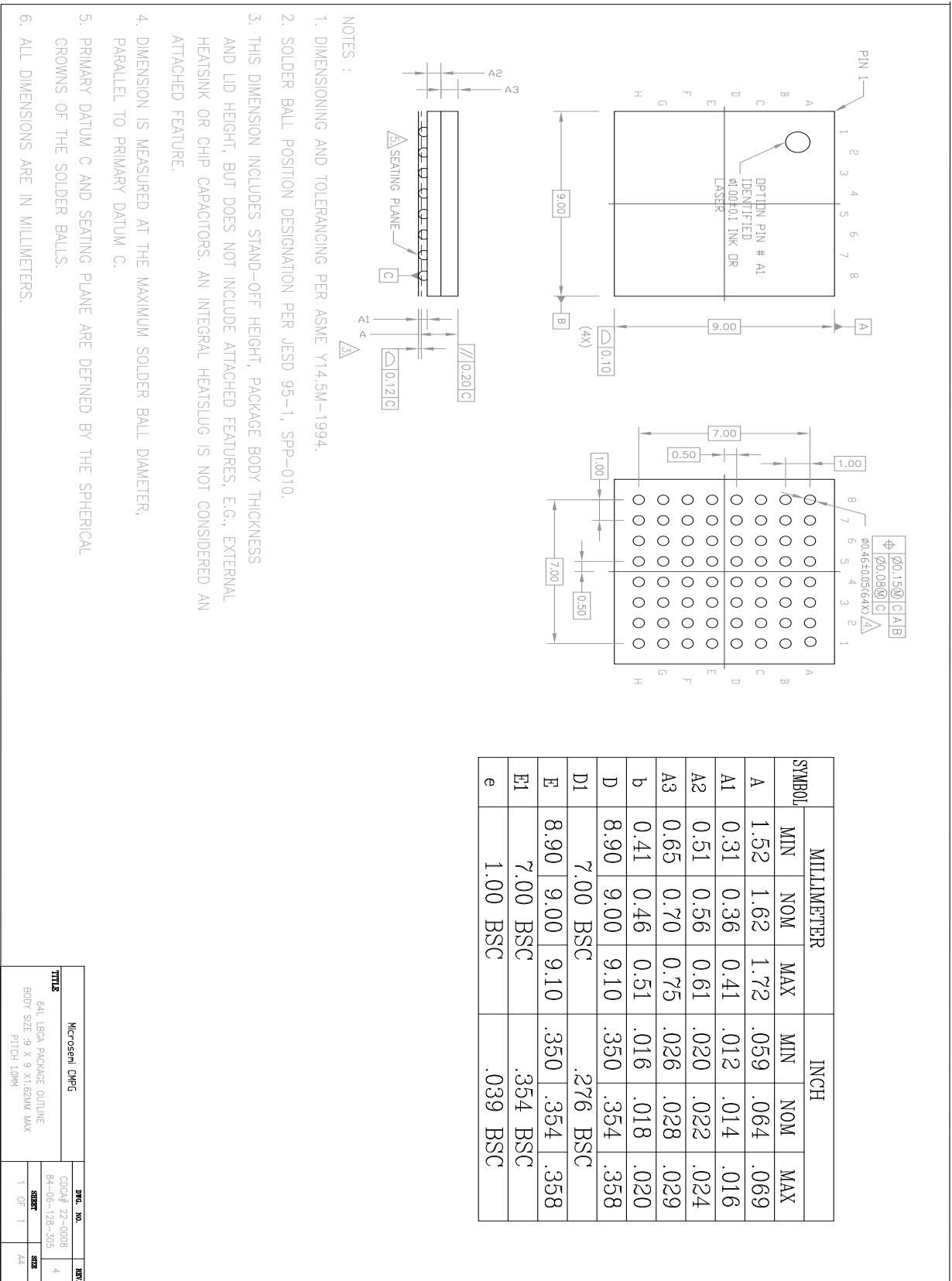


Figure 1 - Functional Block Diagram

Mechanical Drawing



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