FAIRCHILD SEMICONDUCTOR®

January 2009

UniFET™

FDD5N53/FDU5N53

N-Channel MOSFET

530V, 4A, 1.5Ω

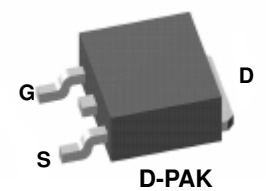
Features

- $R_{DS(on)}$ = 1.25Ω (Typ.)@ V_{GS} = 10V, I_D = 2A
- Low gate charge (Typ. 11nC)
- Low C_{rss} (Typ. 5pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

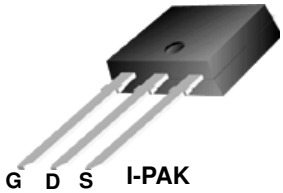
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

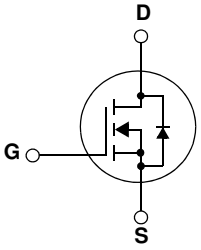
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pluse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power suppliesand active power factor correction.



D-PAK
FDD Series



I-PAK
FDU Series



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter			FDD5N53/FDU5N53	Units
V_{DSS}	Drain to Source Voltage			530	V
V_{GSS}	Gate to Source Voltage			±30	V
I_D	Drain Current	-Continuous (T_C = 25°C)		4	A
		-Continuous (T_C = 100°C)		2.4	
I_{DM}	Drain Current	- Pulsed	(Note 1)	16	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	256	mJ
I_{AR}	Avalanche Current		(Note 1)	4	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	4	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)		40	W
		- Derate above 25°C		0.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	110	

Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD5N53	FDD5N53TM	D-PAK	380mm	16mm	2500
FDD5N53	FDD5N53TF	D-PAK	380mm	16mm	2000
FDU5N53	FDU5N53TU	I-PAK	-	-	70

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_J = 25^oC$	530	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.6	-	$V/^oC$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 530V$, $V_{GS} = 0V$	-	-	1	μA
		$V_{DS} = 424V$, $T_C = 125^oC$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 2A$	-	1.25	1.5	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40V$, $I_D = 2A$ (Note 4)	-	4.3	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz	-	480	640	pF
C_{oss}	Output Capacitance		-	66	88	pF
C_{rss}	Reverse Transfer Capacitance		-	5	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400V$, $I_D = 5A$, $V_{GS} = 10V$ (Note 4, 5)	-	11	15	nC
Q_{gs}	Gate to Source Gate Charge		-	3	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	5	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250V$, $I_D = 5A$, $R_G = 25\Omega$ (Note 4, 5)	-	13	36	ns
t_r	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	28	66	ns
t_f	Turn-Off Fall Time		-	20	50	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	16	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 4A$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 5A$, $dI_F/dt = 100A/\mu s$ (Note 4)	-	300	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.8	-	μC

Notes:
1: Repetitive Rating: Pulse width limited by maximum junction temperature
2: L = 32mH, $I_{AS} = 4A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$
3: $I_{SD} \le 4A$, $di/dt \le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25°C$
4: Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

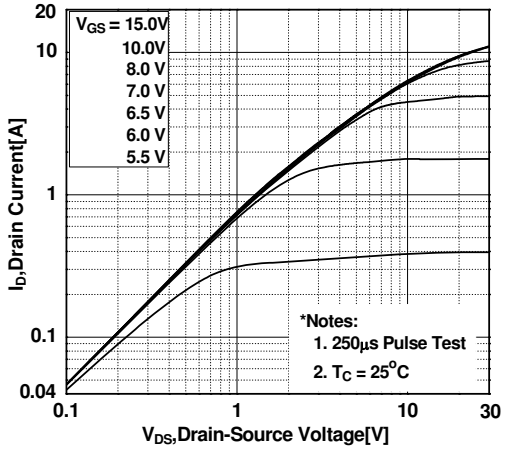


Figure 2. Transfer Characteristics

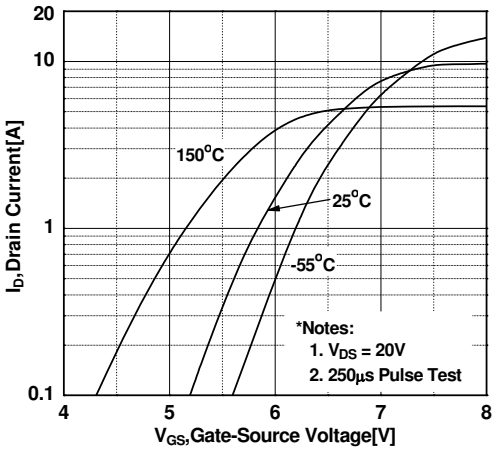


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

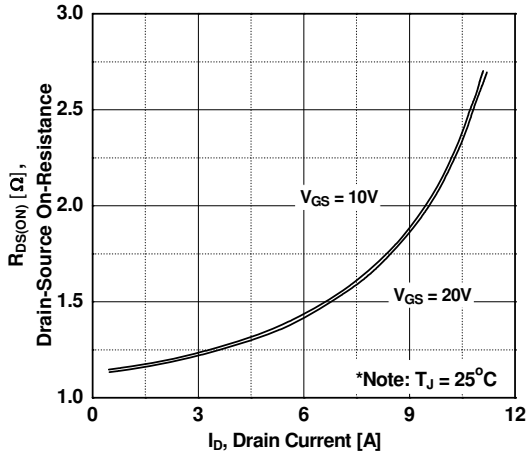


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

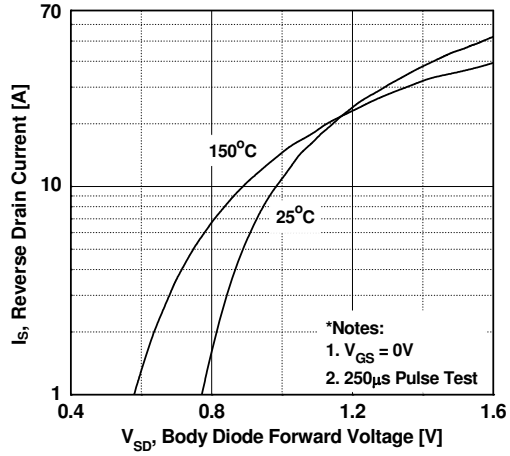


Figure 5. Capacitance Characteristics

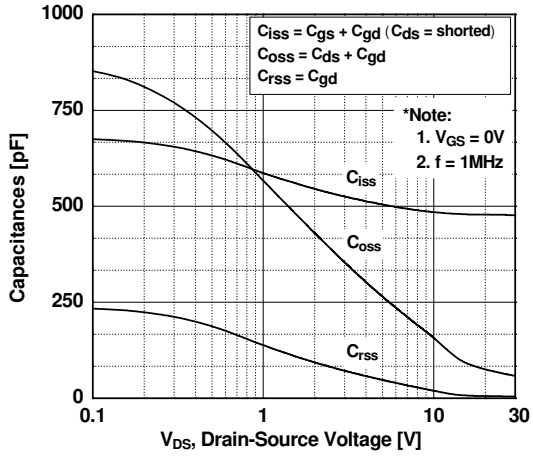
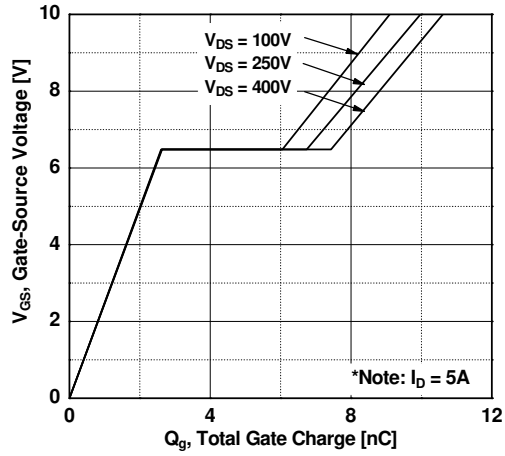


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

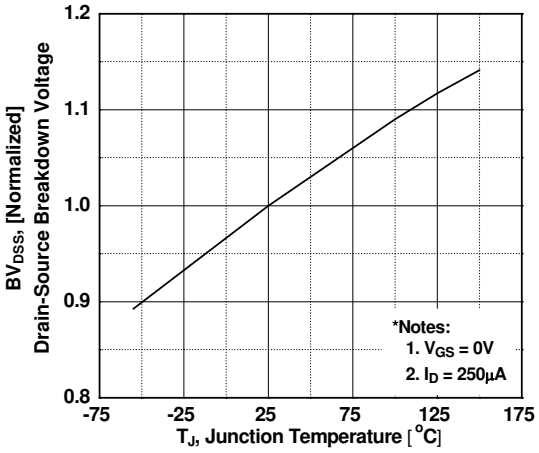


Figure 8. On-Resistance Variation vs. Temperature

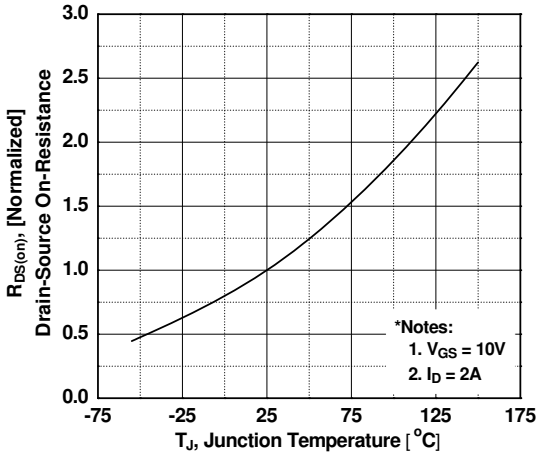


Figure 9. Maximum Safe Operating Area

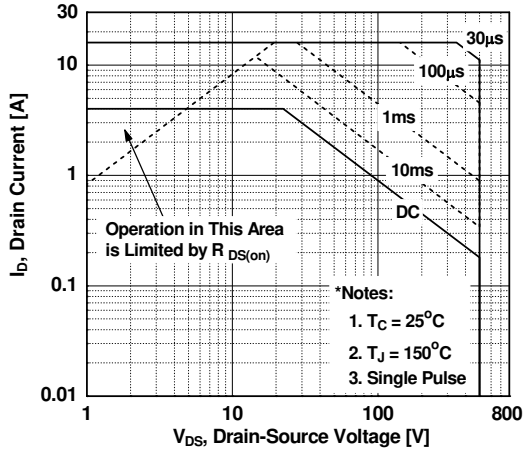


Figure 10. Maximum Drain Current vs. Case Temperature

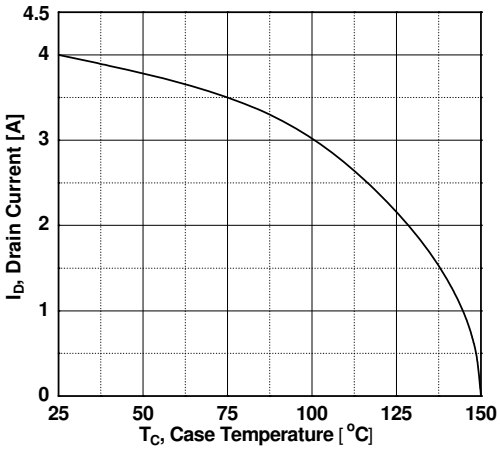
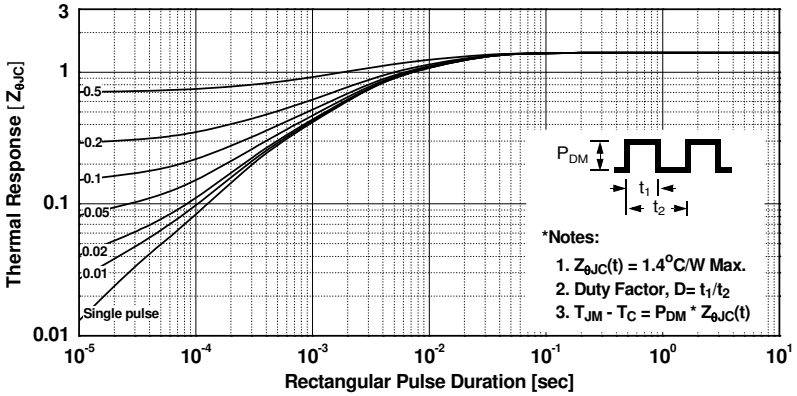
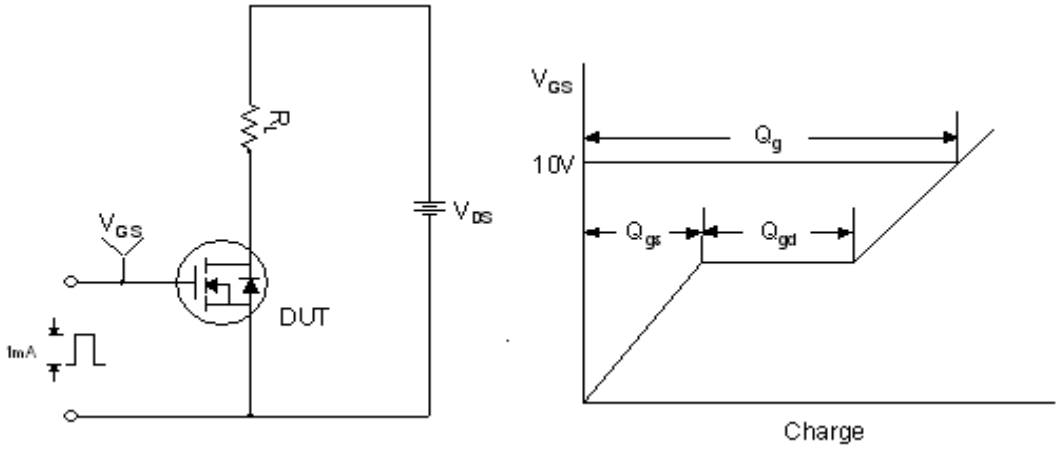


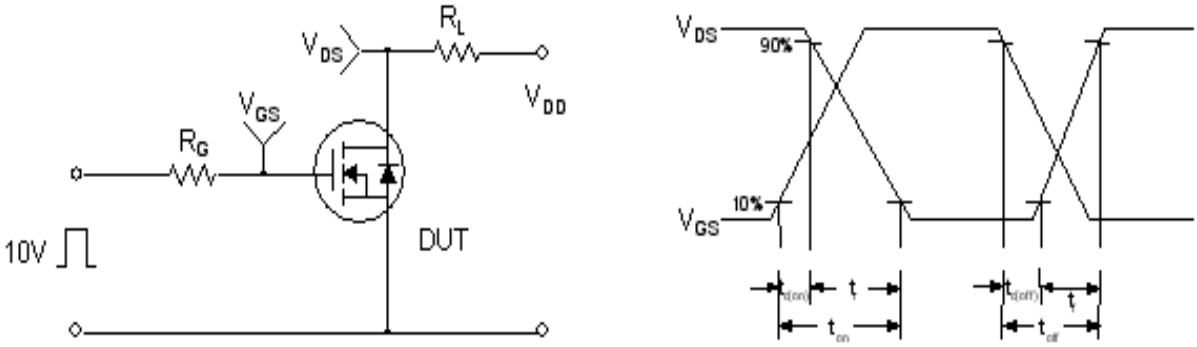
Figure 11. Transient Thermal Response Curve



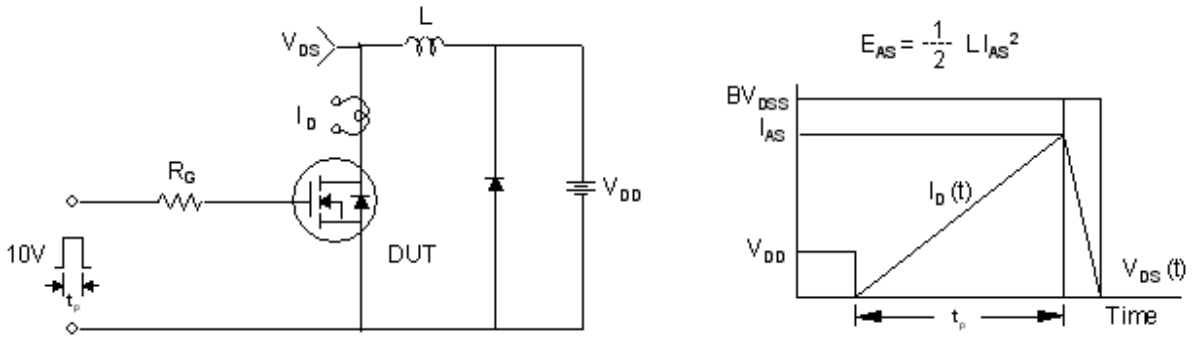
Gate Charge Test Circuit & Waveform



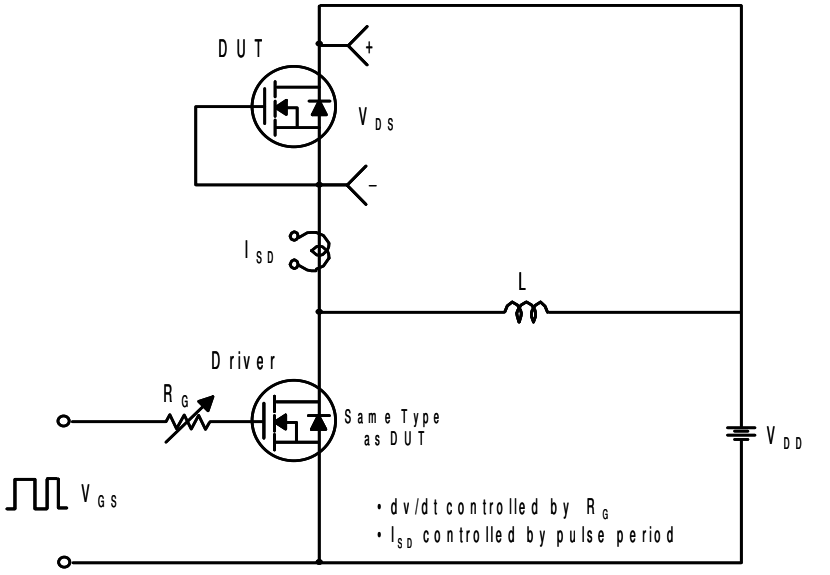
Resistive Switching Test Circuit & Waveforms

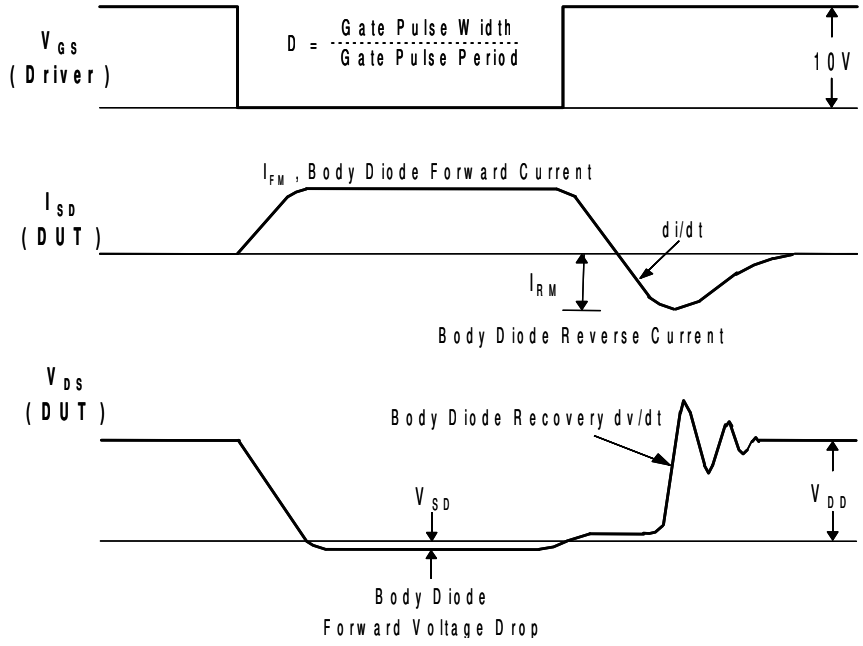


Unclamped Inductive Switching Test Circuit & Waveforms



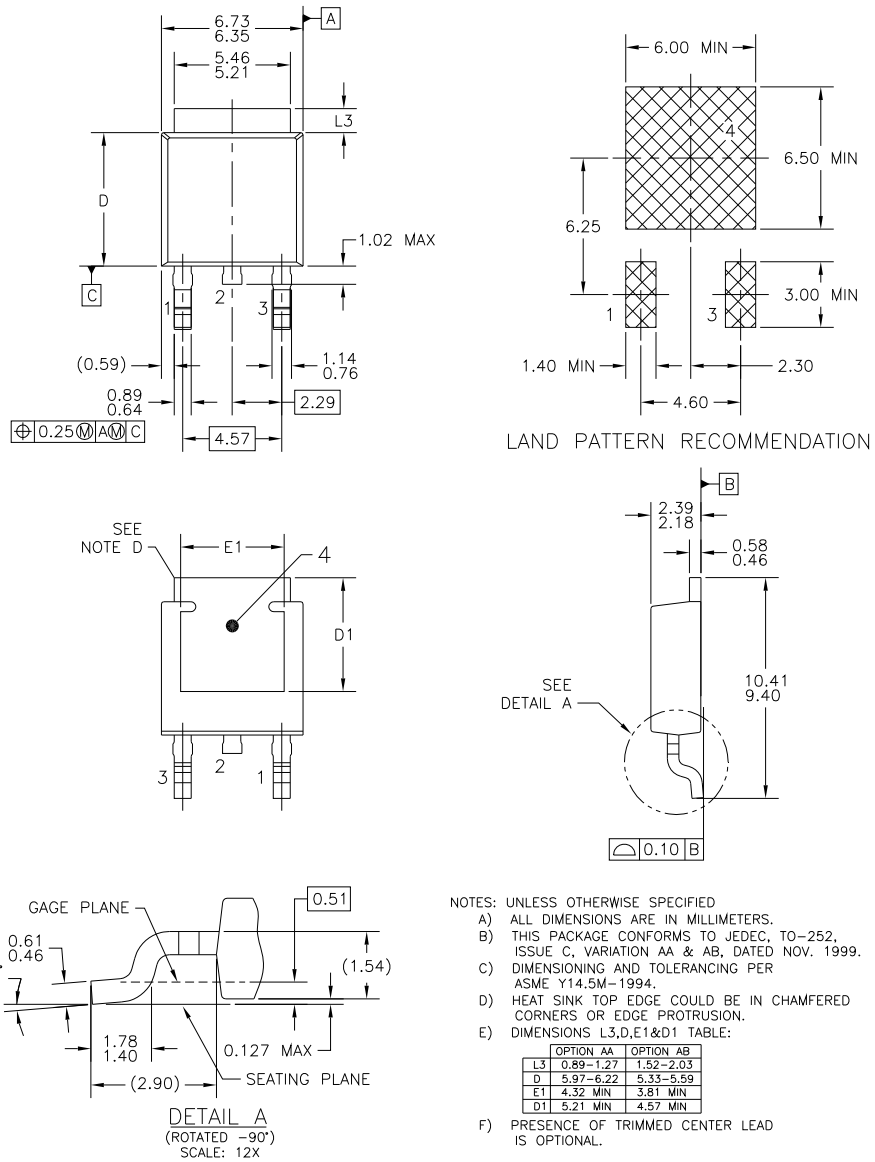
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

E) DIMENSIONS L3,D,E1&D1 TABLE:

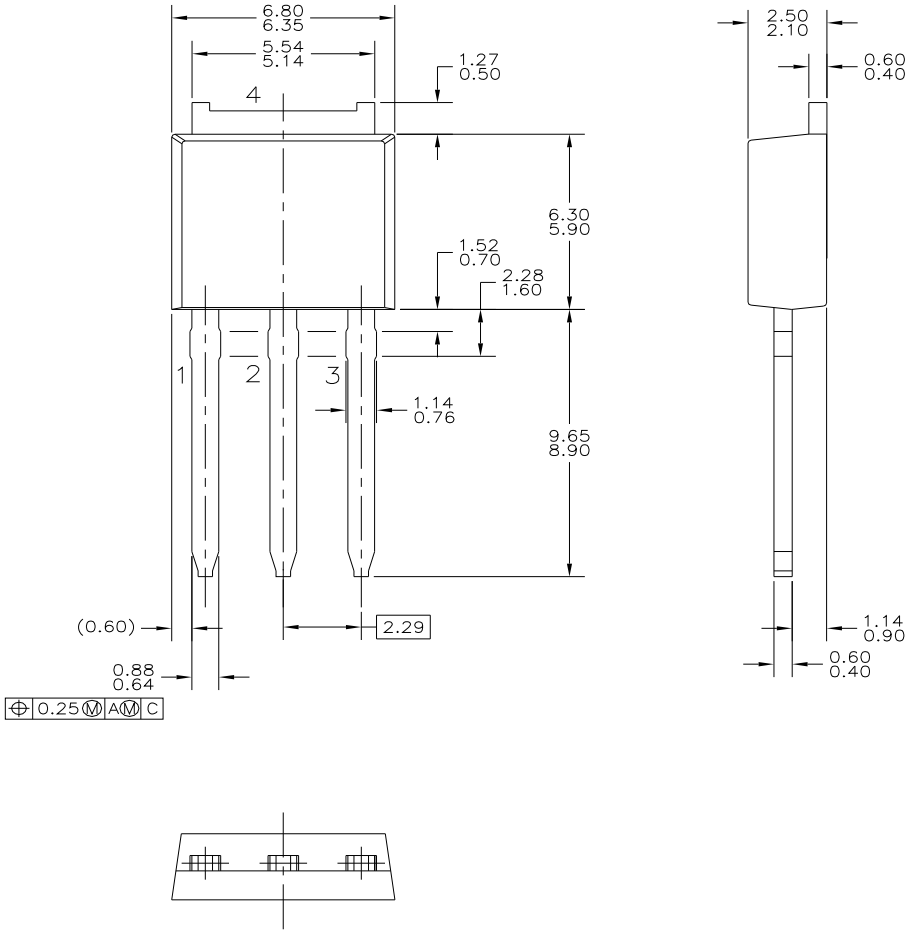
	OPTION AA	OPTION AB
L3	0.89−1.27	1.52−2.03
D	5.97−6.22	5.33−5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

Mechanical Dimensions

I-PAK



Dimensions in Millimeters

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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