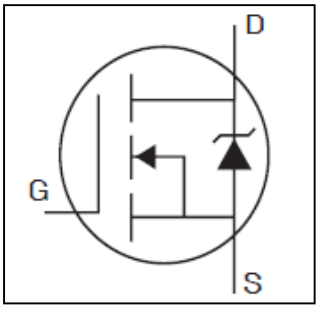
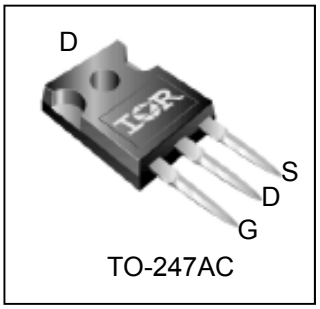
| | |
|---|---|
| $V_{DSS}$ | 300V |
| $R_{DS(on)}$ typ. | 25.5mΩ |
| max. | 32mΩ |
| $I_D$ | 70A |



TO-247AC

| G | D | S |
|---|---|---|
| Gate | Drain | Source |

**Applications**
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

**Benefits**
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free

| Base Part Number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IRFP4868PbF | TO-247AC | Tube | 25 | IRFP4868PbF |

**Absolute Maximum Ratings**

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 70 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V | 49 | |
| $I_{DM}$ | Pulsed Drain Current ① | 280 | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 517 | W |
| | Linear Derating Factor | 3.4 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds<br>(1.6mm from case) | 300 | |
| | Mounting torque, 6-32 or M3 screw | 10lbf·in (1.1N·m) | |

**Avalanche Characteristics**

| | | | |
|---|---|---|---|
| $E_{AS\ (Thermally\ limited)}$ | Single Pulse Avalanche Energy ② | 1093 | mJ |
| $I_{AR}$ | Avalanche Current ① | See Fig. 14, 15, 22a, 22b | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | | mJ |

**Thermal Resistance**

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑦⑧ | ––– | 0.29 | |
| $R_{\theta CS}$ | Case-to-Sink, Flat Greased Surface | 0.24 | ––– | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | ––– | 40 | |

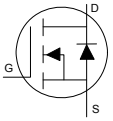
**Static @ $T_J$ = 25°C (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 300 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.29 | — | V/°C | Reference to 25°C, $I_D$ = 5mA① |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 25.5 | 32 | mΩ | $V_{GS}$ = 10V, $I_D$ = 42A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 3.0 | — | 5.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 20 | µA | $V_{DS}$ = 300V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 300V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -20V |
| $R_G$ | Internal Gate Resistance | — | 1.1 | — | Ω | |

**Dynamic @ $T_J$ = 25°C (unless otherwise specified)**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 80 | — | — | S | $V_{DS}$ = 50V, $I_D$ = 42A |
| $Q_g$ | Total Gate Charge | — | 180 | 270 | nC | $I_D$ = 42A |
| $Q_{gs}$ | Gate-to-Source Charge | — | 60 | — | | $V_{DS}$ =150V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | — | 57 | — | | $V_{GS}$ = 10V ④ |
| $Q_{sync}$ | Total Gate Charge Sync. ($Q_g$ - $Q_{gd}$) | — | 123 | — | | $I_D$ = 42A, $V_{DS}$ =0V, $V_{GS}$ = 10V |
| $t_{d(on)}$ | Turn-On Delay Time | — | 24 | — | ns | $V_{DD}$ = 195V |
| $t_r$ | Rise Time | — | 16 | — | | $I_D$ = 42A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 62 | — | | $R_G$ = 1.0Ω |
| $t_f$ | Fall Time | — | 45 | — | | $V_{GS}$ = 10V ④ |
| $C_{iss}$ | Input Capacitance | — | 10774 | — | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 612 | — | | $V_{DS}$ = 50V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 193 | — | | *f* = 1.0 MHz, See Fig. 5 |
| $C_{oss}$ eff. (ER) | Effective Output Capacitance (Energy Related) ⑥ | — | 406 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 240V ⑥, See Fig. 11 |
| $C_{oss}$ eff. (TR) | Effective Output Capacitance (Time Related)⑤ | — | 710 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 240V ⑤ |

**Diode Characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 70 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 280 | A | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.3 | V | $T_J$ = 25°C, $I_S$ = 42A, $V_{GS}$ = 0V ④ |
| dv/dt | Peak Diode Recovery ③ | — | 7.3 | — | V/ns | $T_J$ = 25°C, $I_S$ = 42A, $V_{DS}$ = 300V |
| $t_{rr}$ | Reverse Recovery Time | — | 351 | — | ns | $T_J$ = 25°C |
| | | — | 454 | — | | $T_J$ = 125°C |
| $Q_{rr}$ | Reverse Recovery Charge | — | 2520 | — | nC | $T_J$ = 25°C |
| | | — | 3686 | — | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | — | 16 | — | A | $T_J$ = 25°C |
| $t_{on}$ | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

$V_R$ = 255V, $I_F$ = 42A di/dt = 100A/µs ④

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 1.2mH $R_G$ = 50Ω, $I_{AS}$ = 42A, $V_{GS}$ =10V. Part not recommended for use above this value.

③ ISD ≤ 42A, di/dt ≤ 1706A/µs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ Coss eff. (TR) is a fixed capacitance that gives the same charging time as Coss while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑥ Coss eff. (ER) is a fixed capacitance that gives the same energy as Coss while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ $R_\theta$ is measured at $T_J$ approximately 90°C.

⑧ $R_{\theta JC}$ value shown is at time zero.

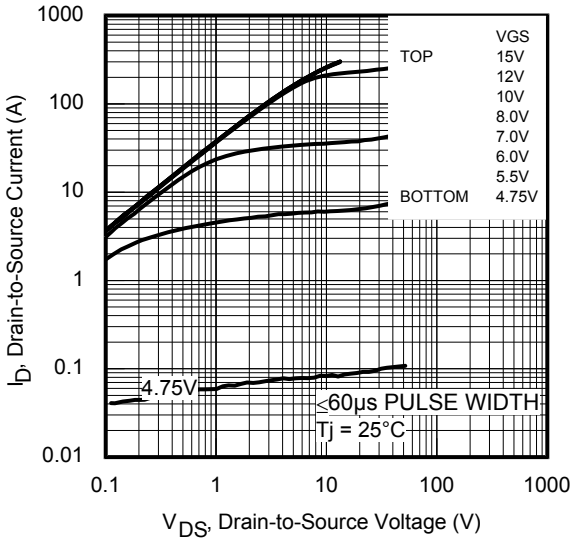



**Fig 1.** Typical Output Characteristics

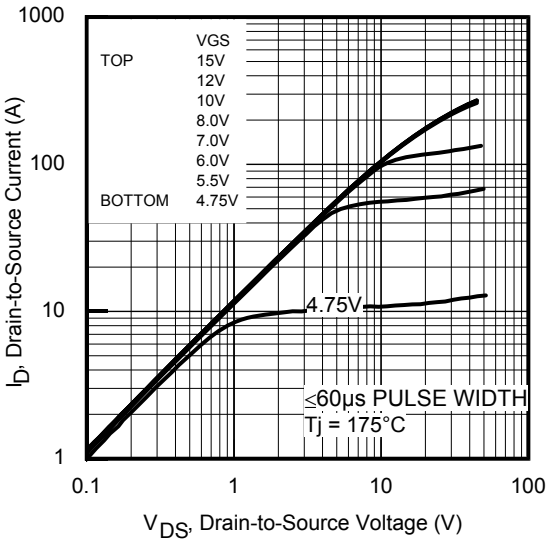



**Fig 2.** Typical Output Characteristics

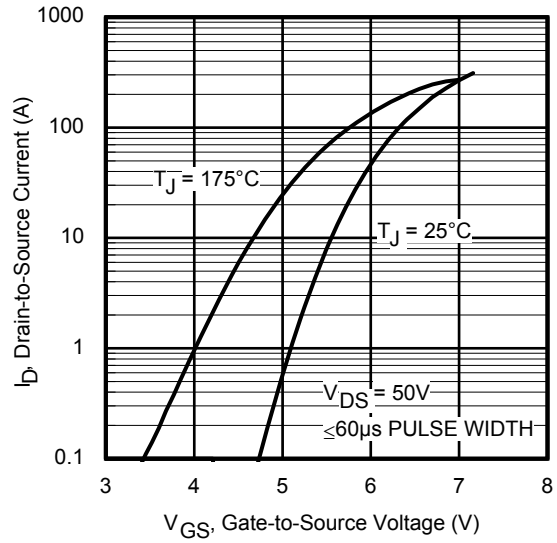



**Fig 3.** Typical Transfer Characteristics

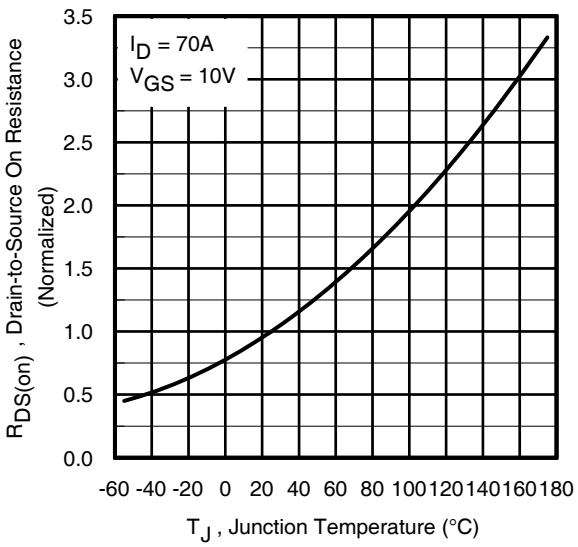



**Fig 4.** Normalized On-Resistance vs. Temperature

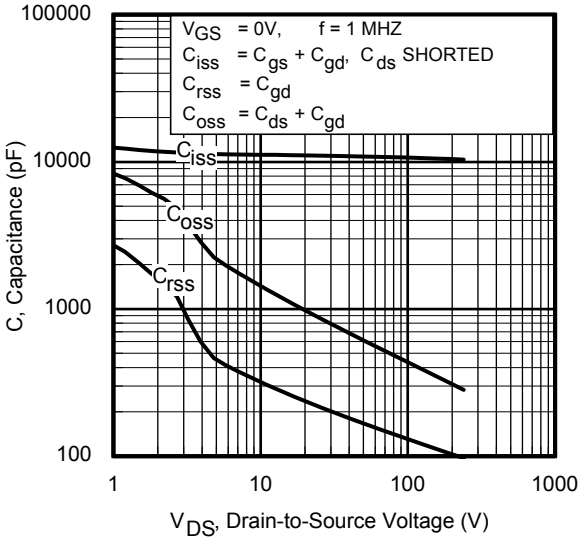



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

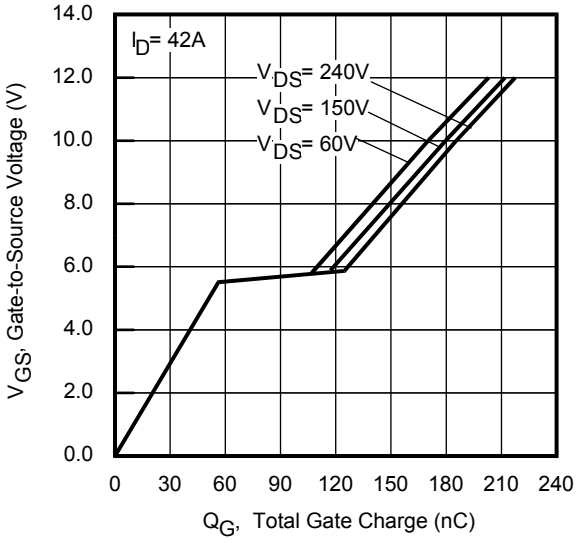



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

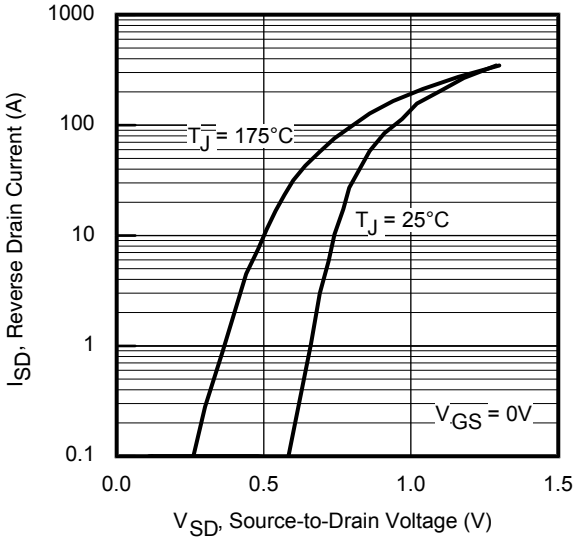



**Fig 7.** Typical Source-to-Drain Diode Forward Voltage

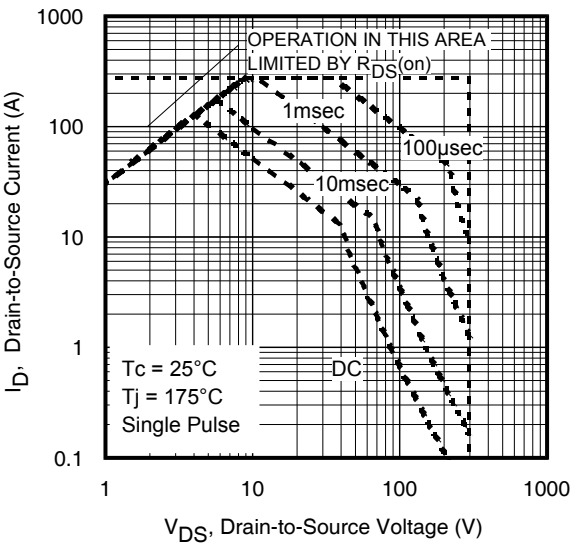



**Fig 8.** Maximum Safe Operating Area

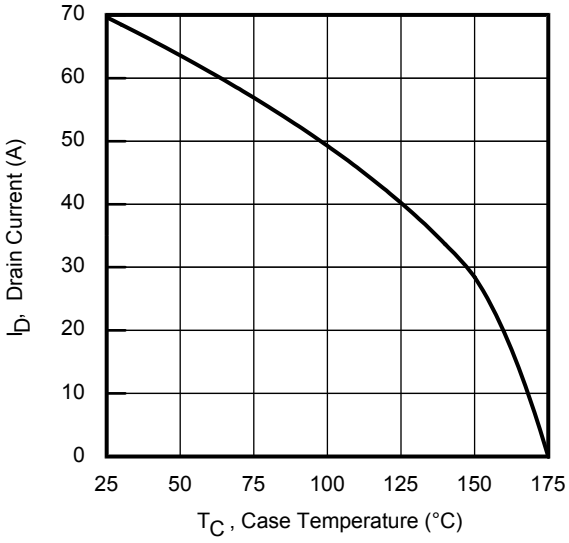



**Fig 9.** Maximum Drain Current vs. Case Temperature

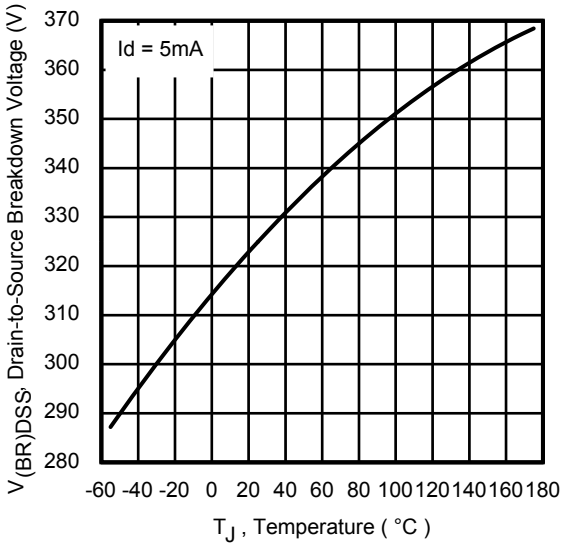



**Fig 10.** Drain-to-Source Breakdown Voltage

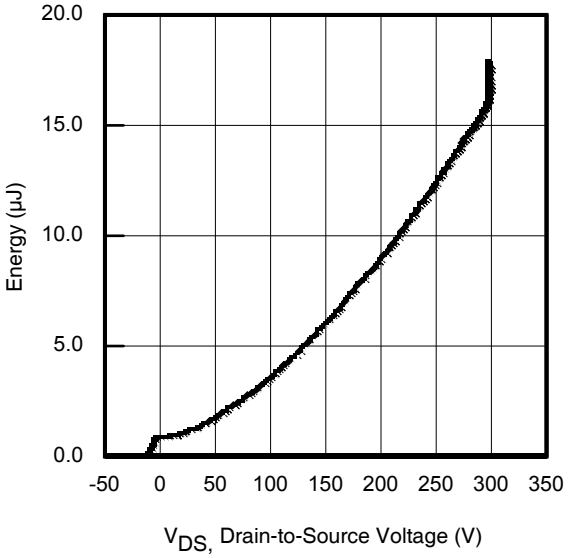



**Fig 11.** Typical Coss Stored Energy

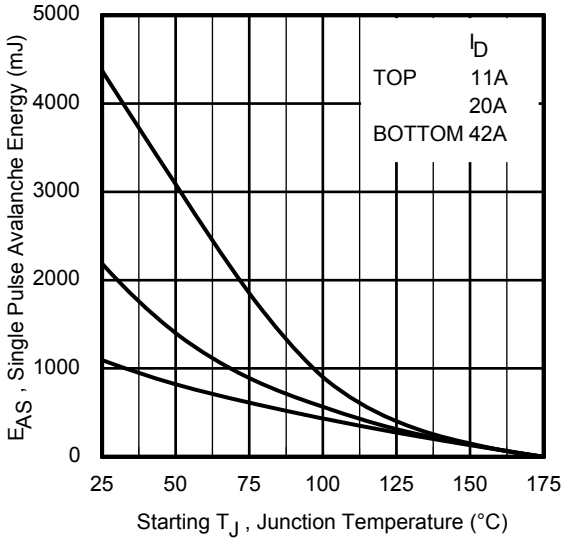



**Fig 12.** Maximum Avalanche Energy vs. Drain Current

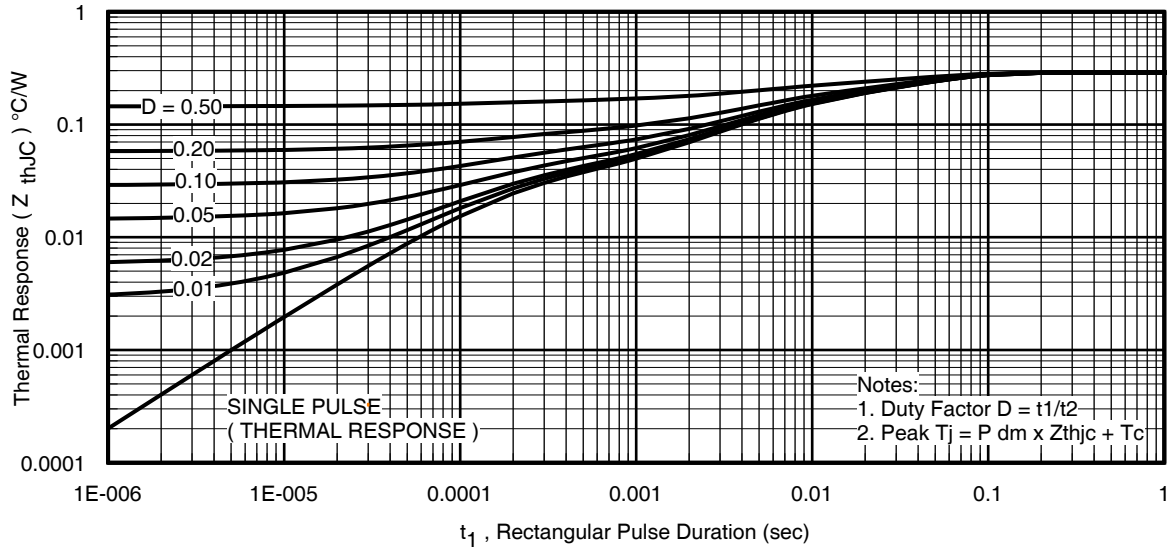



**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

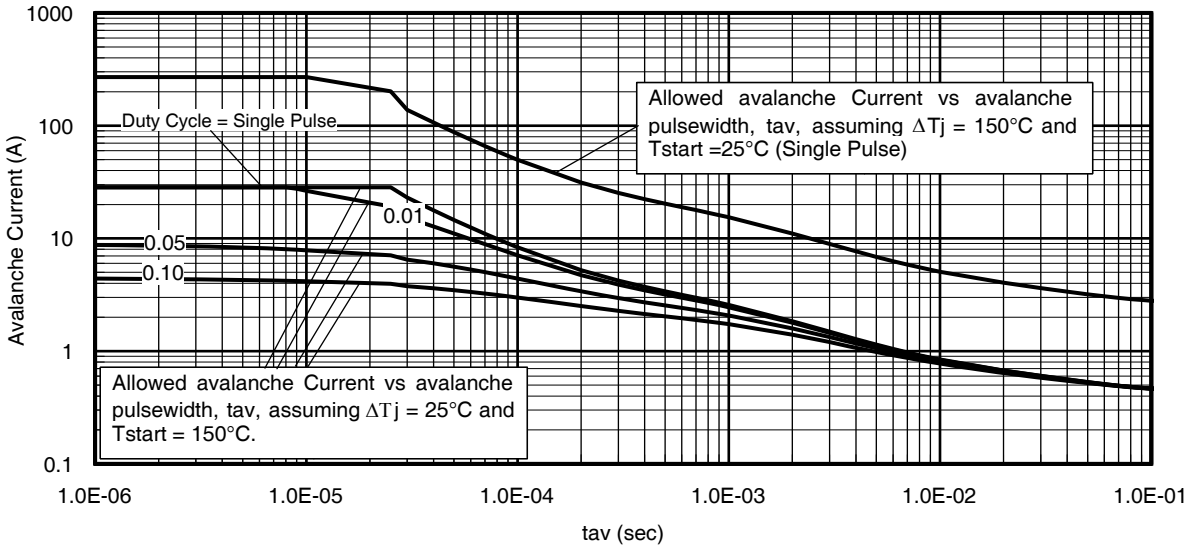



**Fig 14.** Typical Avalanche Current vs. Pulsewidth

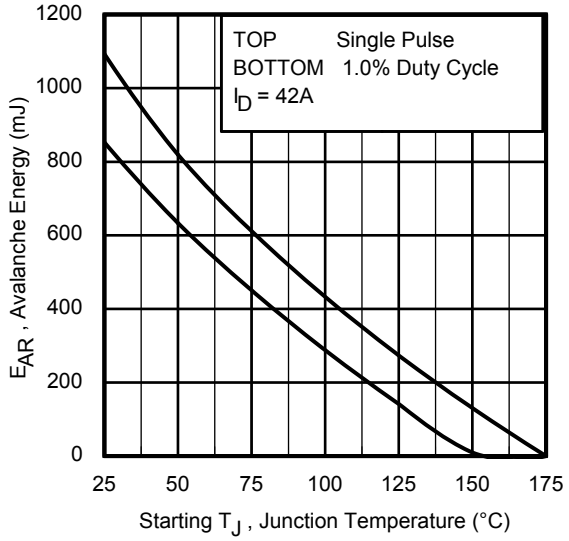



**Fig 15.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of Tjmax. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as Tjmax is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed Tjmax (assumed as 25°C in Figure 14, 15).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

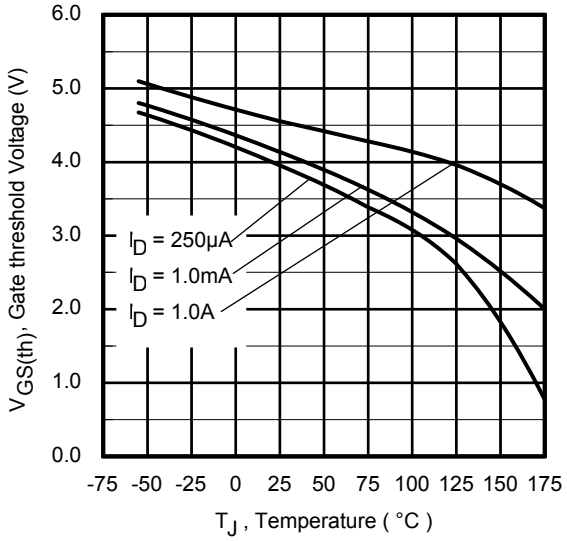



**Fig. 16** Threshold Voltage vs. Temperature

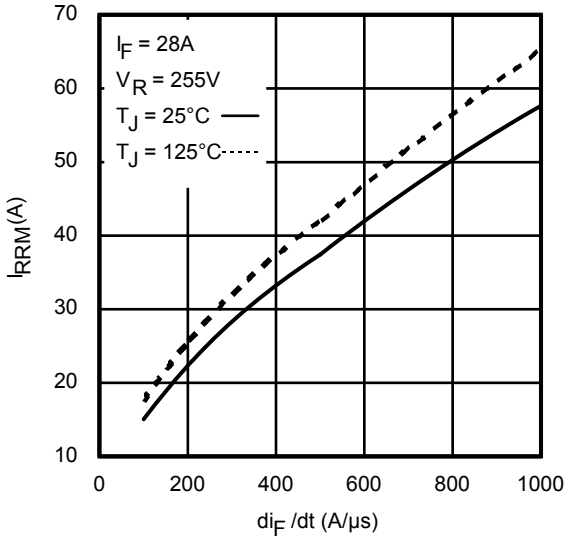



**Fig. 17** Typical Recovery Current vs. $di_f/dt$

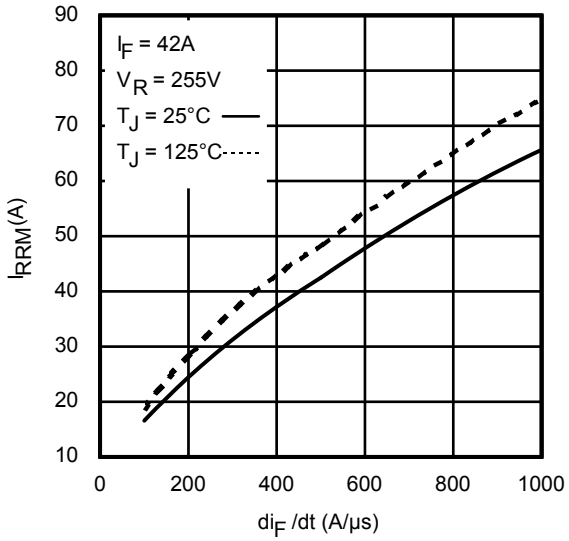



**Fig 18.** Typical Recovery Current vs. $di_f/dt$

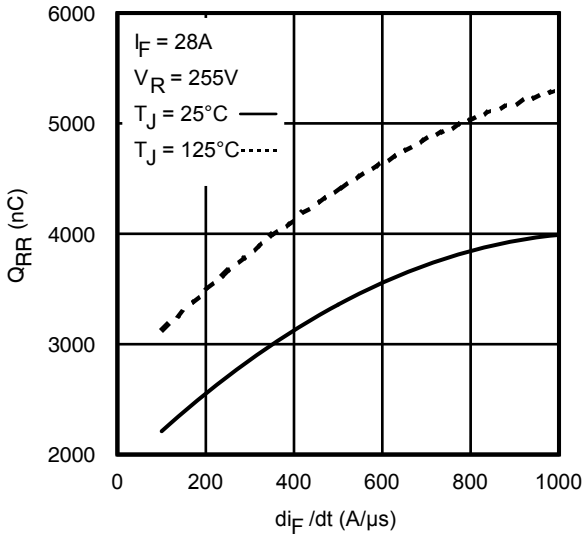



**Fig 19.** Typical Stored Charge vs. $di_f/dt$

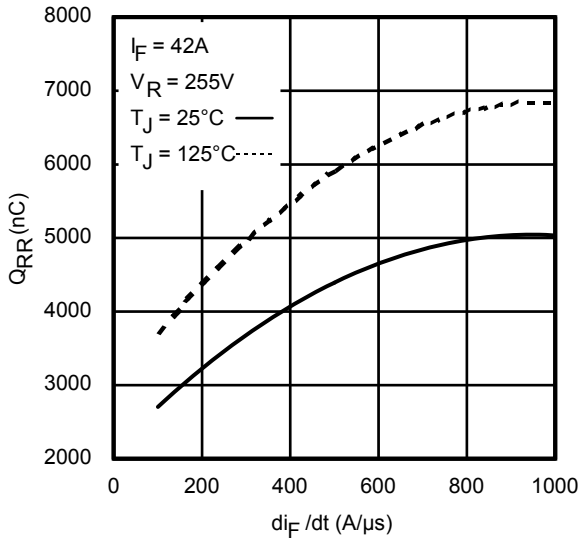



**Fig 20.** Typical Stored Charge vs. $di_f/dt$

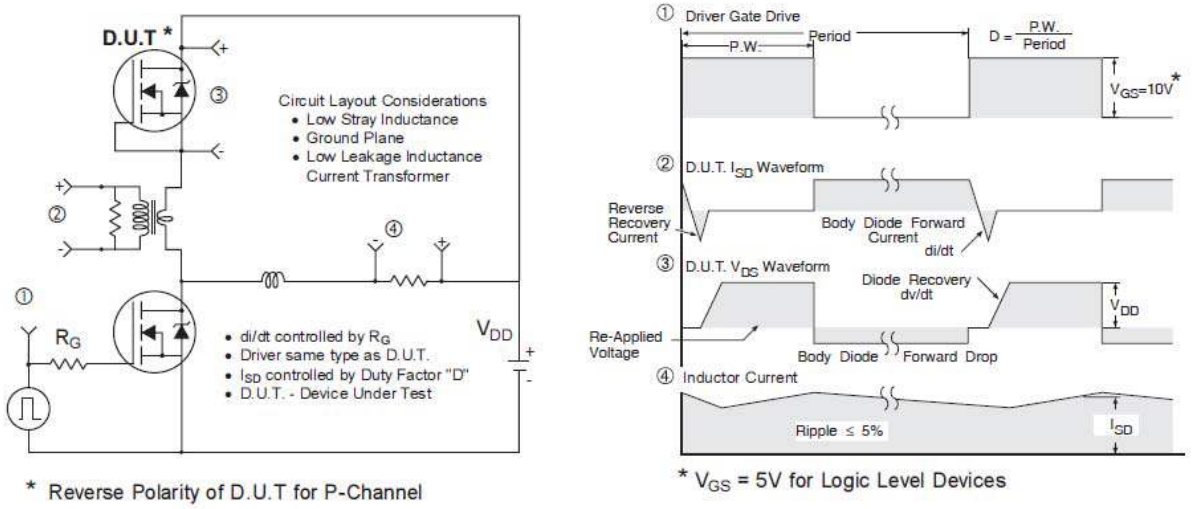



**Fig 21.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

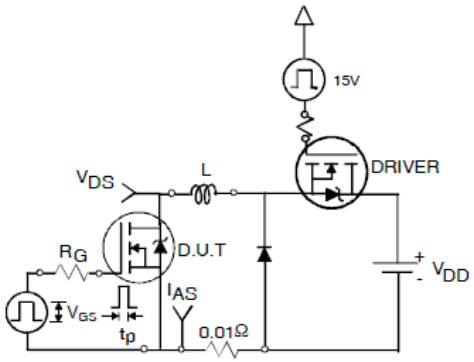



**Fig 22a.** Unclamped Inductive Test Circuit

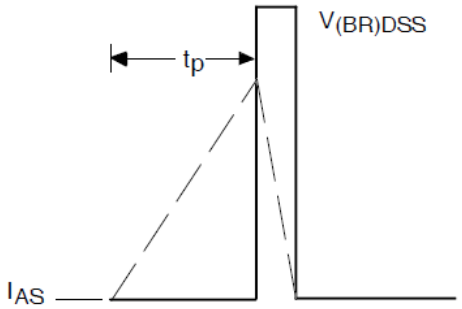



**Fig 22b.** Unclamped Inductive Waveforms

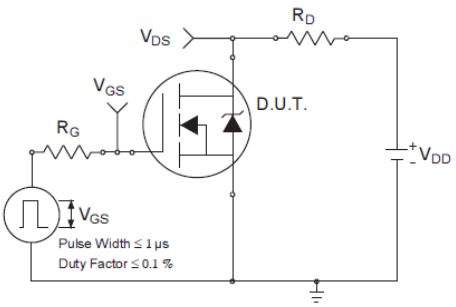



**Fig 23a.** Switching Time Test Circuit

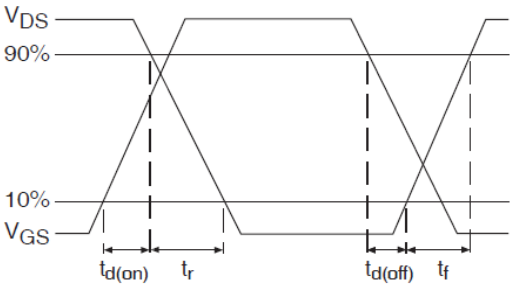



**Fig 23b.** Switching Time Waveforms

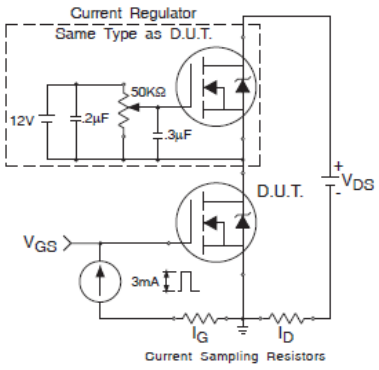



**Fig 24a.** Gate Charge Test Circuit

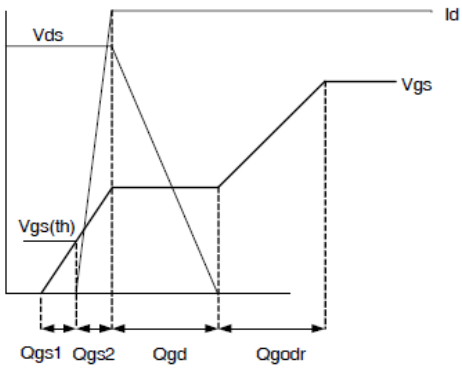
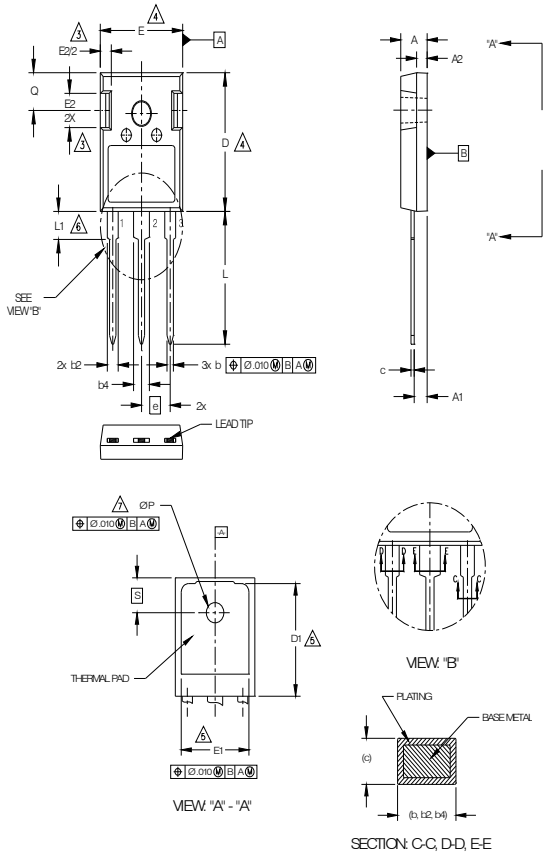



**Fig 24b.** Gate Charge Waveform

# TO-247AC Package Outline

Dimensions are shown in millimeters (inches)




| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | INCHES | | MILLIMETERS | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | .190 | .204 | 4.83 | 5.20 | |
| A1 | .090 | .100 | 2.29 | 2.54 | |
| A2 | .075 | .085 | 1.91 | 2.16 | |
| b | .042 | .052 | 1.07 | 1.33 | |
| b2 | .075 | .094 | 1.91 | 2.41 | |
| b4 | .113 | .133 | 2.87 | 3.38 | |
| c | .022 | .026 | 0.55 | 0.68 | |
| D | .819 | .830 | 20.80 | 21.10 | 4 |
| D1 | .640 | 694 | 16.25 | 17.65 | 5 |
| E | .620 | .635 | 15.75 | 16.13 | 4 |
| E1 | .512 | .570 | 13.00 | 14.50 | |
| E2 | .145 | .196 | 3.68 | 5.00 | |
| e | .215 Typical | | 5.45 Typical | | |
| L | .780 | .800 | 19.80 | 20.32 | |
| L1 | .161 | .173 | 4.10 | 4.40 | |
| ø P | .138 | .143 | 3.51 | 3.65 | |
| Q | .216 | .236 | 5.49 | 6.00 | |
| S | .238 | .248 | 6.04 | 6.30 | |

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

DIODES

1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

NOTES:

1 DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.

2 DIMENSIONS ARE SHOWN IN INCHES AND MILLIMETERS.

3 CONTOUR OF SLOT OPTIONAL.

4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.

5 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.

6 LEAD FINISH UNCONTROLLED IN L1.

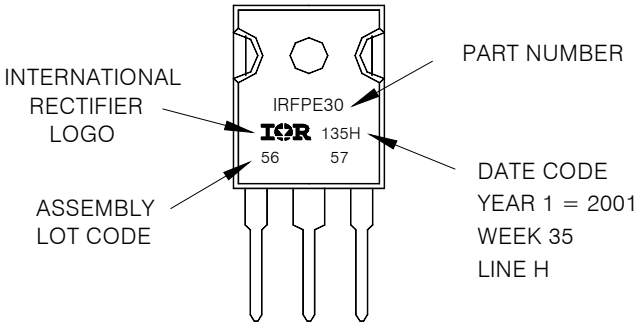
7 ø P TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.

# TO-247AC Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"




TO-247 package is not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

**Qualification information**†

| | | |
|---|---|---|
| Qualification level | Industrial†† (per JEDEC JESD47F ††† guidelines ) | |
| Moisture Sensitivity Level | TO-247AC | N/A |
| RoHS compliant | Yes | |

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

Data and specifications subject to change without notice.

International IOR Rectifier

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