

Description

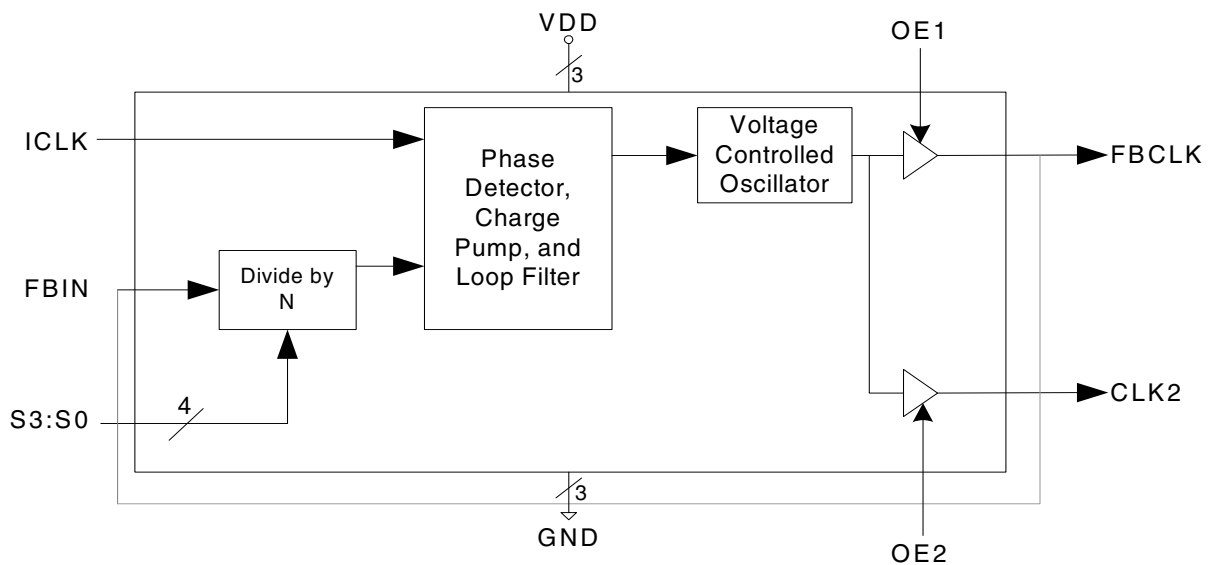
The ICS670-02 is a high speed, low phase noise, Zero Delay Buffer (ZDB) which integrates IDT's proprietary analog/digital Phase Locked Loop (PLL) techniques. Part of IDT's ClockBlocks™ family, the part's zero delay feature means that the rising edge of the input clock aligns with the rising edges of the outputs giving the appearance of no delay through the device. There are two identical outputs on the chip. The FBCLK should be used to connect to the FBIN. Each output has its own output enable pin.

The ICS670-02 is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to video. By allowing off-chip feedback paths, the chip can eliminate the delay through other devices. The 15 different on-chip multipliers work in a variety of applications. For other multipliers, including functional multipliers, see the ICS527.

Features

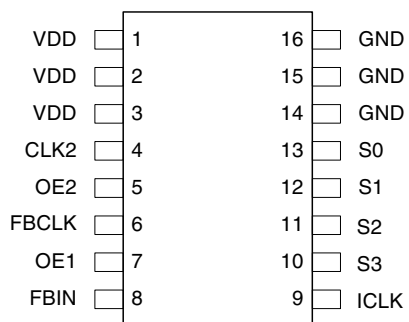
- Packaged in 16-pin SOIC
- Pb (lead) free package, RoHS compliant
- Clock inputs from 5 to 160 MHz (see page 2)
- Patented PLL with low phase noise
- Output clocks up to 160 MHz at 3.3 V
- 15 selectable on-chip multipliers
- Power down mode available
- Low phase noise: -111 dBc/Hz at 10 kHz
- Output enable function tri-states outputs
- Low jitter 15 ps one sigma
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V or 5 V
- Industrial temperature range available (-40 to +85°C)

Block Diagram



External Feedback from FBCLK is recommended.

Pin Assignment



Multiplier Select Table

S3	S2	S1	S0	CLK2 (and FBCLK)	Input Range (MHz)
0	0	0	0	Low (Power down entire chip)	-
0	0	0	1	Input x1.333	18 - 120
0	0	1	0	Input x6	5 - 26.67
0	0	1	1	Input x1.5	16.67 - 107
0	1	0	0	Input x3.333	7.5 - 48
0	1	0	1	Input x2.50	10 - 64
0	1	1	0	Input x4	6 - 40
0	1	1	1	Input x1	25 - 160
1	0	0	0	Input x2.333	11 - 69
1	0	0	1	Input x2.666	10 - 60
1	0	1	0	Input x12	5 - 13.33
1	0	1	1	Input x3	8 - 53.33
1	1	0	0	Input x10	5 - 16
1	1	0	1	Input x5	6 - 32
1	1	1	0	Input x8	5 - 20
1	1	1	1	Input x2	12 - 80

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1 - 3	VDD	Input	Power supply. Connect both pins to the same voltage (either 3.3 V or 5 V).
4	CLK2	Output	Clock output from VCO. Output frequency equals the input frequency times multiplier.
5	OE2	Input	Output clock enable 2. Tri-states the clock 2 output when low.
6	FBCLK	Output	Clock output from VCO. Output frequency equals the input frequency times multiplier.
7	OE1	Input	Output clock enable 1. Tri-states the feedback clock output when low.
8	FBIN	Input	Feedback clock input.
9	ICLK	Input	Clock input. Connect to a 5 - 160 MHz clock.
10	S3	Input	Multiplier select pin 3. Determines outputs per table above. Internal pull-up.
11	S2	Input	Multiplier select pin 2. Determines outputs per table above. Internal pull-up.
12	S1	Input	Multiplier select pin 1. Determines outputs per table above. Internal pull-up.
13	S0	Input	Multiplier select pin 0. Determines outputs per table above. Internal pull-up.
14 - 16	GND	Power	Connect to ground.

External Components

The ICS670-02 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 μ F should be connected between VDD and GND on pins 4 and 5, and VDD and GND on pins 13 and 12, as close to the device as possible. A series termination resistor of 33 Ω may be used to each clock output pin to reduce reflections.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS670-02. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=3.3 V \pm 10%, Ambient temperature -40 to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V _{IH}		2			V
Input Low Voltage	V _{IL}				0.8	V
Output High Voltage	V _{OH}	I _{OH} = -12 mA	2.4			V
Output Low Voltage	V _{OL}	I _{OL} = 12 mA			0.4	V
Output High Voltage, CMOS level	V _{OH}	I _{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No Load		35		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Short Circuit Current	I_{OS}	Each output		±50		mA
Internal Pull-up Resistor	R_{PU}	OE, select pins		200		kΩ
Input Capacitance	C_{IN}	OE, select pins		5		pF

AC Electrical Characteristics

VDD = 3.3V ±10%, Ambient Temperature -40 to +85° C, unless stated otherwise

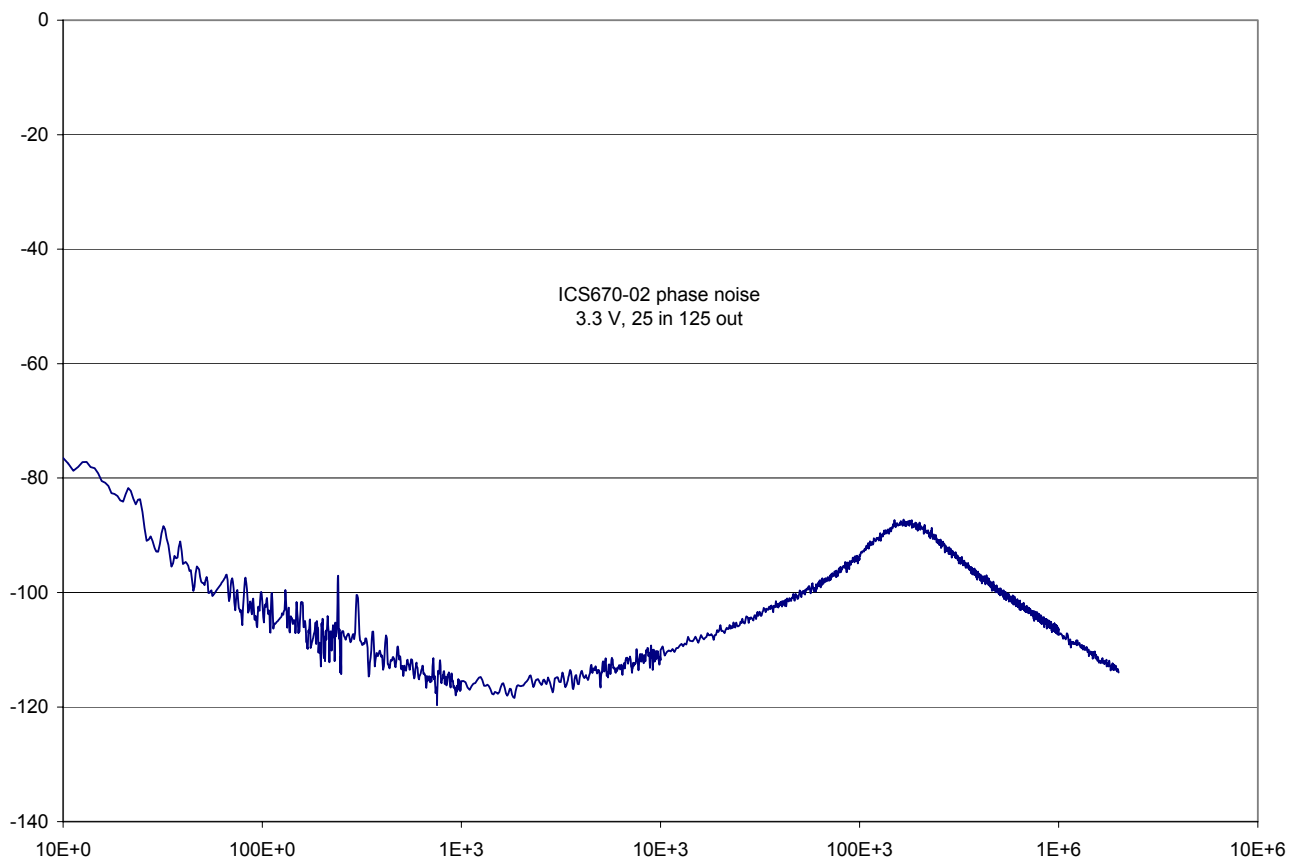
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency	f_{IN}	See table on page 2	5		160	MHz
Output Clock Frequency					160	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, no load			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, no load			1.5	ns
Output Clock Duty Cycle	t_{DC}	measured at VDD/2	45	50	55	%
Input to Output Skew		Note 1		±100		ps
Maximum Absolute Jitter		short term		±45		ps
Maximum Jitter		one sigma		15		ps
Phase Noise, relative to carrier, 125 MHz (x5)		100 Hz offset		-103		dBc/Hz
		1 kHz offset		-117		dBc/Hz
		10 kHz		-111		dBc/Hz
		200 kHz		-88		dBc/Hz

Note 1: Rising edge of ICLK compared with rising edge of CLK2, with FBCLK connected to FBIN, and 15 pF load on CLK2.

Thermal Characteristics

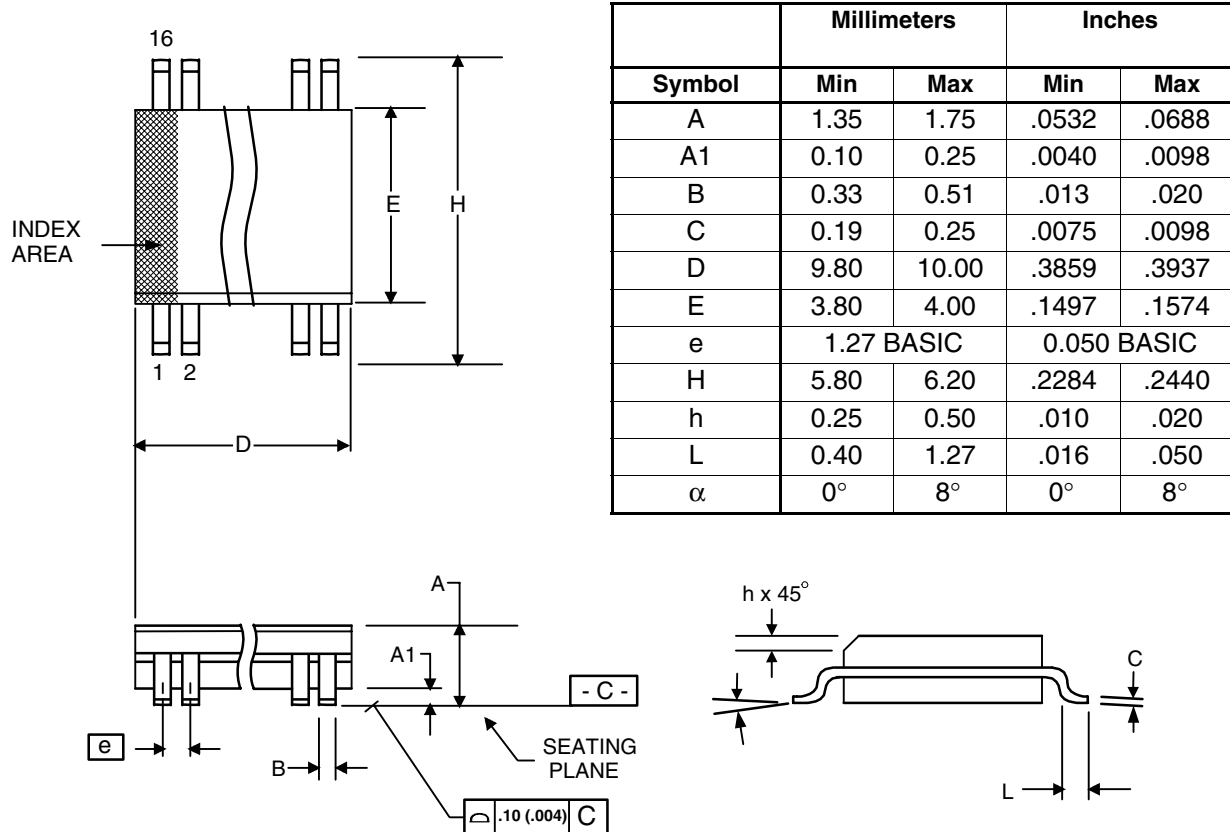
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Phase Noise for 125 MHz output, 25 MHz clock input (VDD = 3.3 V)



Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
670M-02LF	670M-02LF	Tubes	16-pin SOIC	0 to +70° C
670M-02LFT	670M-02LF	Tape and Reel	16-pin SOIC	0 to +70° C
670MI-02LF	670MI-02LF	Tubes	16-pin SOIC	-40 to +85° C
670MI-02LFT	670MI-02LF	Tape and Reel	16-pin SOIC	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.