CSD87503Q3E 30-V N-Channel NexFET™ Power MOSFETs

1 Features

- Dual N-Ch Common Source MOSFETs
- Optimized for 5-V Gate Drive
- Low-Thermal Resistance
- Low Q_g and Q_{gd}
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

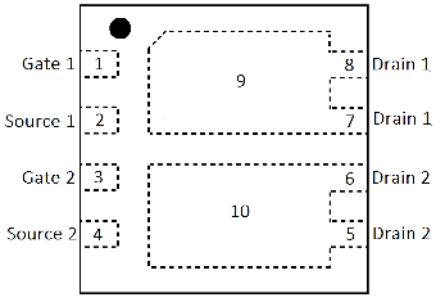
2 Applications

- USB Type-C/PD VBus Protection
- Battery Protection
- Load Switch

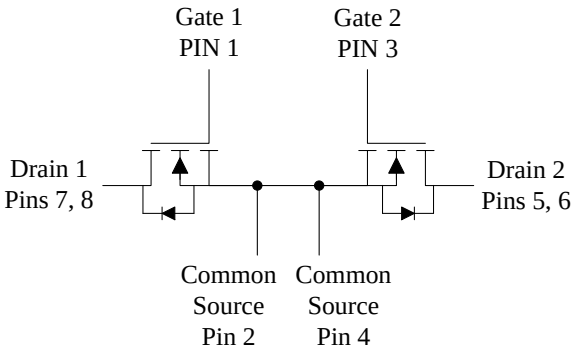
3 Description

The CSD87503Q3E is a 30-V, 13.5-mΩ, common source, dual N-channel device designed for USB Type-C/PD and battery protection. This SON 3.3 × 3.3 mm device has low drain-to-drain on-resistance that minimizes losses and offers low component count for space constrained applications.

Top View



Circuit Image



Product Summary

T_A = 25°C		VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	13.4		nC
Q_{gd}	Gate Charge Gate-to-Drain	5.8		nC
$R_{DD(on)}$	Drain-to-Drain On-Resistance	V_{GS} = 4.5 V	17.3	mΩ
		V_{GS} = 10 V	13.5	
$V_{GS(th)}$	Threshold Voltage	1.7		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD87503Q3E	2500	13-Inch Reel	SON 3.30-mm × 3.30-mm Plastic Package	Tape and Reel
CSD87503Q3ET	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

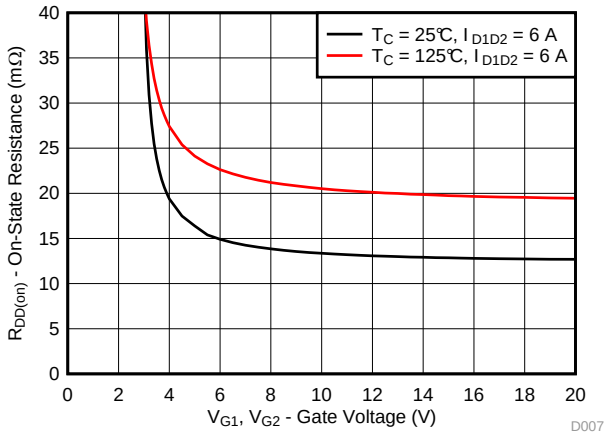
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
$I_{D1, D2}$	Continuous Drain-to-Drain Current (Package Limited)	10	A
I_{DS}	Continuous Drain-to-Source Current (Package Limited)	1.5	A
$I_{D1, D2M}$	Pulsed Drain-to-Drain Current,(1)	89	A
P_D	Power Dissipation(2)	2.6	W
P_D	Power Dissipation, T_C = 25°C	15.6	W
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C

(1) Max $R_{\theta JC}$ = 8°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.

(2) Typical $R_{\theta JA}$ = 50°C/W when mounted on a 1-in² (6.45-cm²), 2-oz (0.071-mm) thick Cu pad on a 0.06-in (1.52-mm) thick FR4 PCB.

$R_{DD(on)}$ vs V_{GS}



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4 Revision History

DATE	REVISION	NOTES
September 2017	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage(1)	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Drain-to-source leakage current(1)	V_{GS} = 0 V, V_{DS} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage current(1)	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage(1)	V_{DS} = V_{GS}, I_D = 250 µA	1.3	1.7	2.1	V
$R_{DD(on)}$	Drain-to-drain on-resistance	V_{GS} = 4.5 V, I_{D1D2} = 6 A		17.3	21.9	mΩ
		V_{GS} = 10 V, I_{D1D2} = 6 A		13.5	16.9	
g_{fs}	Transconductance	V_{DS} = 3 V, I_{D1D2} = 6 A		24		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{D1D2} = 15 V, f = 1 MHz		782	1020	pF
C_{OSS}	Output capacitance			157	204	pF
C_{RSS}	Reverse transfer capacitance			149	194	pF
R_g	Series gate resistance(1)			1.5	3.0	Ω
Q_g	Gate charge total (4.5 V)	V_{D1D2} = 15 V, I_{D1D2} = 6 A		13.4	17.4	nC
	Gate charge total (10 V)			32.9	42.8	
Q_{gd}	Gate charge gate-to-drain			5.8		nC
Q_{gs}	Gate charge gate-to-source			4.8		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.0		nC
Q_{OSS}	Output charge	V_{D1D2} = 15 V, V_{GS} = 0 V		4.3		nC
$t_{d(on)}$	Turnon delay time	V_{D1D2} = 15 V, V_{GS} = 10 V, I_{D1D2} = 6 A, R_G = 0 Ω		10		ns
t_r	Rise time			40		ns
$t_{d(off)}$	Turnoff delay time			25		ns
t_f	Fall time			8		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage(1)	I_D = 0.5 A, V_{GS} = 0 V		0.75	0.95	V
Q_{rr}	Reverse recovery charge(1)	V_{DS} = 15 V, I_F = 6 A, di/dt = 300 A/µs		9.2		nC
t_{rr}	Reverse recovery time(1)			14		ns

(1) Parameter measured on both MOSFETs individually. Table values are for a single FET.

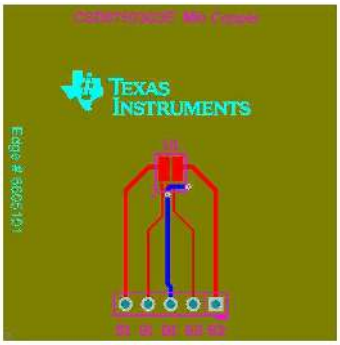
5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)			60	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

Max $R_{\theta JA}$ = 60°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 185°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

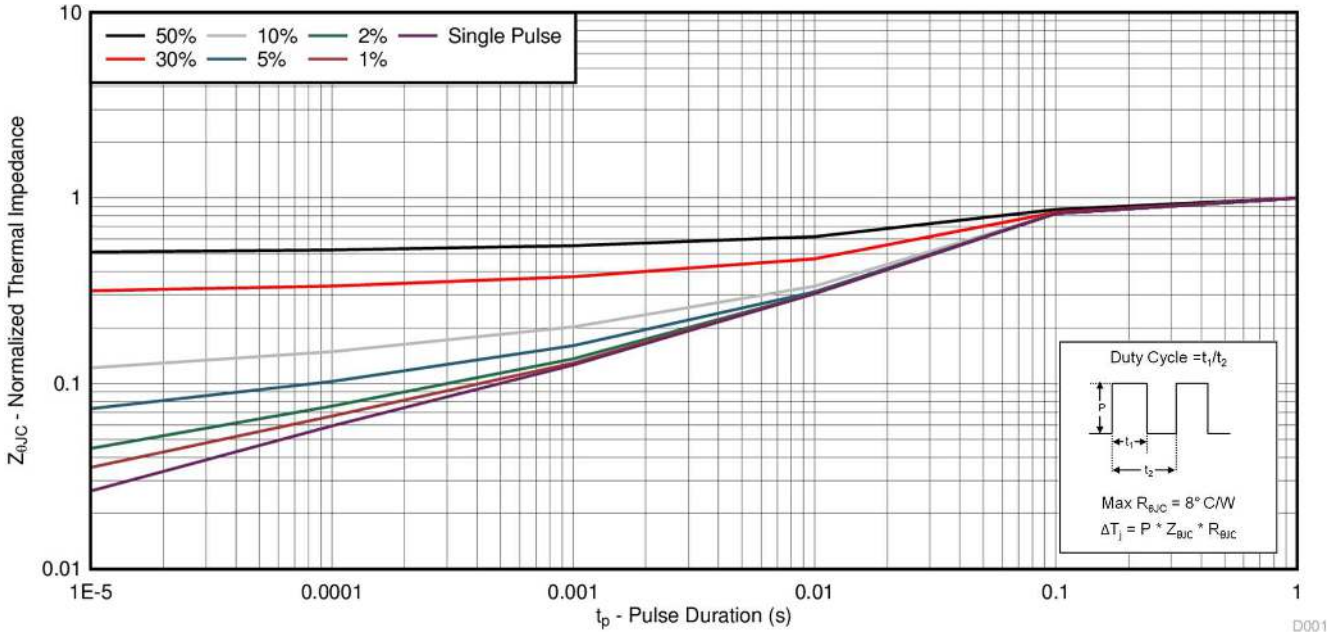
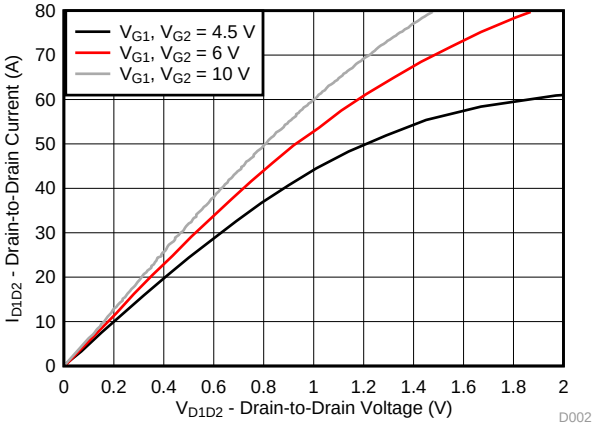


Figure 1. Transient Thermal Impedance

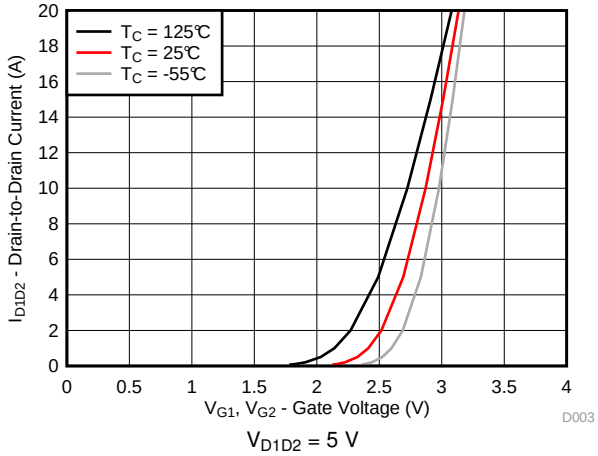
Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



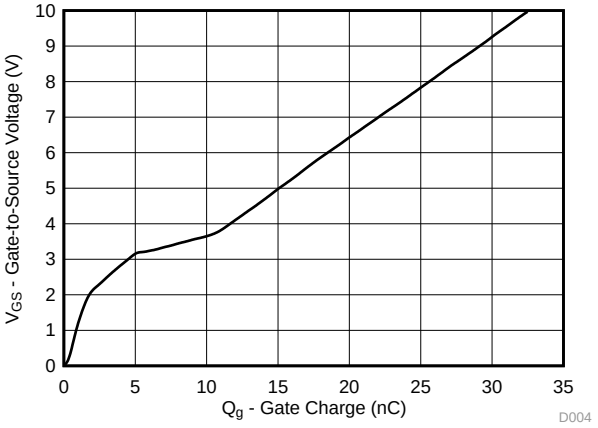
Note: Measurement taken with both gates tied together

Figure 2. Saturation Characteristics



V_{D1D2} = 5 V

Figure 3. Transfer Characteristics



I_{D1D2} = 6 A V_{D1D2} = 15 V

Figure 4. Gate Charge

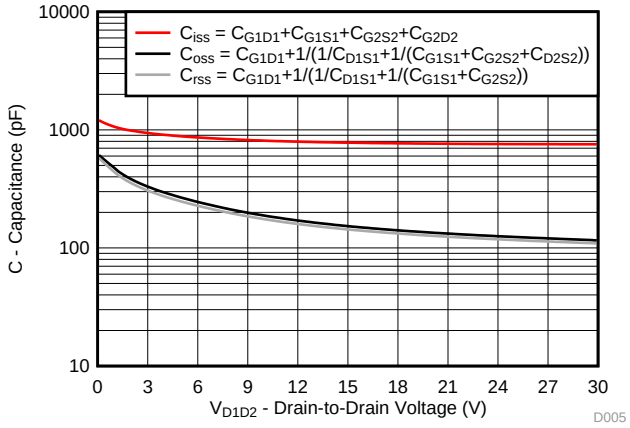
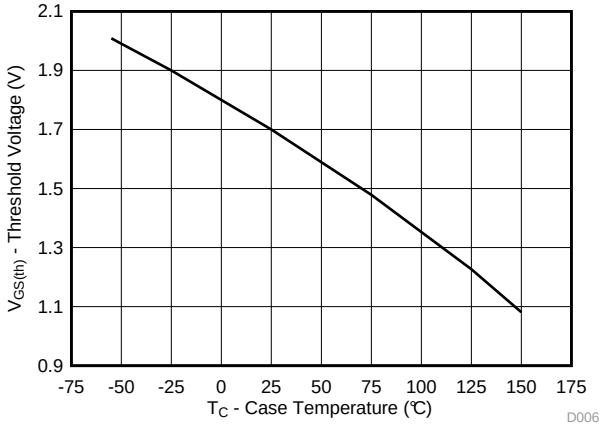


Figure 5. Capacitance



I_D = 250 µA

Figure 6. Threshold Voltage vs Temperature

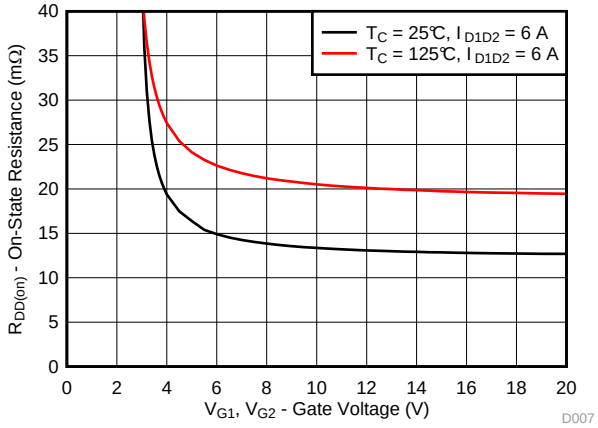
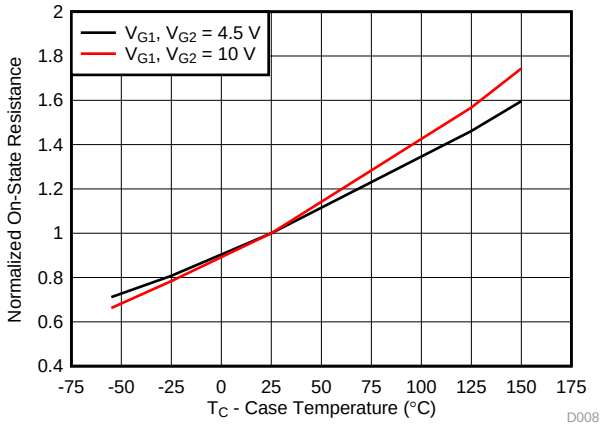


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_{D1D2} = 6 A V_{D1D2} = 15 V

Note: Measurement taken with both gates tied together

Figure 8. Normalized On-State Resistance vs Temperature

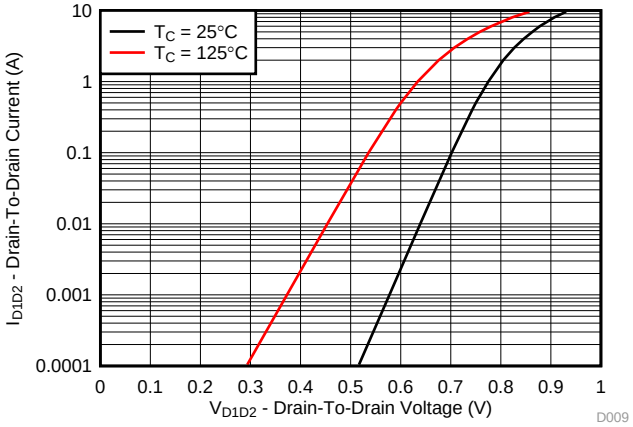
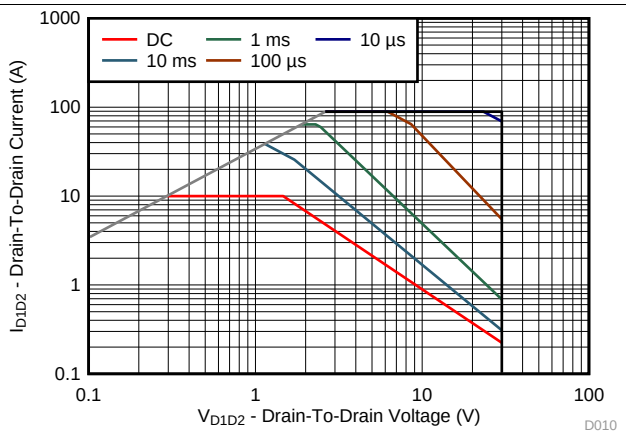


Figure 9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 8°C/W

Figure 10. Maximum Safe Operating Area

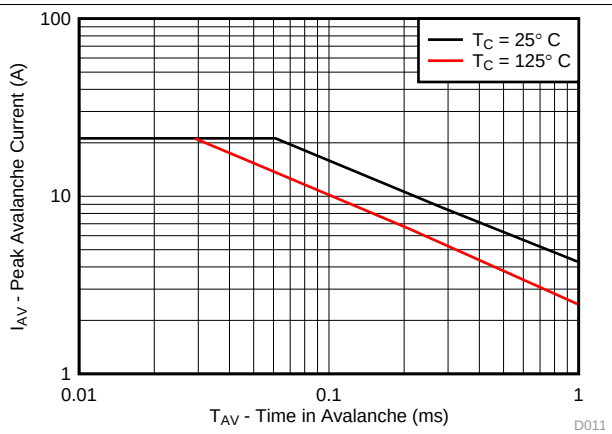


Figure 11. Single Pulse Unclamped Inductive Switching

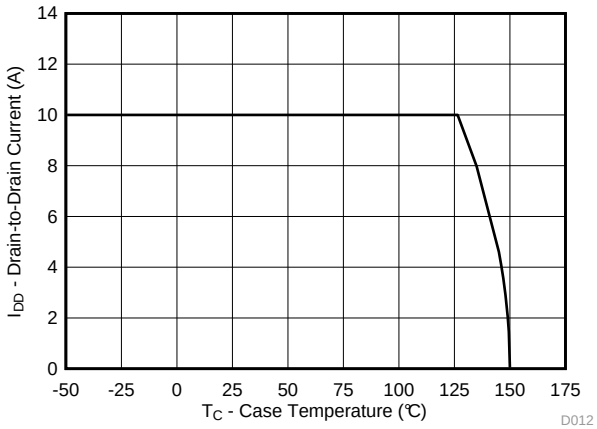


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

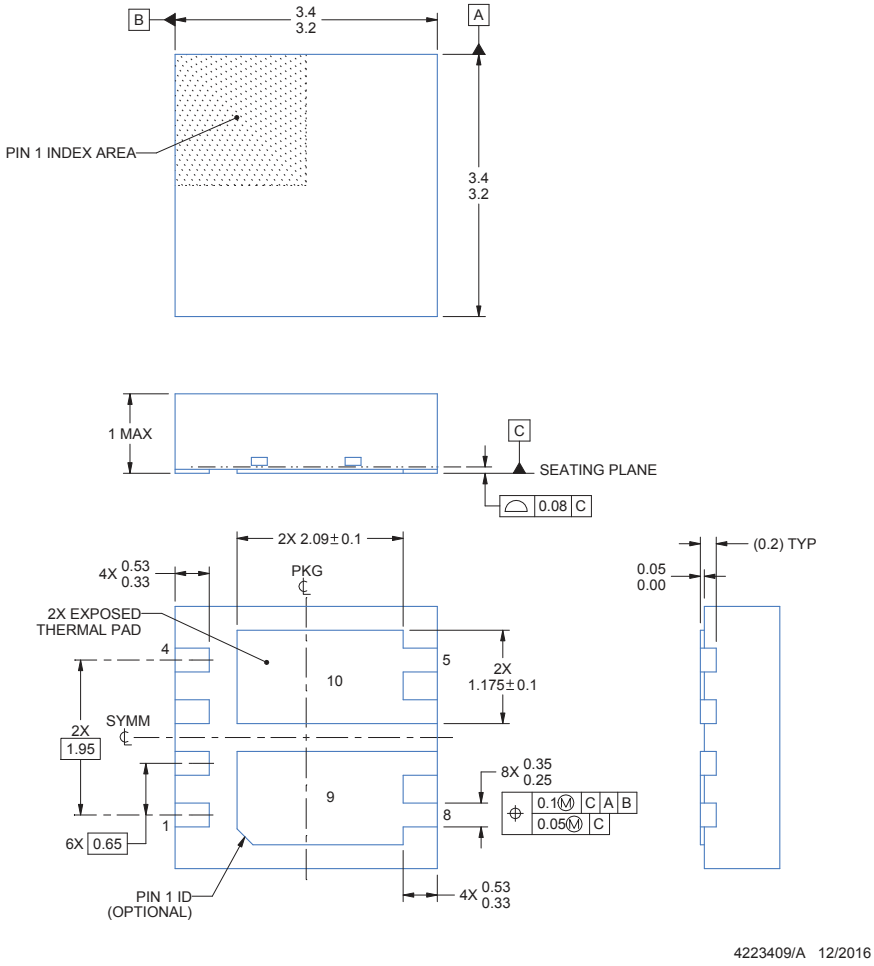
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions

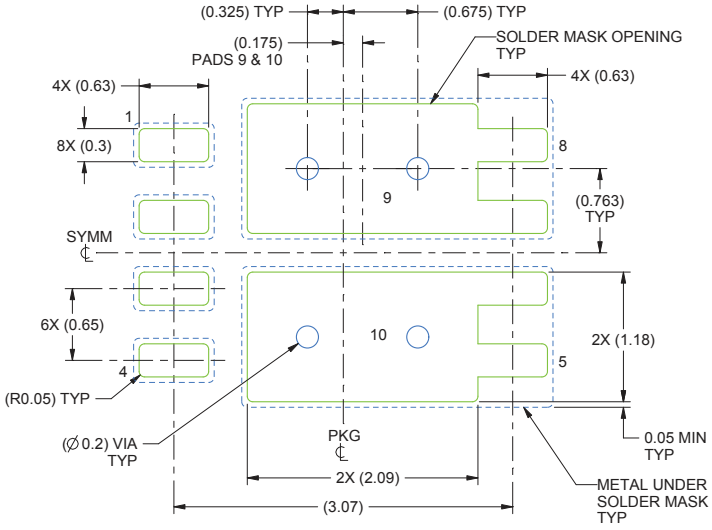


1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

Table 1. Pin Configuration

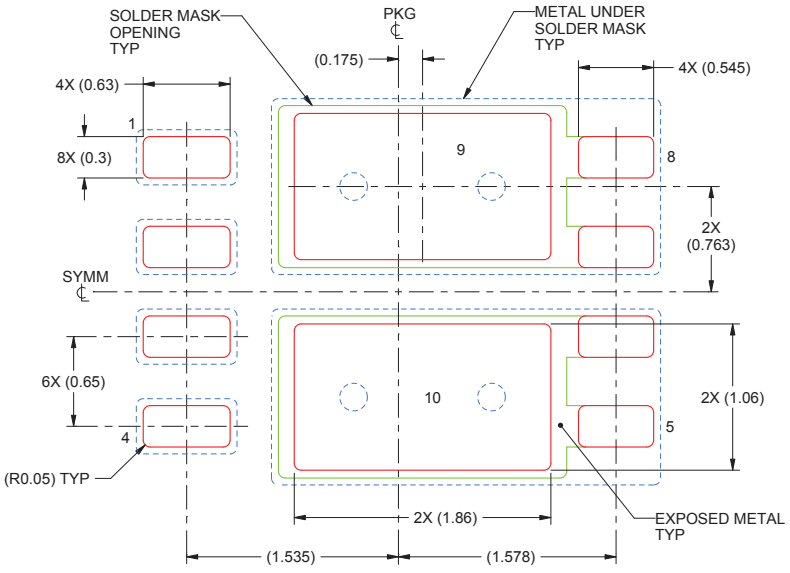
POSITION	DESIGNATION
Pin 1	Gate 1
Pin 2	Common Source
Pin 3	Gate 2
Pin 4	Common Source
Pins 5, 6	Drain 2
Pins 7, 8	Drain 1

7.2 Recommended PCB Pattern



1. This package is designed to be soldered to a thermal pad on the board. For more information, see *QFN/SON PCB Attachment* (SLUA271).
2. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged, or tented.
3. This drawing is subject to change without notice.

7.3 Recommended Stencil Opening



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PADS 9 & 10
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
2. This drawing is subject to change without notice.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87503Q3E	ACTIVE	VSON	DTD	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E	Samples
CSD87503Q3ET	ACTIVE	VSON	DTD	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87503E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

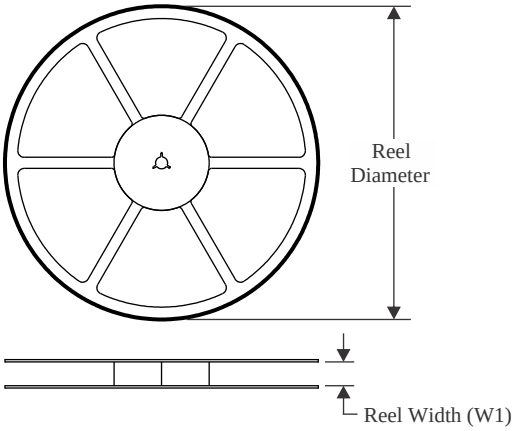
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

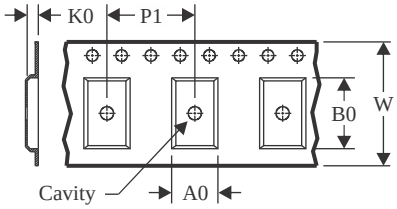
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

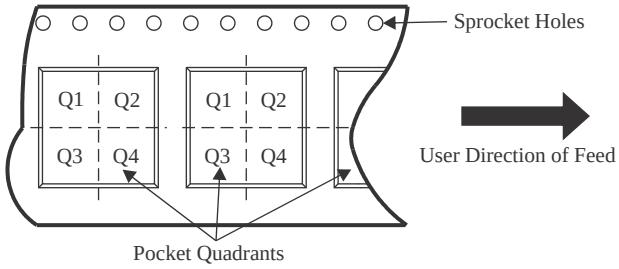


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

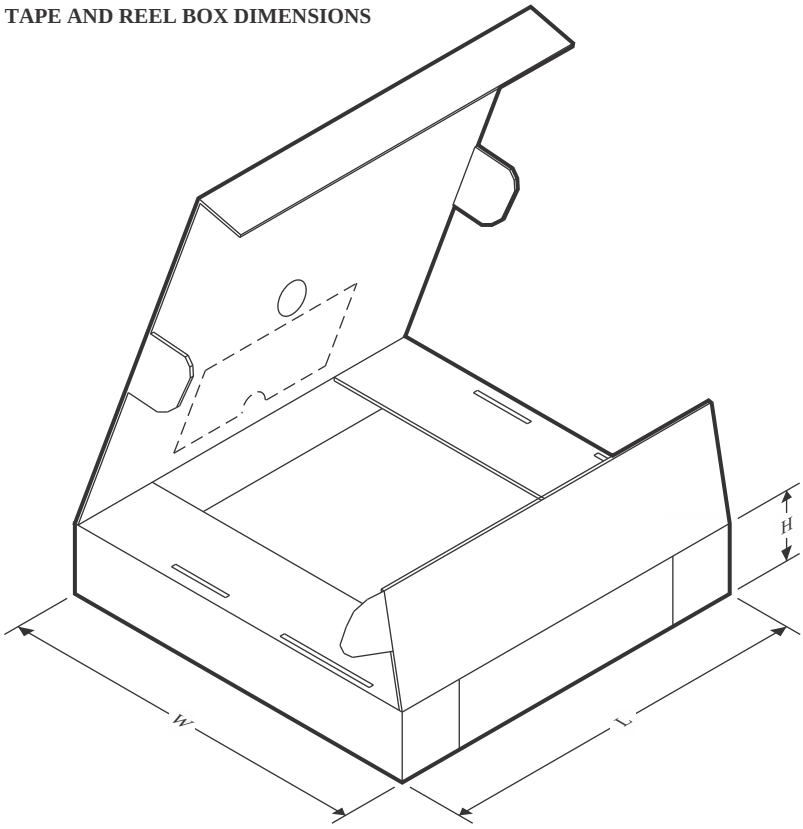
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87503Q3E	VSON	DTD	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD87503Q3ET	VSON	DTD	8	250	178.0	13.5	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

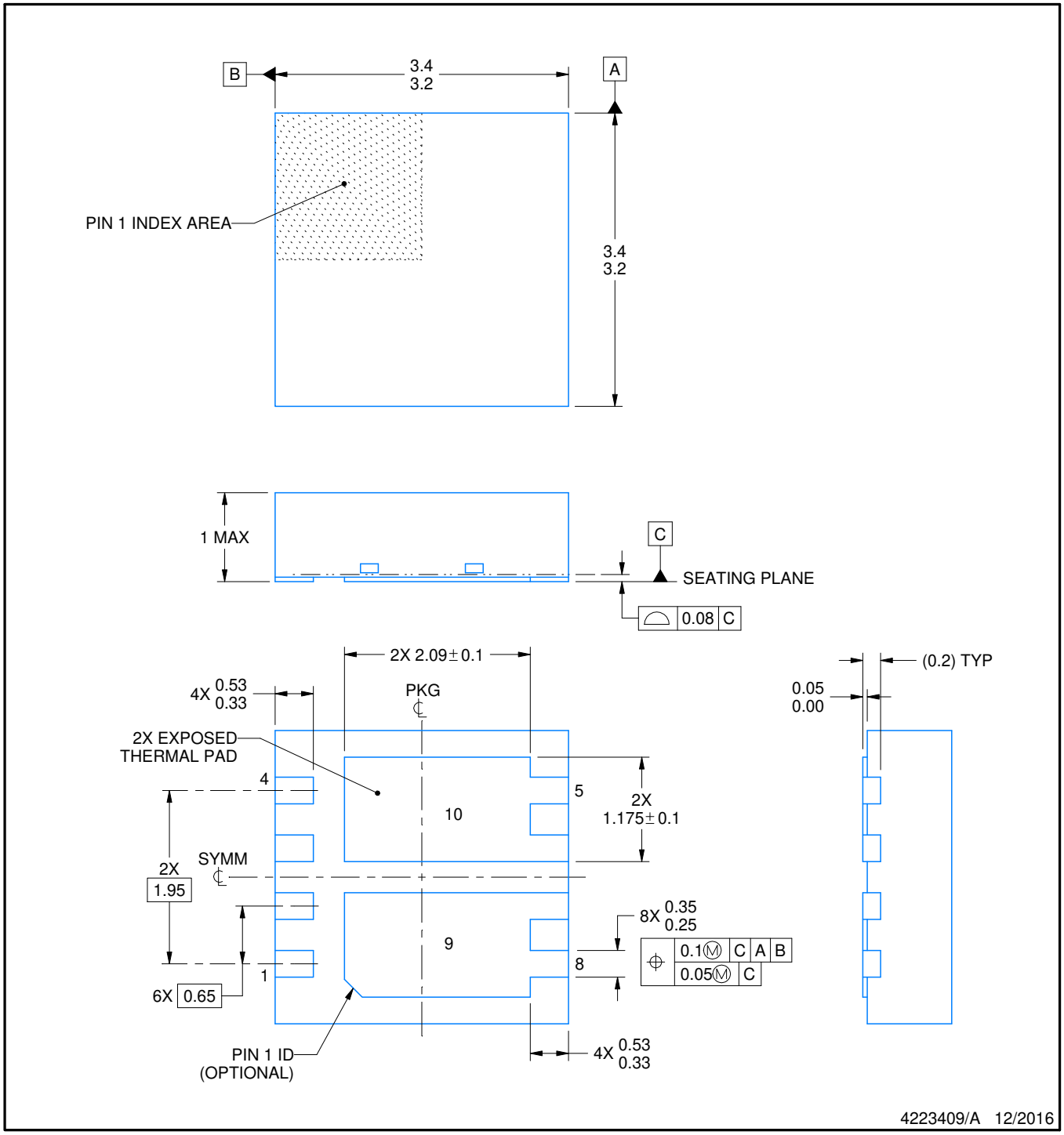
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87503Q3E	VSON	DTD	8	2500	364.0	357.0	31.0
CSD87503Q3ET	VSON	DTD	8	250	189.0	185.0	36.0

DTD0008A

PACKAGE OUTLINE

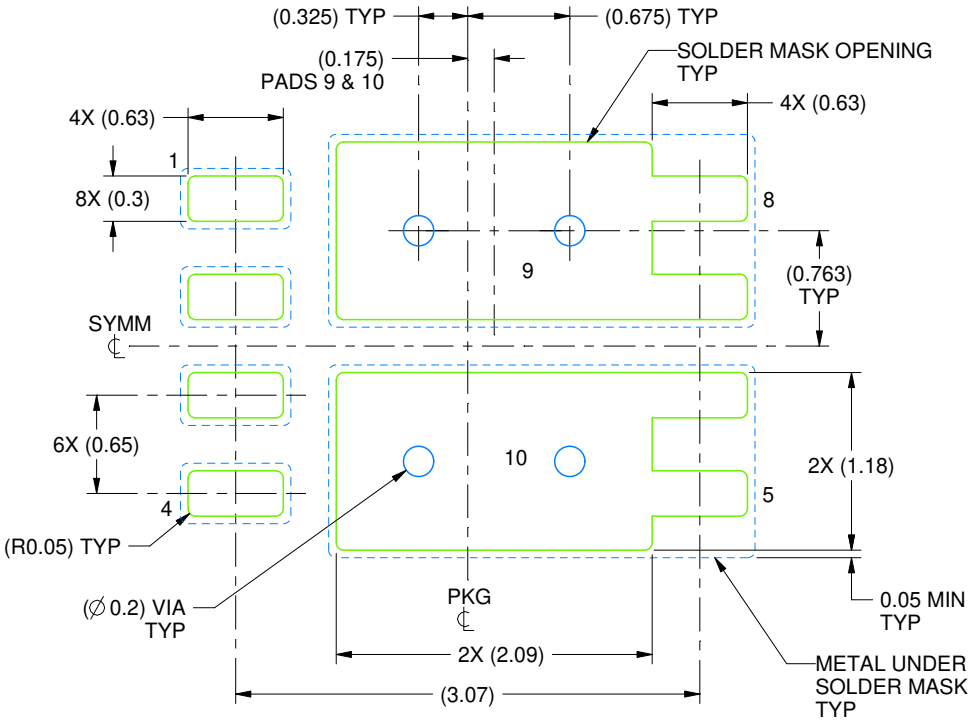
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for optimal thermal and mechanical performance.

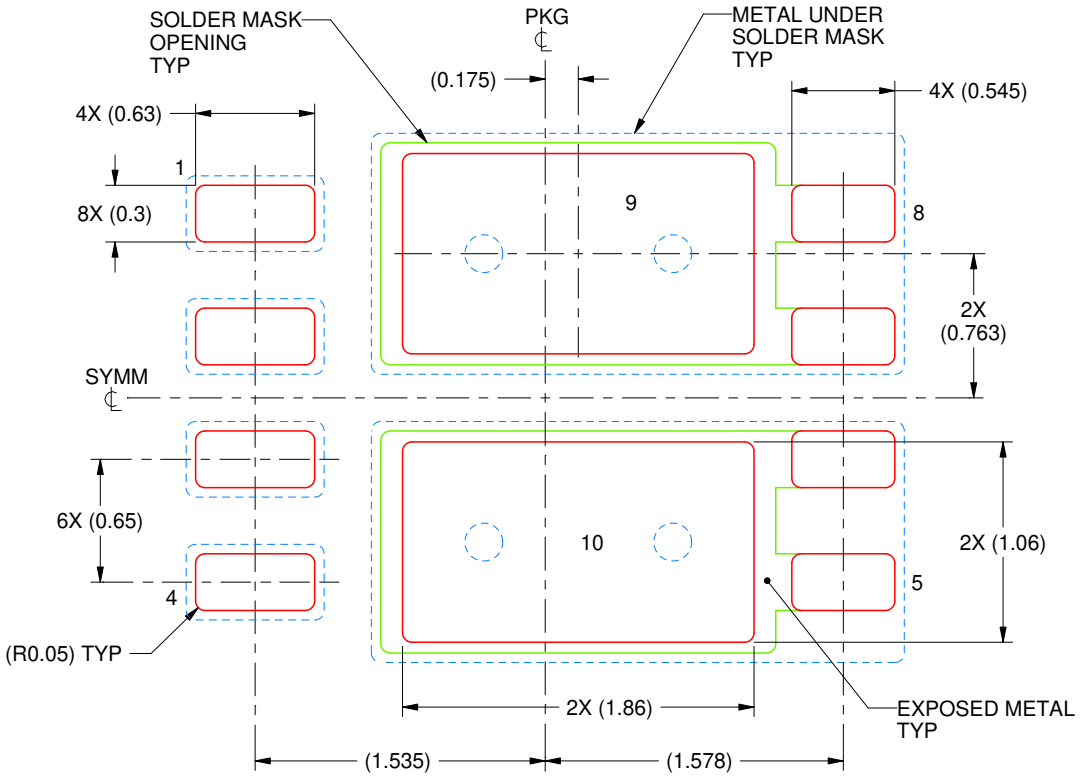


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:20X

4223409/A 12/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PADS 9 & 10
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4223409/A 12/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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