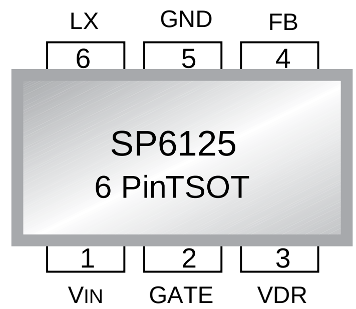
SP6125

High-Voltage, Step Down Controller in TSOT6

FEATURES

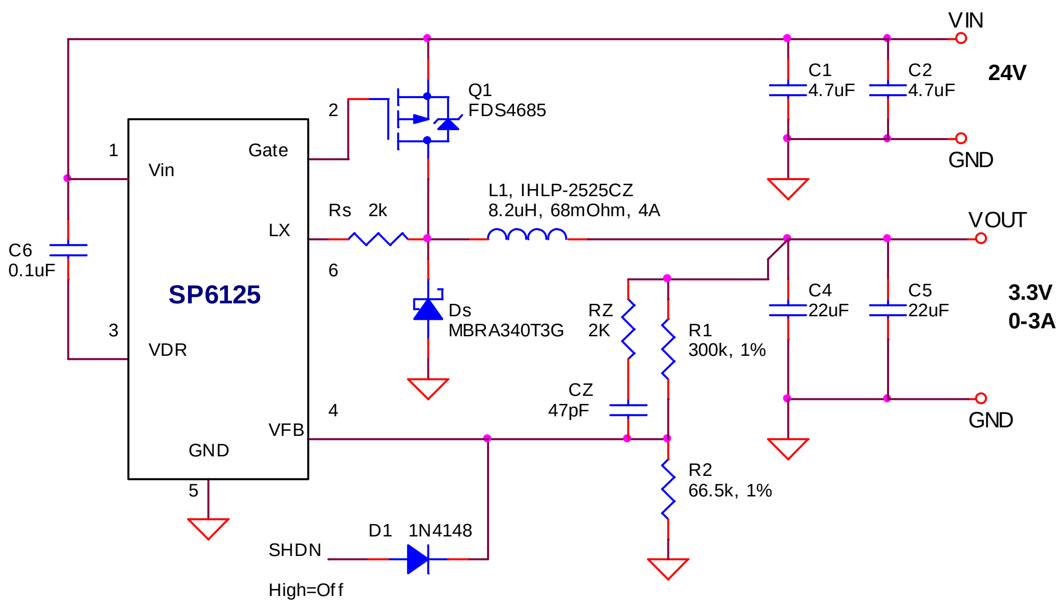
- Wide 4.5V – 29V Input Voltage Range
- Internal Compensation
- Built-in High Current PMOS Driver
- Adjustable Overcurrent Protection
- Internal soft-start
- 300kHz Constant Frequency Operation
- 0.6V Reference Voltage
- 1% output setpoint accuracy
- Lead Free, RoHS Compliant Package: Small 6 pin TSOT



DESCRIPTION

The SP6125 is a PWM controlled step down (buck) voltage mode regulator with VIN feedforward and internal Type-II compensation. It operates from 4.5V to 29V, making is suitable for 5V, 12V, and 24V applications. By using a PMOS driver, this device is capable of operating at 100% duty cycle. The high side driver is designed to drive the gate 5V below VIN. The programmable overcurrent protection is based on high-side MOSFET's ON resistance sensing and allows setting the overcurrent protection value up to 300mV threshold (measured from VIN-LX). The SP6125 is available in a space-saving 6-pin TSOT package making it the smallest controller available capable of operating from 24VDC supplies.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only, and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Input Voltage……...-0.3V to 30V
Lx…………………………………………..…………-2V to 30V
FB…………...-0.3V to 5.5V
Storage Temperature.…………………..……-65 °C to 150 °C
Junction Temperature...................................-40°C to 125°C
Lead Temperature (Soldering, 1…0 sec)……………..300 °C
ESD Rating……………….1kV LX, 2kV all other nodes, HBM

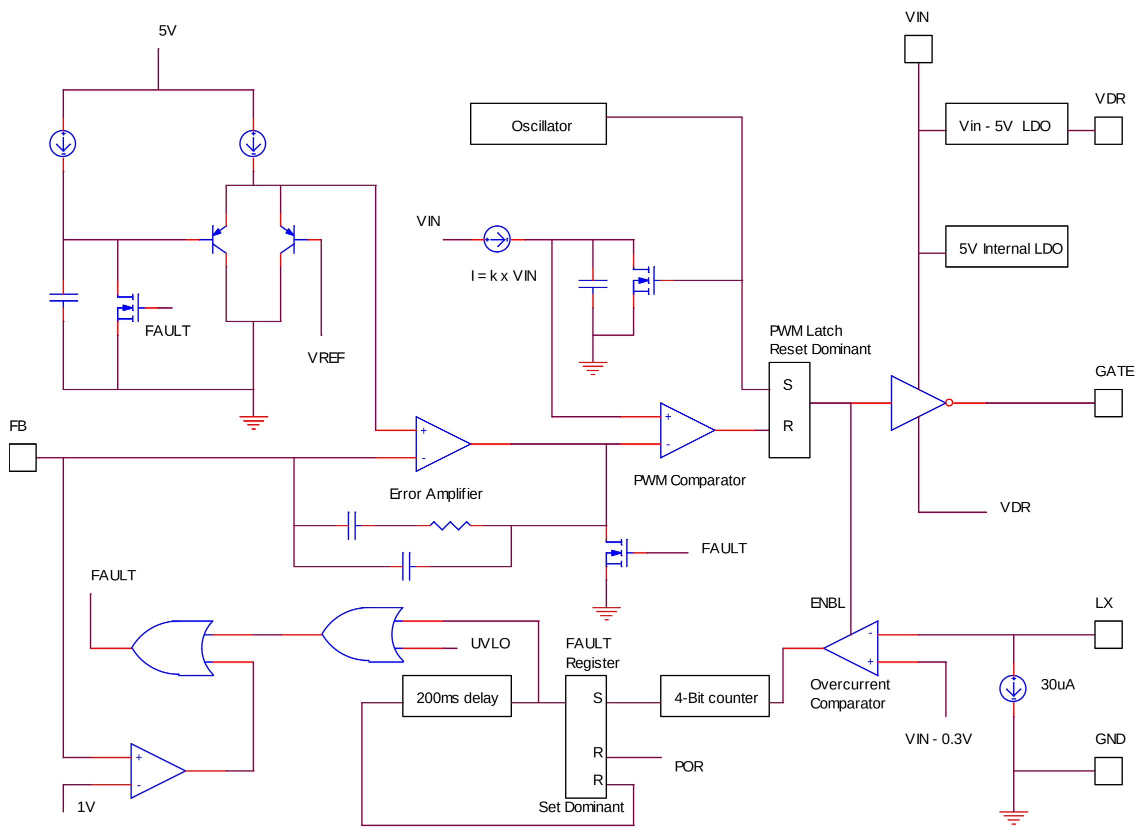
ELECTRICAL SPECIFICATIONS

Specifications are for $T_{AMB}=T_J=25°C$, and those denoted by ♦ apply over the full operating range, -40°C< T_j <125°C. Unless otherwise specified: V_{IN} =4.5V to 29V, C_{IN} = 4.7µF.

PARAMETER	MIN	TYP	MAX	UNITS	♦	CONDITIONS
UVLO Turn-On Threshold	4.2	4.35	4.5	V		0°C< T_j <125°C
UVLO Turn-Off Threshold	4.0	4.2	4.4	V		0°C< T_j <125°C
UVLO Hysterisis		0.2		V		
Operating Input Voltage Range	4.5		29	V		0°C< T_j <125°C
Operating Input Voltage Range	7		29	V	♦	
Operating VCC Current		0.3	3	mA		VFB=1.2V
Reference Voltage Accuracy		0.5	1	%		
Reference Voltage Accuracy		0.5	2	%	♦	
Reference Voltage	0.594	0.6	0.606	V		
Reference Voltage	0.588	0.6	0.612	V	♦	
Switching Frequency	255	300	345	kHz		
Peak-to-peak ramp Modulator		V_{IN}/5		V		
Minimum ON-Pulse Duration		40	100	ns	♦	
Minimum Duty Cycle			0	%		
Maximum Duty Cycle	100			%		
Gate Driver Turn-Off Resistance		50	60	kΩ		Internal resistor between GATE and V_{IN}
Gate Driver Pull-Down Resistance		4	8	Ω		V_{IN}=12V, V_{FB}=0.5V, Measure resistance between GATE and VDR
Gate Driver Pull-up Resistance		3	6	Ω		V_{IN}=12V, V_{FB}=0.7V, Measure resistance between GATE and V_{IN}
V_{IN} - VDR voltage difference	4.5		5.5	V	♦	Measure V_{IN} – VDR, V_{IN}>7V
Overcurrent Threshold	270	300	330	mV		Measure V_{IN} - LX
LX pin Input Current	25	30	35	uA		V_{LX} = V_{IN}
OFF interval during hiccup		200		ms		
Soft start time	3	5	9	ms		VFB=0.58V, measure between V_{IN}=4.5V and first GATE pulse
SHDN Threshold	0.9	1.0	1.1	V	♦	Apply voltage to FB
SHDN Threshold Hysteresis		100		mV		

PIN #	PIN NAME	DESCRIPTION
1	VIN	Input power supply for the controller. Place input decoupling capacitor as close as possible to this pin.
2	GATE	Connect to the gate terminal of the external P-channel MOSFET.
3	VDR	Power supply for the internal driver. This voltage is internally regulated to about 5V below VIN. Place a 0.1uF decoupling capacitor between VDR and Vin as close as possible to the IC.
4	FB	Regulator feedback input. Connect to a resistive voltage-divider network to set the output voltage. This pin can be also used for ON/OFF control. If this pin is pulled above 1V the P-channel driver is disabled and controller resets internal soft start circuit.
5	GND	Ground pin.
6	LX	This pin is used as a current limit input for the internal current limit comparator. Connect to the drain pin of the external MOSFET through an optional resistor. Internal threshold is pre-set to 300mV nominal and can be decreased by changing the external resistor based on the following formula: V_{TRSHLD} = 300mV – 30uA * R

BLOCK DIAGRAM



The SP6125 is a fixed frequency, Voltage-mode, non-synchronous PWM controller optimized for minimum component, small form factor and cost effectiveness. It has been designed for single-supply operation ranging from 4.5V to 29V. SP6125 has Type-II internal compensation for use with Electrolytic or Tantalum output capacitors. For ceramic capacitors Type-III compensation can be implemented by simply adding an R and C between output and Feedback. A precision 0.6V reference, present on the positive terminal of the Error Amplifier, permits programming of the output voltage down to 0.6V via the FB pin. The output of the Error Amplifier is internally compared to a feed-forward (V_{IN}/5 peak-to-peak) ramp and generates the PWM control. Timing is governed by an internal oscillator that sets the PWM frequency at 300kHz.

SP6125 contains useful protection features. Overcurrent protection is based on high-side MOSFET's $R_{DS(ON)}$ and is programmable via a resistor placed at LX node. Under-Voltage Lock-Out (UVLO) ensures that the controller starts functioning only when sufficient voltage exists for powering IC's internal circuitry.

SP6125 Loop Compensation

The SP6125 includes Type-II internal compensation components for loop compensation. External compensation components are not required for systems with tantalum or aluminum electrolytic output capacitors with sufficiently high ESR. Use the condition below as a guideline to determine whether or not the internal compensation is sufficient for your design.

Type-II internal compensation is sufficient if the following condition is met:

$$f_{ESRZERO} < f_{DBPOLE} \quad \text{.................. (1)}$$

where:

$$f_{ESRZERO} = \frac{1}{2.\pi.R_{ESR}.C_{OUT}} \quad \text{.......... (2)}$$

$$f_{DBPOLE} = \frac{1}{2.\pi.\sqrt{L \cdot C_{OUT}}} \quad \text{........... (3)}$$

$$CZ = \frac{\sqrt{L \cdot C}}{1.3 \times R1} \quad \text{........................... (4)}$$

Creating a Type-III compensation Network

The above condition requires the ESR zero to be at a lower frequency than the double-pole from the LC filter. If this condition is not met, Type-III compensation should be used and can be accomplished by placing a series RC combination in parallel with R1 as shown below. The value of CZ can be calculated as follows and RZ selected from table 1.

$f_{ESRZERO} \div f_{DBPOLE}$	RZ
1X	50K
2X	40K
3X	30K
5X	10K
>= 10X	2K

Table1- Selection of RZ

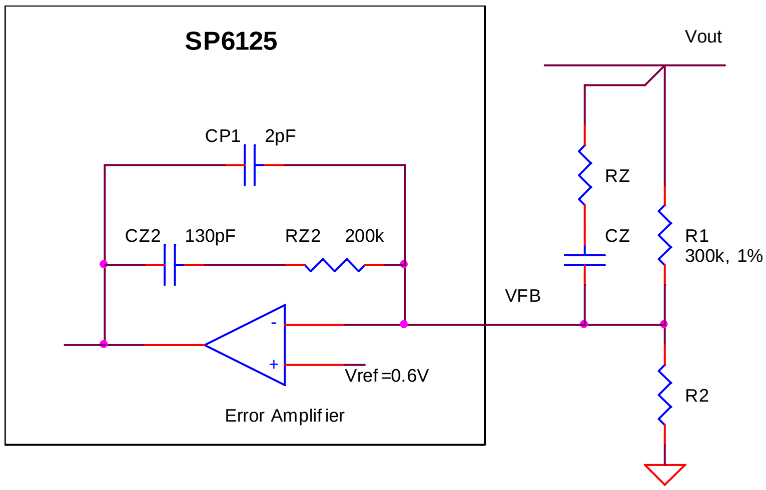


Figure 1- RZ and CZ in conjunction with internal compensation components form a Type-III compensation

Loop Compensation Example 1- A converter utilizing a SP6125 has a 8.2uH inductor and two 22uF/5mΩ ceramic capacitor. Determine whether Type-III compensation is needed.

From equation (2) $f_{ESRZERO}$ = 1.45MHz. From equation (3) f_{DBPOLE} = 8.4kHz. Since the condition specified in (1) is not met, Type-III compensation has to be used by adding external components RZ and CZ. Using equation (4) CZ is calculated 48.7pF (use 47 pF). Following the guideline given in table 1, a 2kΩ RZ should be used.
The steps followed in example 1 were used to compensate the typical application circuit shown on page 1. Satisfactory frequency response of the circuit, seen in figure 2, validates the above procedure.
Loop Compensation Example 2- A converter utilizing a SP6125 has a 8.2uH inductor and a 150uF, 82mΩ Aluminum Electrolytic capacitor. Determine whether Type-III compensation is needed.

From equation (2) $f_{ESRZERO}$ = 13kHz. From equation (3) f_{DBPOLE} = 4.5kHz. Since the condition specified in (1) is not met, Type-III compensation has to be used by adding external components RZ and CZ. Using equation (4) CZ is calculated 89.9pF (use 100pF). Since $f_{ESRZERO} \div f_{DBPOLE}$ is approximately 3, RZ has to be set at 30kΩ.

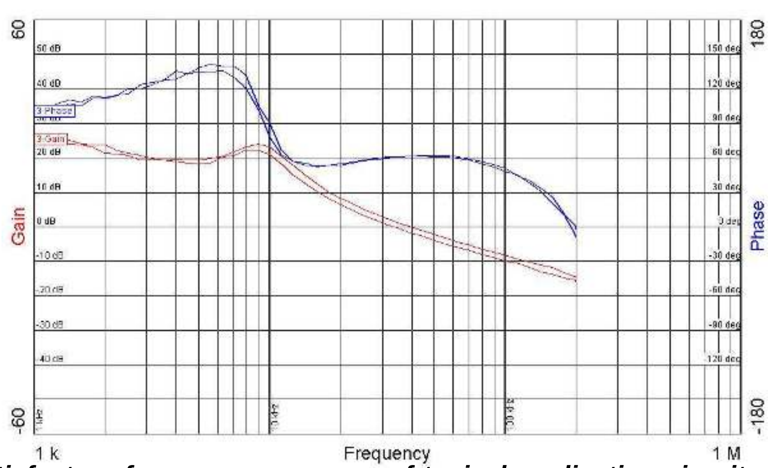


Figure 2- Satisfactory frequency response of typical application circuit shown on page 1. Crossover frequency fc is about 35kHz with a corresponding phase margin of 60 degrees. The two sets of curves, which are essentially identical, correspond to load current of 1A and 2.5A.

Overcurrent protection

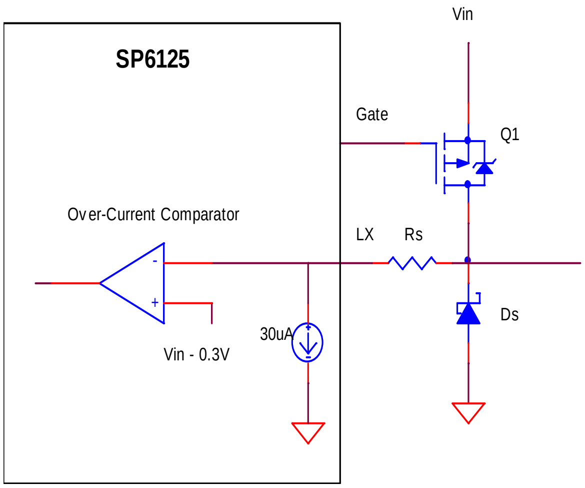


Figure 3- Overcurrent protection circuit

The overcurrent protection circuit functions by monitoring the voltage across the high-side FET Q1. When this voltage exceeds 0.3V, the overcurrent comparator triggers and the controller enters hiccup mode. For example if Q1 has Rds(on)=0.1Ω, then the overcurrent will trigger at I = 0.3V/0.1Ω=3A. To program a lower overcurrent use a resistor Rs as shown in figure 1. Calculate Rs from:

$$Rs = \frac{0.3 - (1.15 \times Iout \times Rds(on))}{30uA} \quad \text{……… (5)}$$

The overcurrent circuit triggers at peak current through Q1 which is usually about 15% higher than average output current. Hence the multiplier 1.15 is used in (5).

Example: A switching MOSFET used with SP6125 has Rds(on) of 0.1Ω. Program the over-current circuit so that maximum output is 2A.

$$Rs = \frac{0.3 - (1.15 \times 2A \times 0.1Ohm)}{30uA}$$

Rs = 2333Ω

Using the above equation there is good agreement between calculated and test results for Rs in the range of 0.5kΩ to 3kΩ. For Rs larger than 3kΩ test results are lower than those predicted by (5), due to circuit parasitics. Therefore maximum value of Rs should be limited to 3kΩ.

Using the ON/OFF Function

The Feedback pin serves a dual role of ON/OFF control. The MOSFET driver is disabled when a voltage greater than 1V is applied at the FB pin. Maximum voltage rating of this pin is 5.5V. The controlling signal should be applied through a small signal diode as shown on page 1. *Please note that an optional 10kΩ bleeding resistor across the output helps keep the output capacitor discharged under no load condition.*

Programming the Output Voltage

To program the output voltage, calculate R2 using the following equation:

$$R2 = \frac{R1}{\left(\frac{Vout}{Vref} - 1\right)}$$

Where:

Vref=0.6 is the reference voltage of the SP6125
R1=200kΩ is a fixed-value resistor that, in addition to being a voltage divider, it is part of the compensation network. In order to simplify compensation calculations, R1 is fixed at 200kΩ.

Soft Start

Soft Start is preset internally to 5ms (nominal). Internal Soft Start eliminates the need for the external capacitor CSS that is commonly used to program this function.

MOSFET Gate Drive

P-channel drive is derived through an internal regulator that generates VIN-5V. This pin (VDR) has to be connected to VIN with a 0.1uF decoupling capacitor. The gate drive circuit swings between VIN and VIN-5 and employs powerful drivers for efficient switching of the P-channel MOSFET.

Power MOSFET Selection

Select the Power MOSFET for Voltage rating BV_{DSS}, On resistance $R_{DS(ON)}$, and thermal resistance Rthja. BV_{DSS} should be about twice as high as VIN in order to guard against switching transients. Recommended MOSFET voltage rating for VIN of 5V, 12V and 24V is 12V, 30V and 40V respectively. $R_{DS(ON)}$, must be selected such that when operating at peak current and junction temperature the Overcurrent threshold of the SP6125 is not exceeded. Allowing 50% for temperature coefficient of $R_{DS(ON)}$ and 15% for inductor current ripple, the following expression can be used:

$$RDS(ON) \leq \left(\frac{300mV}{1.5 \times 1.15 \times Iout} \right)$$

Within this constraint, selecting MOSFETs with lower $R_{DS(ON)}$ will reduce conduction losses at the expense of increased switching losses. As a rule of thumb select the highest $R_{DS(ON)}$ MOSFET that meets the above criteria. Switching losses can be assumed to roughly equal the conduction losses. A simplified expression for conduction losses is given by:

$$Pcond = Iout \times RDS(ON) \times \left(\frac{Vout}{Vin} \right)$$

MOSFET's junction temperature can be estimated from:

$$T = (2 \times Pc \times Rthja) + Tambient$$

Schottky Rectifier selection

Select the Schottky for Voltage rating V_R, Forward voltage V_f, and thermal resistance Rthja. Voltage rating should be selected using the same guidelines outlined for MOSFET voltage selection. For a low duty cycle application such as the circuit shown on first page, the Schottky is conducting most of the time and its conduction losses are the largest component of losses in the converter. Conduction losses can be estimated from:

$$Pc = Vf \times Iout \times \left(1 - \frac{Vout}{Vin} \right)$$

where:
Vf is diode forward voltage at IOUT

Schottky's AC losses due to its switching capacitance are negligible.

Inductor Selection

Select the Inductor for inductance L and saturation current Isat. Select an inductor with Isat higher than the programmed overcurrent. Calculate inductance from:

$$L = (Vin - Vout) \times \left(\frac{Vout}{Vin} \right) \times \left(\frac{1}{f} \right) \times \left(\frac{1}{Irip} \right)$$

where:

VIN is converter input voltage
VOUT is converter output voltage
f is switching frequency
IRIP is inductor peak-to-peak current ripple (nominally set to 30% of IOUT)

Keep in mind that a higher IRIP results in a smaller inductor which has the advantages of small size, low DC equivalent resistance DCR, high saturation current Isat and allows the use of a lower output capacitance to meet a given step load transient. A higher Irip, however, increases the output voltage ripple and increases the current at which converter enters Discontinuous Conduction Mode. The output current at which converter enters DCM is ½ of IRIP. Note that a negative current step load that drives the converter into DCM will result in a large output voltage transient. Therefore the lowest current for a step load should be larger than ½ of IRIP.

Output Capacitor Selection

Select the output capacitor for voltage rating, capacitance and Equivalent Series Resistance (ESR). Nominally the voltage rating is selected to be twice as large as the output voltage. Select the capacitance to satisfy the specification for output voltage overshoot or undershoot caused by current step load. A steady-state output current IOUT corresponds to inductor stored energy of ½ L $IOUT^2$. A sudden decrease in IOUT forces the energy surplus in L to be absorbed by COUT.

This causes an overshoot in output voltage that is corrected by power switch reduced duty cycle. Use the following equation to calculate C_{OUT}:

$$Cout = L \times \left(\frac{I_2^{\ 2} - I_1^{\ 2}}{\text{Vos}^2 \text{ - Vout}^2} \right)$$

Where:

L is the output inductance
I_2 is the step load high current
I_1 is the step load low current
Vos is output voltage including overshoot
V_{OUT} is steady state output voltage

Output voltage undershoot calculation is more complicated. Test results for SP6125 buck circuits show that undershoot is approximately equal to overshoot. Therefore above equation provides a satisfactory method for calculating C_{OUT}.

Select ESR such that output voltage ripple (V_{RIP}) specification is met. There are two components to V_{RIP}: First component arises from charge transferred to and from C_{OUT} during each cycle. The second component of V_{RIP} is due to inductor ripple current flowing through output capacitor's ESR. It can be calculated from:

$$Vrip = Irip \times \sqrt{ESR^2 + \left(\frac{1}{8 \times Cout \times fs} \right)^2}$$

Where:
I_{RIP} is inductor ripple current
f_S is switching frequency
C_{OUT} is output capacitor calculated above

Note that a smaller inductor results in a higher I_{RIP}, therefore requiring a larger C_{OUT} and/or lower ESR in order to meet V_{RIP}.

Input Capacitor Selection

Select the input capacitor for Voltage, Capacitance, ripple current, ESR and ESL. Voltage rating is nominally selected to be twice the input voltage. The RMS value of input capacitor current, assuming a low inductor ripple current (Irip), can be calculated from:

$$Icin = Iout \times \sqrt{D(1 - D)}$$

In general total input voltage ripple should be kept below 1.5% of V_{IN} (not to exceed 180mV). Input voltage ripple has three components: ESR and ESL cause a step voltage drop upon turn on of the MOSFET. During on time capacitor discharges linearly as it supplies I_{OUT} - I_{IN}. The contribution to Input voltage ripple by each term can be calculated from:

$$\Delta V, Cin = \frac{Iout \times Vout \times (Vin - Vout)}{fs \times Cin \times Vin^2}$$

$$\Delta V, ESR = ESR(Iout - 0.5Irip)$$

$$\Delta V, ESL = ESL \frac{(Iout - 0.5Irip)}{Trise}$$

Where Trise is the rise time of current through capacitor

Total input voltage ripple is sum of the above:

$$\Delta V, Tot = \Delta V, Cin + \Delta V, ESR + \Delta V, ESL$$

In circuits where converter input voltage is applied via a mechanical switch excessive ringing may be present at turn-on that may interfere with smooth startup of SP6126. Addition of an inexpensive 100µF Aluminum Electrolytic capacitor at the input will help reduce ringing and restore a smooth startup.

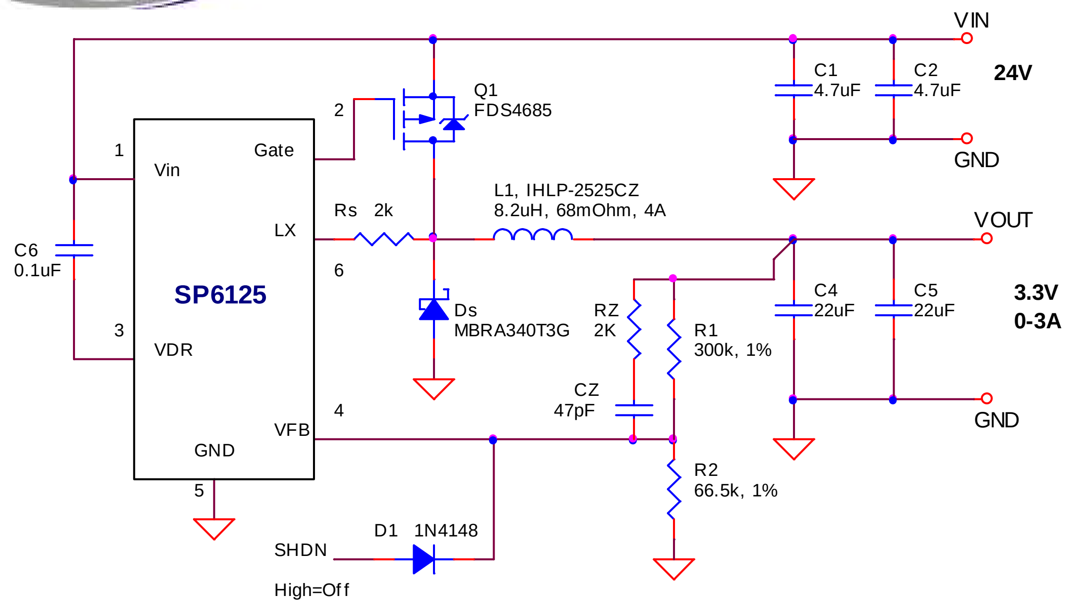


Figure 4- Application circuit for Vin=24V

TYPICAL PERFORMANCE CHARACTERISTICS

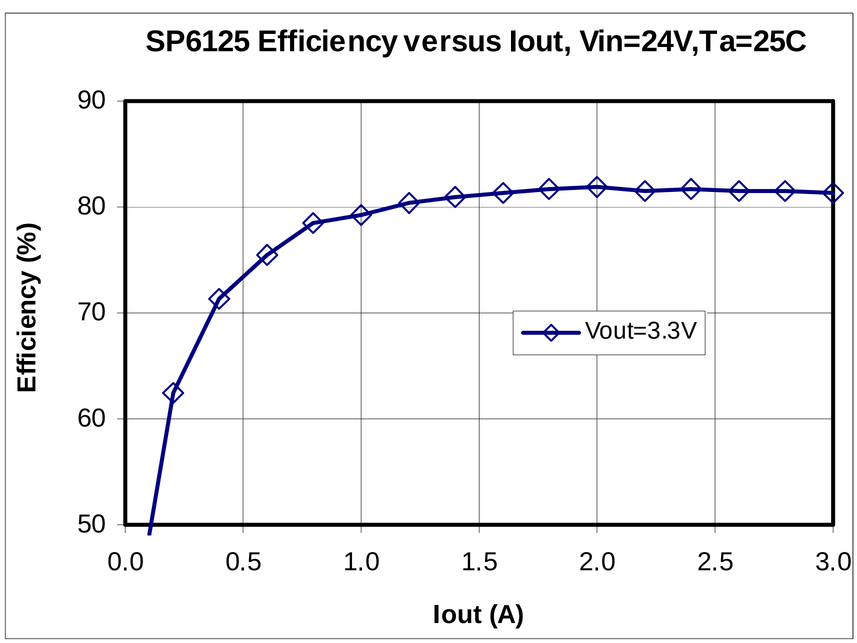


Figure 5- Efficiency at V_{IN} = 24 V , T_A= 25˚C, natural convection

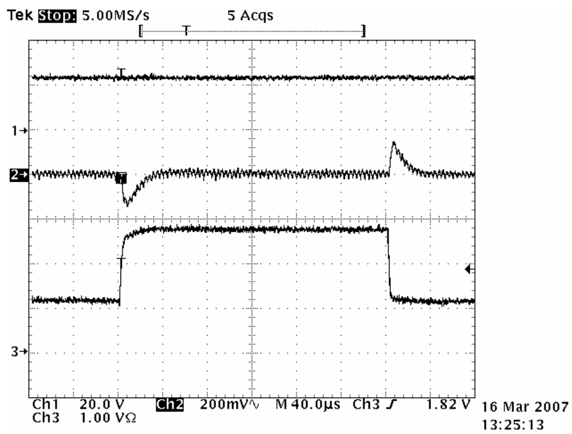


Figure 6- Step load 1.2-2.8A,
ch1: VIN; ch2: VOUT; ch3: IOUT

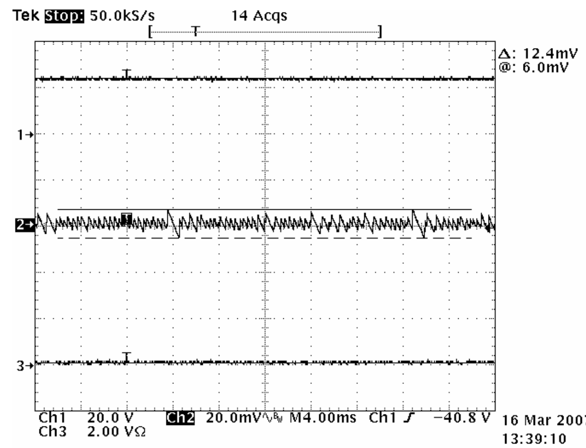


Figure 9- Output ripple at 0A is 12mV,
ch1: VIN; ch2: VOUT; ch3: IOUT

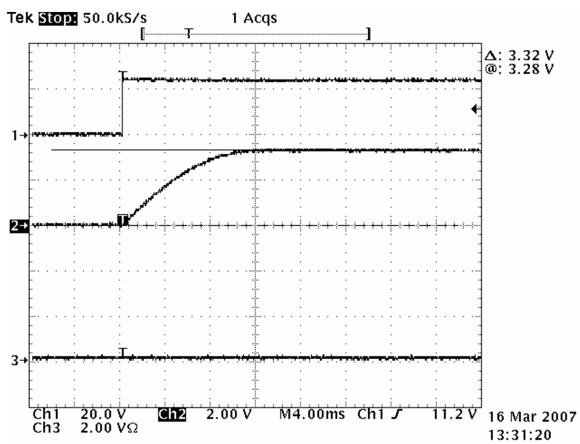


Figure 7- Startup no load,
ch1: VIN; ch2: VOUT, ch3: IOUT

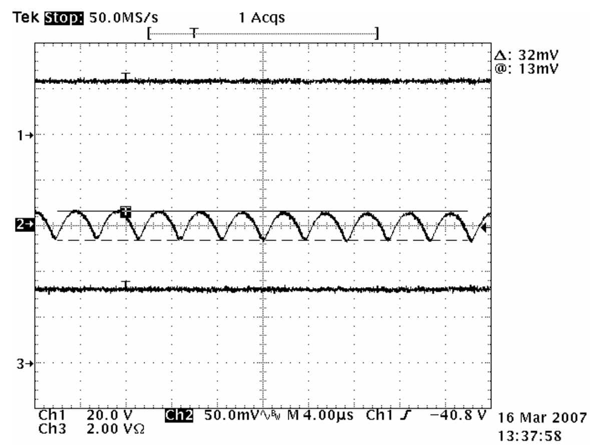


Figure 10- Output ripple at 3A is 32mV,
ch1: VIN; ch2: VOUT; ch3: IOUT

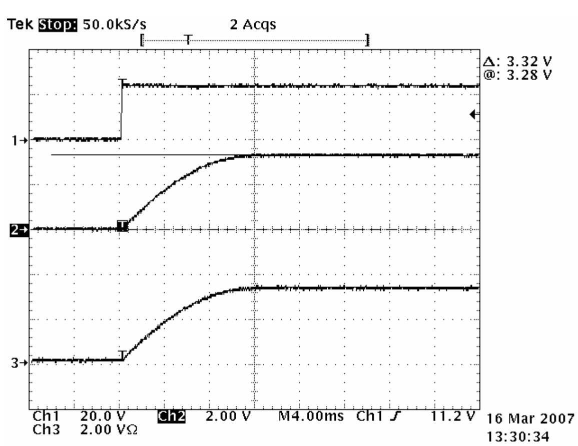
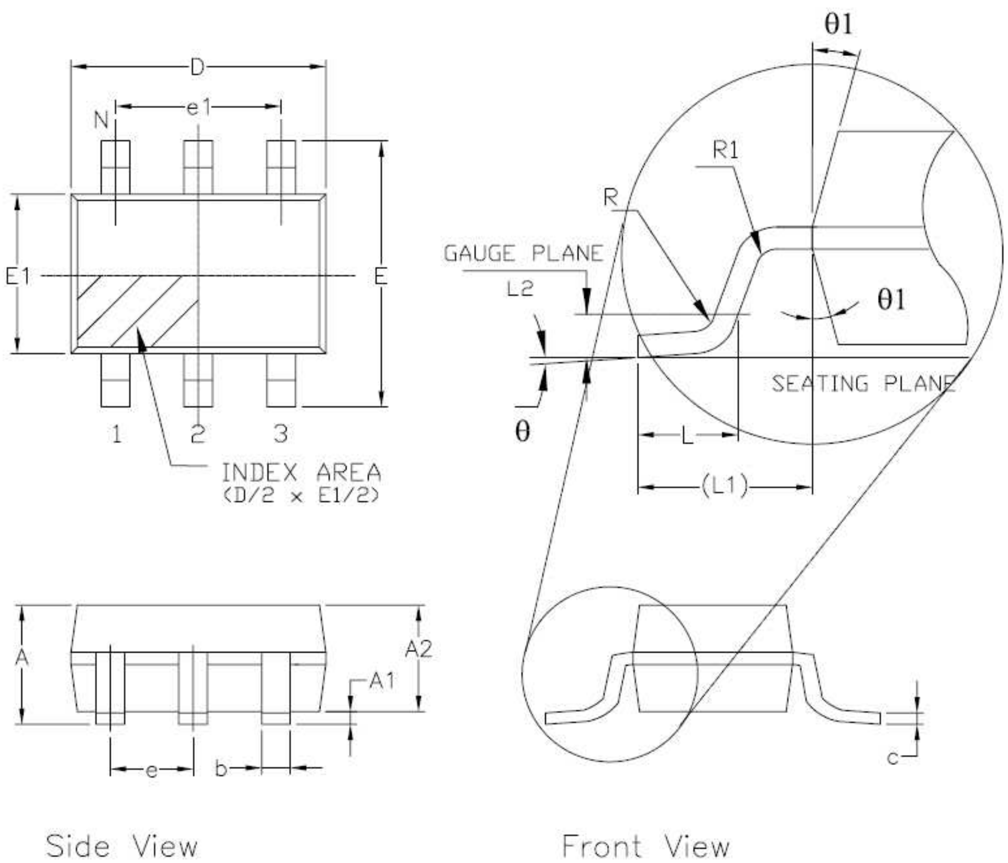


Figure 8- Start up 3A,
ch1: VIN; ch2: VOUT; ch3: IOUT

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/03/05	JL
B	DRAWING FORMAT MODIFICATION	09/13/06	JL



6 Pin TSOT JEDEC MO-193 Variation AA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.10	0.000	—	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
b	0.30	—	0.50	0.012	—	0.020
c	0.08	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.95 BSC			0.038 BSC		
e1	1.90 BSC			0.075 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	6			6		

EXAR Powering Connectivity		EXAR CORPORATION	
		6 PIN TSOT PACKAGE OUTLINE	
Packaging Approval:		Drawing No: 6-PIN TSOT	
By: JL	Date: 09/13/06	Revision: B	Sheet: 1 OF 1

Part Number	Temperature Range	Package
SP6125EK1-L	-40°C to +125°C	(Lead Free) 6 Pin TSOT
SP6125EK1-L/TR	-40°C to +125°C	(Lead Free) 6 Pin TSOT

/TR = Tape and Reel
Pack Quantity for Tape and Reel is 2500

For further assistance:

Email: customersupport@exar.com
EXAR Technical Documentation: http://www.exar.com/TechDoc/default.aspx?

Exar Corporation
Headquarters and
Sales Office
48720 Kato Road
Fremont, CA 94538
main: 510-668-7000
fax: 510-668-7030