

# CBT16212

24-bit bus exchange switch with 12-bit output enables

Rev. 02 — 3 November 2008

Product data sheet

## 1. General description

The CBT16212 provides 24 bits of high-speed TTL-compatible bus switching or exchanging. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBT16212 operates either as a 24-bit bus switch or as a 12-bit bus exchanger, providing data exchange between four signal ports using the port select inputs (S0, S1 and S2).

The CBT16212 is characterized for operation from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

## 2. Features

- $5\ \Omega$  switch connection between two ports
- TTL compatible input levels
- ESD protection:
  - ◆ HBM JESD22-A114E Class 1C exceeds 1500 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Latch-up performance:
  - ◆ JESD78 exceeds 100 mA

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBT16212DGG	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
CBT16212DL	$-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1

4. Functional diagram

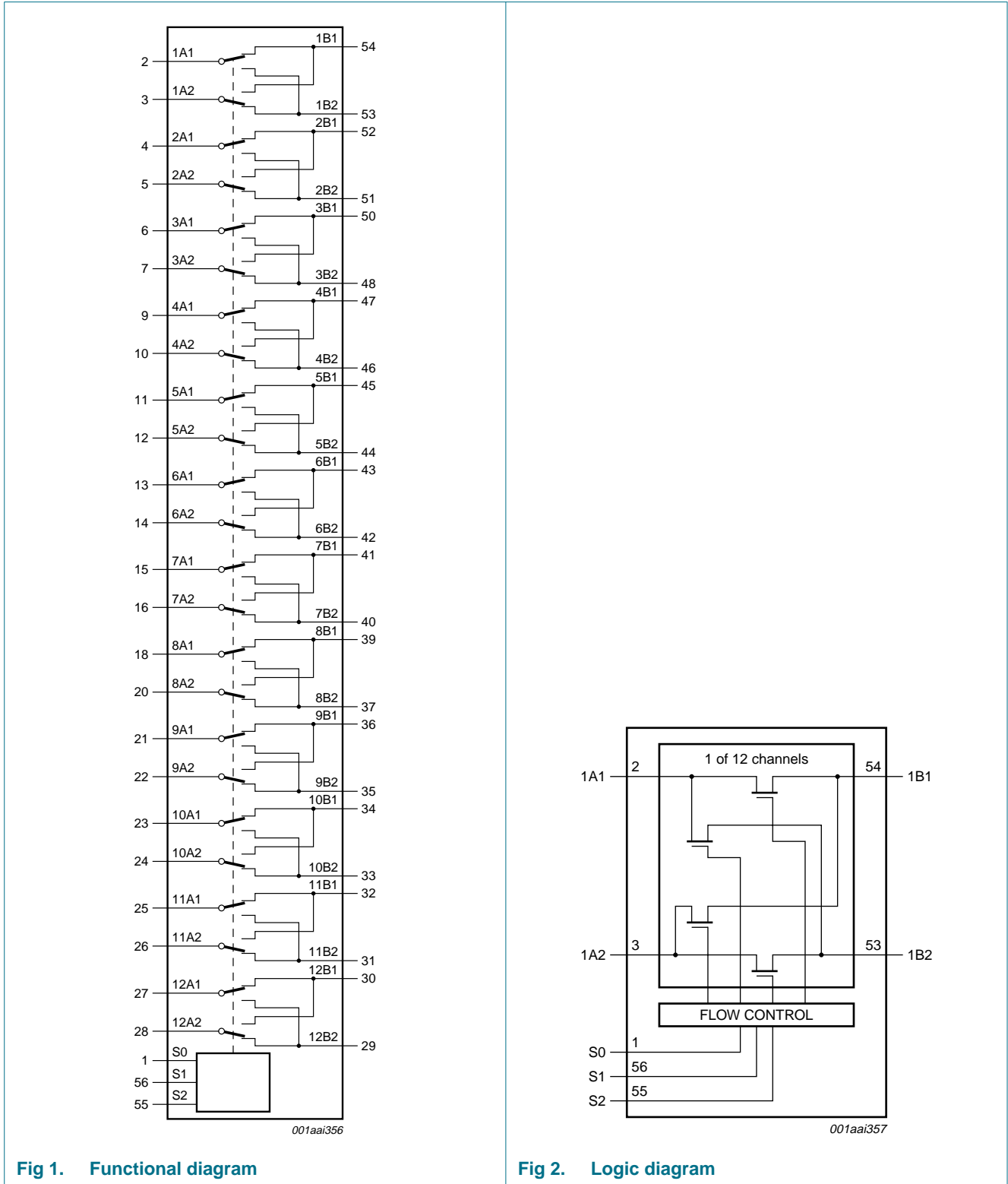
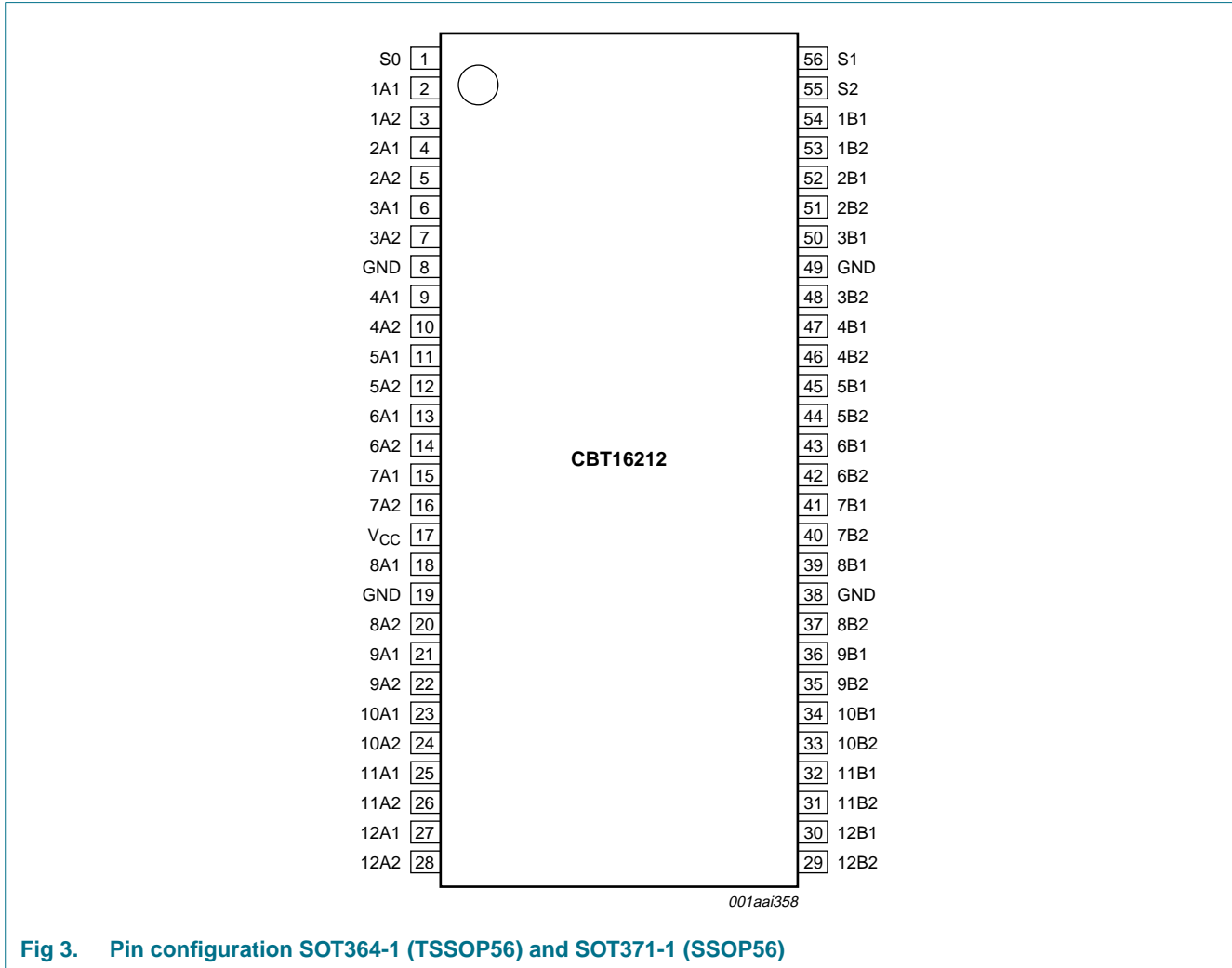


Fig 1. Functional diagram

Fig 2. Logic diagram

## 5. Pinning information

### 5.1 Pinning



**Fig 3. Pin configuration SOT364-1 (TSSOP56) and SOT371-1 (SSOP56)**

### 5.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
S0, S1, S2	1, 56, 55	port select input
1A1 to 12A1	2, 4, 6, 9, 11, 13, 15, 18, 21, 23, 25, 27	A1 port
1A2 to 12A2	3, 5, 7, 10, 12, 14, 16, 20, 22, 24, 26, 28	A2 port
GND	8, 19, 38, 49	ground (0 V)
V <sub>CC</sub>	17	supply voltage
1B1 to 12B1	54, 52, 50, 47, 45, 43, 41, 39, 36, 34, 32, 30	B1 port
1B2 to 12B2	53, 51, 48, 46, 44, 42, 40, 37, 35, 33, 31, 29	B2 port

## 6. Functional description

Table 3. Function selection<sup>[1]</sup>

Port select input			Input/output		Function
S2	S1	S0	nA1	nA2	
L	L	L	Z	Z	disconnect
L	L	H	nB1	Z	nA1 = nB1
L	H	L	nB2	Z	nA1 = nB2
L	H	H	Z	nB1	nA2 = nB1
H	L	L	Z	nB2	nA2 = nB2
H	L	H	Z	Z	disconnect
H	H	L	nB1	nB2	nA1 = nB1 and nA2 = nB2
H	H	H	nB2	nB1	nA1 = nB2 and nA2 = nB1

[1] H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+7.0	V
V <sub>I</sub>	input voltage		<sup>[1]</sup> -0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>O</sub>	output voltage	output at HIGH level or OFF-state	-0.5	+5.5	V
I <sub>O</sub>	output current	output at LOW level	-	128	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C			
		SSOP56 package	<sup>[3]</sup> -	850	mW
		TSSOP56 package	<sup>[4]</sup> -	600	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
- [3] Above 55 °C the value of P<sub>tot</sub> derates linearly with 11.3 mW/K.
- [4] Above 55 °C the value of P<sub>tot</sub> derates linearly with 8 mW/K.

## 8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		4.0	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	V
V <sub>IL</sub>	LOW-level input voltage		-	0.8	V
T <sub>amb</sub>	ambient temperature	operating in free-air	-40	+85	°C

## 9. Static characteristics

**Table 6. Static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
$V_{IK}$	input clamping voltage	$V_{CC} = 4.5\text{ V}$ ; $I_I = -18\text{ mA}$	-	-	-1.2	V	
$I_I$	input leakage current	$V_{CC} = 0\text{ V}$ ; $V_I = 5.5\text{ V}$	-	-	10	$\mu\text{A}$	
		$V_{CC} = 5.5\text{ V}$ ; $V_I = V_{CC}$ or GND	-	-	$\pm 1$	$\mu\text{A}$	
$I_{CC}$	supply current	$V_{CC} = 5.5\text{ V}$ ; $I_O = 0\text{ A}$ ; $V_I = V_{CC}$ or GND	-	-	3	$\mu\text{A}$	
$\Delta I_{CC}$	additional supply current	per port select input pin; $V_{CC} = 5.5\text{ V}$ ; <sup>[2]</sup> one input at 3.4 V, other inputs at $V_{CC}$ or GND	-	-	2.5	mA	
$C_I$	input capacitance	port select input pins; $V_I = 3\text{ V}$ or $0\text{ V}$ ; $V_{CC} = 5.0\text{ V}$ ;	-	4.7	-	pF	
$C_{io(off)}$	off-state input/output capacitance	$V_O = 3\text{ V}$ or $0\text{ V}$ ; $V_{CC} = 0\text{ V}$	-	11.5	-	pF	
$R_{ON}$	ON resistance	$V_{CC} = 4.0\text{ V}$ <sup>[3]</sup>	-	-	-	-	
		$V_I = 2.4\text{ V}$ ; $I_I = 15\text{ mA}$	-	-	21	$\Omega$	
		$V_{CC} = 4.5\text{ V}$ <sup>[3]</sup>	-	-	-	-	-
		$V_I = 0\text{ V}$ ; $I_I = 64\text{ mA}$	-	4	7	$\Omega$	
		$V_I = 0\text{ V}$ ; $I_I = 30\text{ mA}$	-	4	7	$\Omega$	
		$V_I = 2.4\text{ V}$ ; $I_I = 15\text{ mA}$	-	6	12	$\Omega$	

[1] All typical values are measured at  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

[3] Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (A or B) terminals.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{CC} = 4.5\text{ V}$  to  $5.5\text{ V}$ ; for test circuit see [Figure 6](#).

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{pd}$	propagation delay	input A or B to output B or A; see <a href="#">Figure 4</a> <sup>[1][2]</sup>	-	0.25	ns
$t_{en}$	enable time	port select input to output A or B; <a href="#">Figure 5</a> <sup>[3]</sup>	2.4	8.0	ns
$t_{dis}$	disable time	port select input to output A or B; <a href="#">Figure 5</a> <sup>[4]</sup>	2.4	8.0	ns

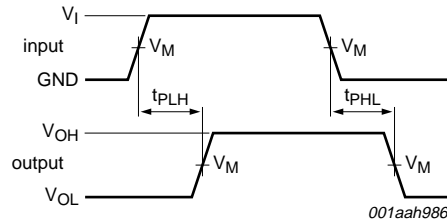
[1] This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical ON resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

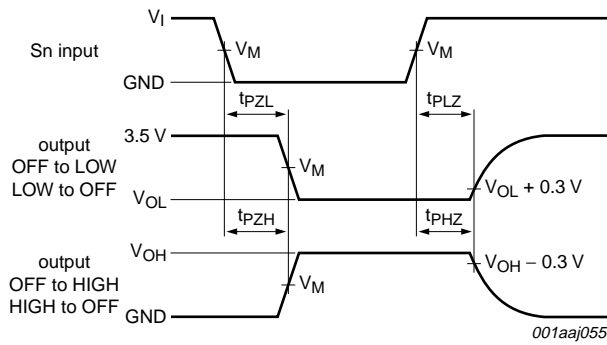
[4]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

11. Waveforms



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 4. Input to output propagation delays

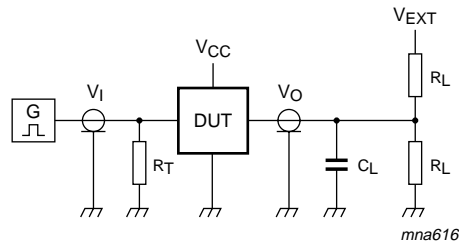


Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 5. Enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
4.5 V to 5.5 V	1.5 V	1.5 V



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 6. Test circuit**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r = t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$
4.5 V to 5.5 V	GND to 3.0 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	open	7.0 V

12. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

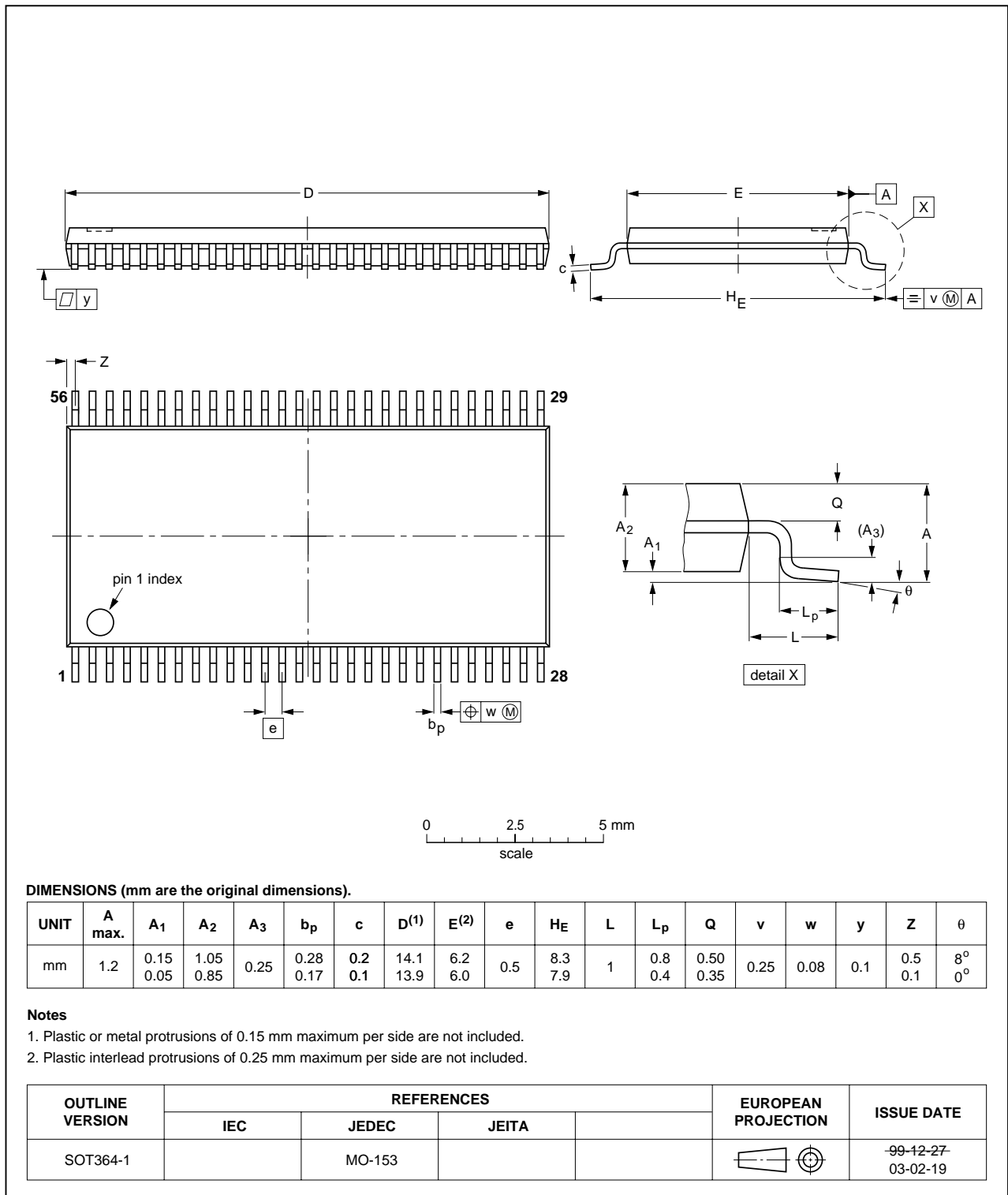


Fig 7. Package outline SOT364-1 (TSSOP56)



SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

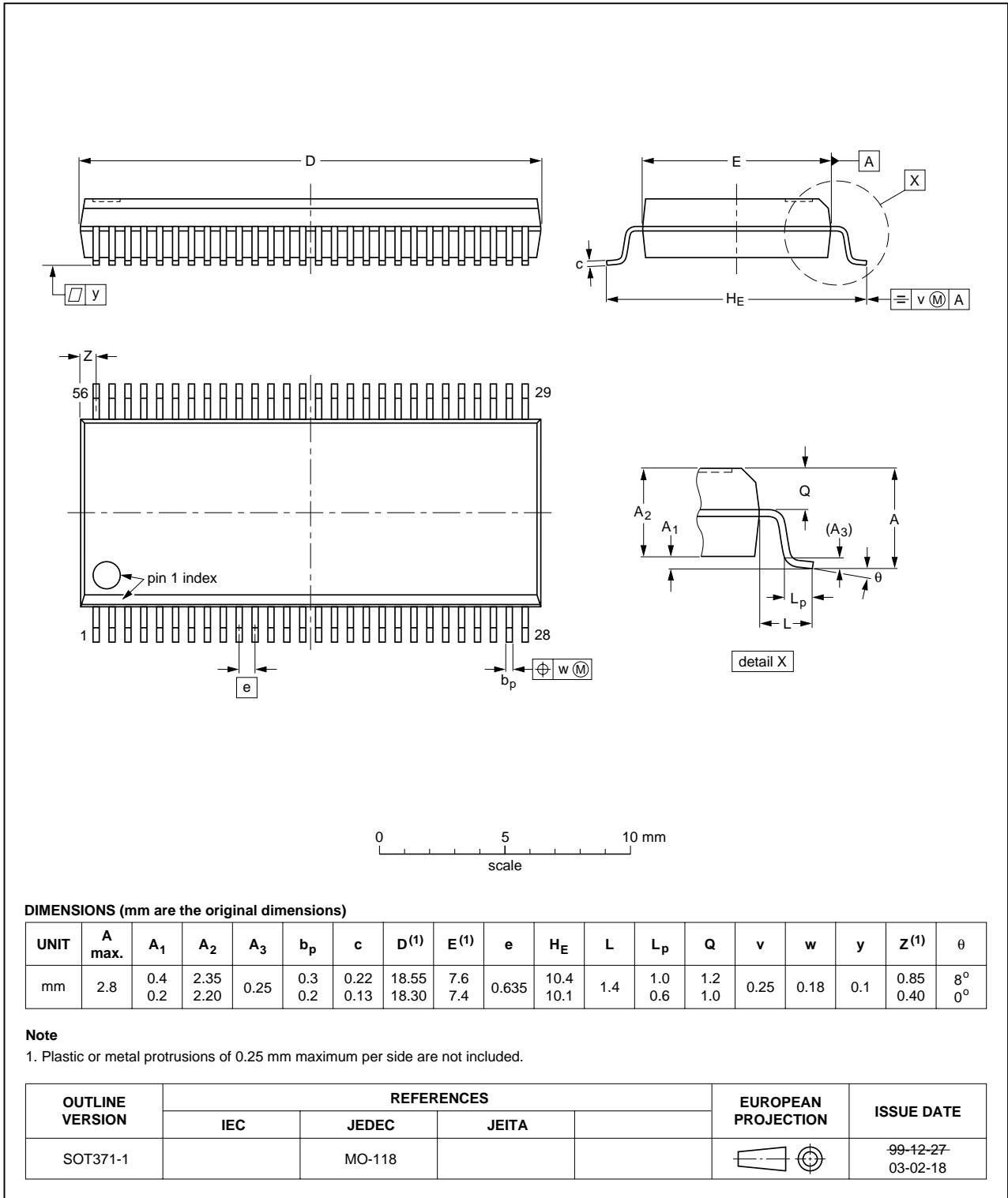


Fig 8. Package outline SOT371-1 (SSOP56)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT16212_2	03112008	Product data sheet	-	CBT16212_1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Table 7 “Dynamic characteristics”</a>: <ul style="list-style-type: none"> <li>– Enable time: min value changed from 3.6 into 2.4.</li> <li>– Disable time: min value changed from 4.5 into 2.4.</li> </ul> </li> </ul>			
CBT16212_1	20010928	Product data	-	-

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### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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**17. Contents**

**1 General description . . . . . 1**

**2 Features . . . . . 1**

**3 Ordering information . . . . . 1**

**4 Functional diagram . . . . . 2**

**5 Pinning information . . . . . 3**

5.1 Pinning . . . . . 3

5.2 Pin description . . . . . 3

**6 Functional description . . . . . 4**

**7 Limiting values . . . . . 4**

**8 Recommended operating conditions . . . . . 4**

**9 Static characteristics . . . . . 5**

**10 Dynamic characteristics . . . . . 5**

**11 Waveforms . . . . . 6**

**12 Package outline . . . . . 8**

**13 Abbreviations . . . . . 10**

**14 Revision history . . . . . 10**

**15 Legal information . . . . . 11**

15.1 Data sheet status . . . . . 11

15.2 Definitions . . . . . 11

15.3 Disclaimers . . . . . 11

15.4 Trademarks . . . . . 11

**16 Contact information . . . . . 11**

**17 Contents . . . . . 12**

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