# ITG-3200 3-Axis Gyro Evaluation Board Application Note Rev 1.1

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## 1. Revision History

| Date | Revision | Description |
|---|---|---|
| 12/07/2009 | 1.0 | Initial release |
| 03/18/2010 | 1.1 | Added assembly drawing, revised schematic, revised BOM, other edits for readability. |

# CONTENTS

## 2. Purpose

This document describes the hardware and circuitry on the ITG-3200 3-Axis Evaluation Board (EVB). It includes applying the EVB to a larger system, understanding the key signals and circuit functions, hardware jumper settings, and port connectors.

### 2.1 Usage

This evaluation board provides three axes of motion processing, comprised of:

- X- , Y-, and Z-Axis gyros with ±2,000 °/sec full-scale range;
- 16-bit digital data measured using on-chip ADCs, transmitted over $I^2C$ interface.

The Evaluation board may be used independently with the $I^2C$ serial communications interface. Alternatively, it may be connected to InvenSense's ARM Evaluation Board (INV-ARMEVB) for connectivity to a host Windows PC using the USB interface.

### 2.2 Related Documents

The following documents are recommended for a more comprehensive understanding of the components and systems described in this Application Note.

- ITG-3200 Product Specification
- ITG-3200 EVB Schematic Diagram (included in this document)

## 3. ITG-3200 3-Axis EVB Overview

The ITG-3200 3-Axis EVB contains the ITG-3200 3-axis digital gyroscope and its interface circuitry. It contains removable and 'solder-across' jumper points that permits several circuit configurations.

Referring to Figure 1, the EVB is populated on its top side only for ease of measurement access. The 20-pin (10 x 2-pin) Main header connector is designed to interface with the InvenSense INV-ARM EVB, which is a host microcontroller board useful for adapting the ITG-3200 3-Axis EVB to a personal computer via its USB port.

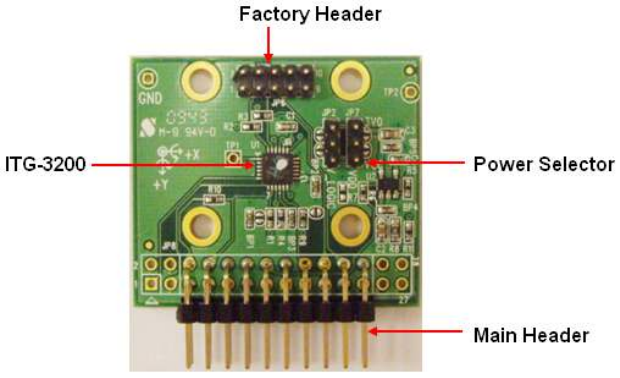


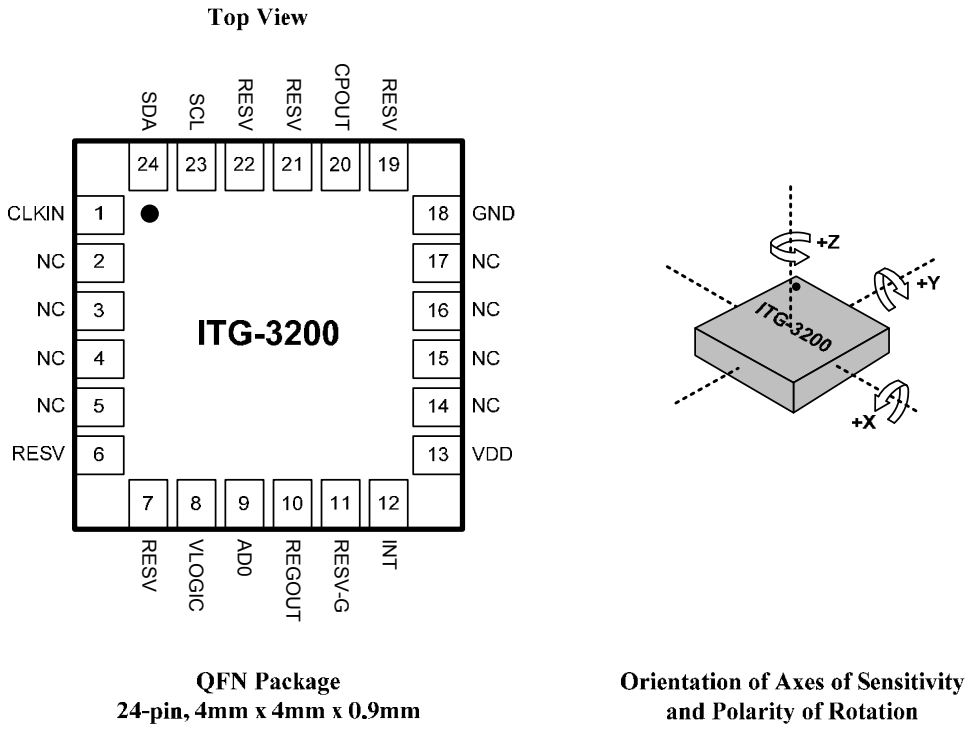

**Figure 1. Top side of the ITG-3200 3-Axis EVB**

The 10-pin (5 x 2-pin) Factory extension header is intended for connecting additional devices to the EVB, such as a digital-output compass, etc. The 3-pin power selection header is used to select which voltage supply is interfaced to the ITG-3200.

The Power select jumper allows the ITG-3200 VDD to be supplied either directly from a 3.3V DC input on the main header, or by a local 3.0V voltage regulator.

### 3.1 ITG-3200 Key Function and Pin-outs

The ITG-3200EVB is a fully-tested evaluation board, providing a quick evaluation of the ITG-3200 X-, Y-, and Z-axis angular rate gyroscope. The ITG-3200 uses InvenSense's proprietary MEMS technology with vertically driven vibrating masses to produce a functionally complete, low-cost motion sensor. All required conditioning electronics are integrated into a single chip measuring 4 x 4 x 0.9mm. It incorporates X-, Y-, and Z-axis low-pass filters and an EEPROM for on-chip factory calibration of the sensor. Factory trimmed scale factors eliminate the need for external active components and end-user calibration. A built-in Proportional-To-Absolute-Temperature (PTAT) sensor provides temperature compensation information. The product is lead-free and Green Compliant. Refer to the ITG-3200 Product Specification for a complete description.




**QFN Package**
**24-pin, 4mm x 4mm x 0.9mm**

**Orientation of Axes of Sensitivity and Polarity of Rotation**

Figure 2. Top View Pin-Out and Sense Orientation of the ITG-3200

## 4. Signal Paths and Configurable Connections

### 4.1 ITG-3200 Functional Block Diagram

The ITG-3200 consists of a MEMS gyroscope, a data-acquisition and digital signal processing section, and a data interface which is compatible to $I^2C$. The data interface is a slave.

VDD and GND are the main supply voltage connections, and VLOGIC is an input which sets the data interface logic-high level. This allows VDD to be different than the IO voltage. Thus, for example, VDD could be 2.6VDC while the data interface could connect to a 1.8V $I^2C$ bus, by using a VLOGIC of 1.8V. REGOUT is for connecting the (nominally) 1.7V internal voltage regulator to a bypass capacitor. CPOUT is for connecting a charge pump capacitor to the internal charge pump.

INT is the ITG-3200 interrupt and may be software configured to a variety of modes. AD0 is the LSB of the $I^2C$ device address, so that when it is tied logic-low, the ITG-3200 address is 68h, and when logic-high (VLOGIC) the ITG-3200 address is 69h.

**Refer to the ITG-3200 product specification for power-on-timing waveforms for VDD and VLOGIC.**

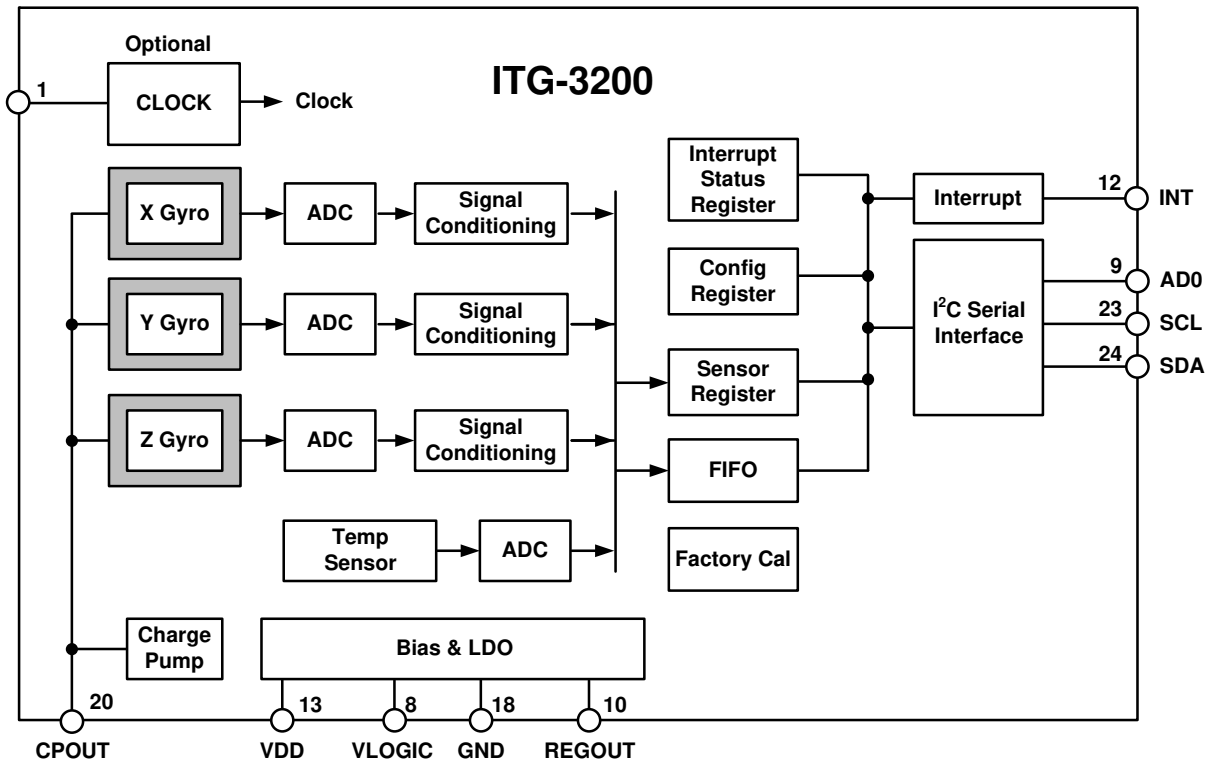
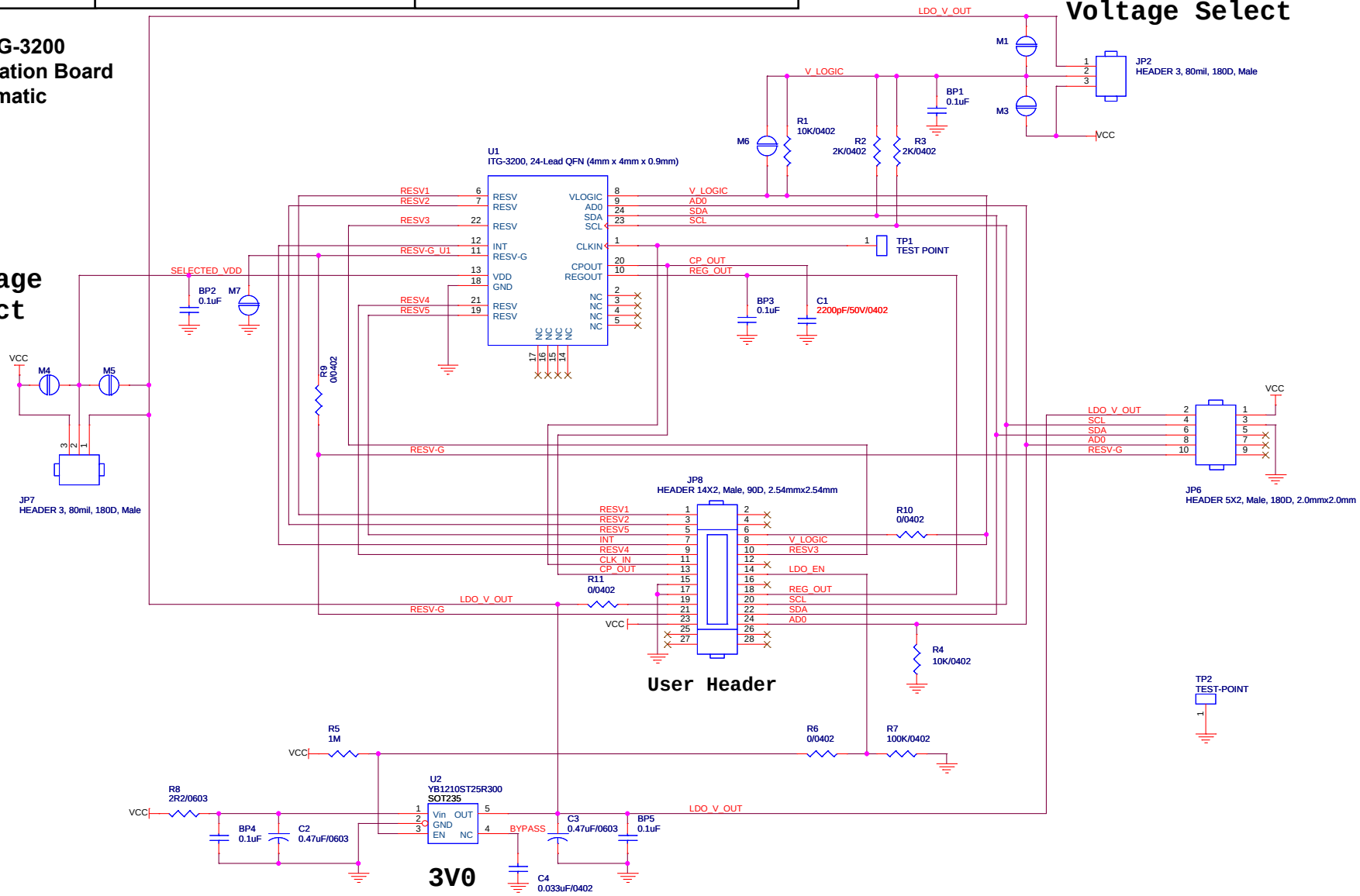



**Figure 3: ITG-3200 Functional Block Diagram**

## 4.2 ITG-3200 Evaluation Board Schematic

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Title: ITG-3200 EVB
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Date: Thursday, March 18, 2010 | Sheet 1 of 1

### 4.3 Bill of Materials (Parts Stuffing List) for ITG-3200 EV Board

Parts Stuffing BOM for ITG-3200 EV Board. Also refer to Assembly Drawing for ITG-3200 EV Board

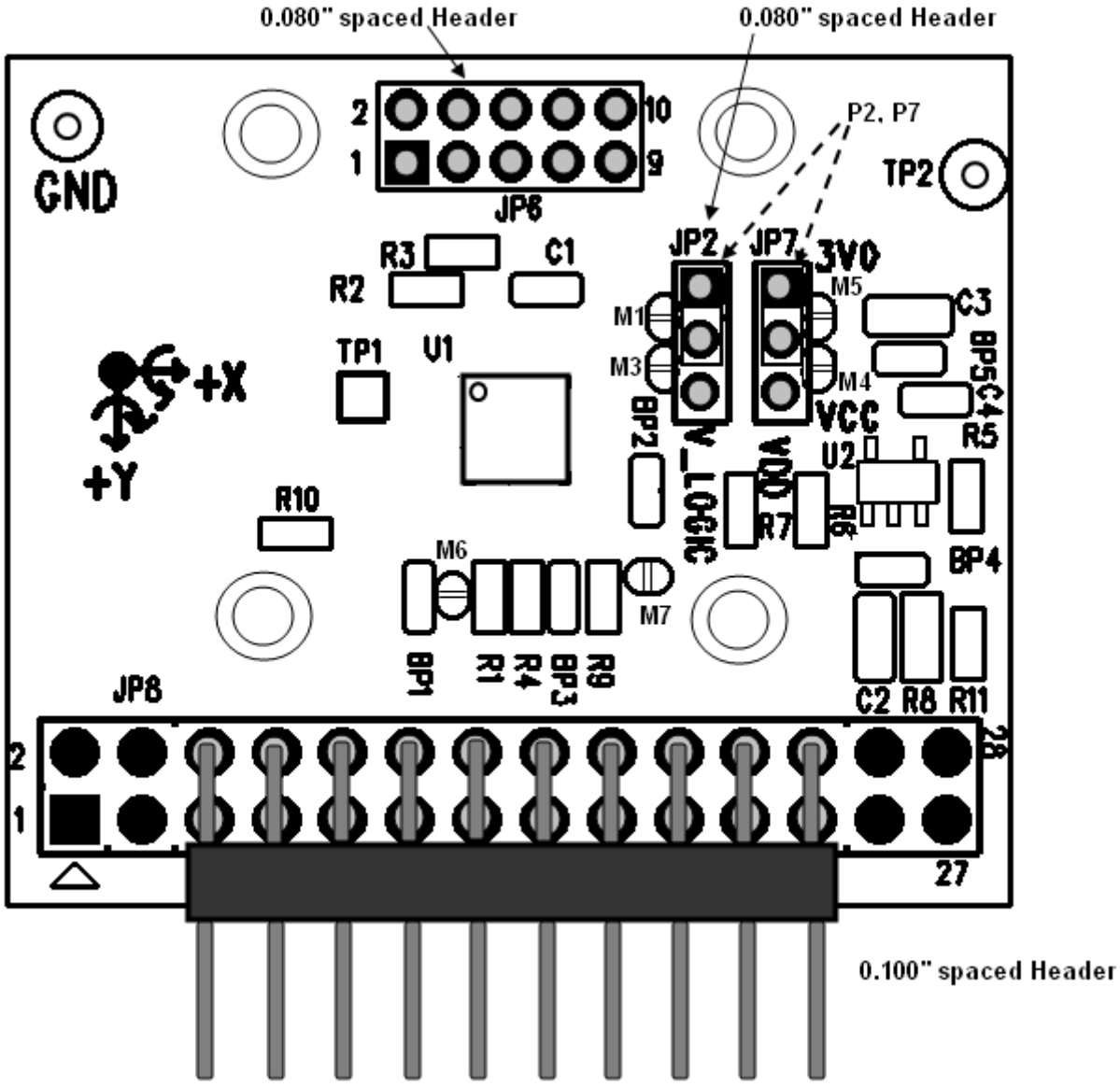
**Table 1. Parts stuffing list the ITG-3200 EVB. Only the top side requires component assembly**

| Item | Quantity | Reference | Part | PCB Footprint |
|---|---|---|---|---|
| 1 | 5 | BP1,BP2,BP3,BP4,BP5 | 0.1uF | 402 smt |
| 2 | 1 | C1 | 2200pF/50V | 402 smt |
| 3 | 2 | C2,C3 | 0.47uF/0603 | 603 smt |
| 4 | 1 | C4 | 0.033uF | 402 smt |
| 5 | 2 | JP2,JP7 | HEADER 3 pin, 80mil, 180D, Male | 3-pin 2mm header |
| 6 | 2 | P2,P7 | PLUG 80mil 2-pin Short circuit plug | Plugs to JP2, JP7 |
| 7 | 1 | JP6 | HEADER 5X2 pin, Male, 180D, 2.0mmx2.0mm | SIP2X5N2 |
| 8 | 1 | JP8 | HEADER 10X2 pin, Male, 90D, 2.54mmx2.54mm | HDB2X10NRA |
| 9 | 4 | R1, R2,R3,R4 | 10K | 402 smt |
| 10 | 1 | R5 | 1M | 402 smt |
| 11 | 1 | R8 | 2R2/0603 | 603 smt |
| 12 | 2 | R6, R10 | 0 Ohm | 402 smt |
| 13 | 1 | U1 | ITG-3200 | QFN-24 |
| 14 | 2 | R9, R7 | DO NOT STUFF | 0402 smt |
| 16 | 1 | U2 | YB1210-ST25R300, 3.0V Regulator[1] | SOT-235 |
| 17 | 1 | M7 | Solder across Jumper | Split oval |
| 18 | 5 | M1, M3, M4, M5, M6 | Do not solder across Jumper | Split oval |
| 19 | 1 | Blank PCB | ITG-3200 EVB REV B | |

Note 1: *www.yobon.com.tw*

### 4.4 Assembly Drawing for ITG-3200 EV Board

Figure 4. ITG-3200 EV Board Assembly Drawing. Follow the Parts Stuffing List for assembly instructions.



### 4.5 Power Supply Connections

JP2 and JP7 are 3 header-pin plug-in jumpers which allow users to select between the on-board LDO and an external DC supply to the ITG-3200. For details, please refer to Table 2. Power Selection Jumpers.

The on-board 3.0V LDO (Low-dropout voltage regulator) is a low-noise part. Its output is called 3V0 on the schematic, and using it will assure that the gyroscope and accelerometer performance will meet the intended specifications.

Selecting the raw VCC line to power the chip is generally done while designing and evaluating with an embedded platform, where the host processor and related electronics need full control over the motion processing chip's power supply. When the user intends to use the on board LDO 3V0 power, the external VCC must be higher than 3.7V to ensure the LDO works properly. If the user provides VCC with 5V, JP2 and JP7 must be set as "1-2 short" to enable the on-board 3.0V LDO. The ITG-3200 VDD and VLOGIC operation range is 2.1V to 3.6V.

**Refer to the ITG-3200 product specification for power-on-timing waveforms for VDD and VLOGIC.**

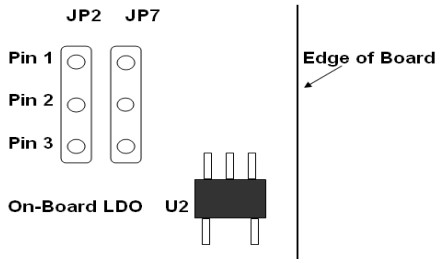



Figure 5. JP2 and JP7 Pin-out

### 4.6 ITG-3200 EVB Connector Signals Description

**Table 2. Power Selection Jumpers (use P2, P7 to short pins as required)**

| JP2 Pin Number | Signal Description |
|---|---|
| 1-2 short | ITG-3200 VLOGIC = 3V using on board LDO |
| 2-3 short | ITG-3200 VLOGIC = VCC (from external) |
| **JP7 Pin Number** | **Signal Description** |
| 1-2 short | ITG-3200 VDD = 3V using on-board LDO |
| 2-3 short | ITG-3200 VDD = VCC (from external) |

**Table 3. "Main Header" User Interface Signals**

| JP8 Pin Number | Signal Name | Signal Description |
|---|---|---|
| 1 | RESV1 | Reserved. Do not connect to this pin. |
| 3 | RESV2 | Reserved. Do not connect to this pin. |
| 5 | RESV5 | Reserved. Do not connect to this pin. |
| 7 | INT | ITG-3200 pin 12 interrupt output to host controller |
| 9 | RESV4 | Reserved. Do not connect to this pin. |
| 11 | CLKIN | ITG-3200 pin 1 external clock input |
| 13 | CPOUT | ITG-3200 pin 20 (charge pump capacitor) |
| 15 | GND | GND |
| 17 | GND | GND |
| 19 | | 3V on-board LDO (regulated DC) output |
| 21 | RESV-G | Reserved. Do not connect to this pin. |
| 23 | VCC | VCC from ARM-7 Controller Board or external 3.3V at >100mA |
| 25 | NC | Not Connected |
| 27 | NC | Not Connected |
| 2 | NC | Not Connected |
| 4 | NC | Not Connected |
| 6 | | Do not connect to this pin. |
| 8 | VLOGIC | VLOGIC DC Input, ITG-3200 pin 8, sets $I^2C$ bus logic levels |
| 10 | RESV3 | Reserved. Do not connect to this pin. |
| 12 | NC | Not Connected |
| 14 | LDO_EN | EVB on-board 3V LDO enable (when pulled to VCC) |
| 16 | NC | Not Connected |
| 18 | REGOUT | ITG-3200 pin 10, on-chip regulator bypass capacitor |
| 20 | SCL | ITG-3200 pin 23 $I^2C$ clock line |
| 22 | SDA | ITG-3200 pin 24 $I^2C$ data line |
| 24 | AD0 | ITG-3200 pin 9 $I^2C$ Address bit zero |
| 26 | NC | Not Connected |
| 28 | NC | Not Connected |

**Table 4. Extended Factory Connector pin functions**

| JP6 Pin Number | Signal Name | Signal Description |
|---|---|---|
| 1 | VCC | Power from ARM-7 controller board or external 3.3V at >100mA |
| 3 | GND | GND |
| 5 | NC | Not Connected |
| 7 | NC | Not Connected |
| 9 | NC | Not Connected |
| 2 | LDO_V_OUT | 3V Output from LDO |
| 4 | SCL | ITG-3200 $I^2C$ clock line |
| 6 | SDA | ITG-3200 $I^2C$ data line |
| 8 | AD0 | ITG-3200 $I^2C$ Address bit zero |
| 10 | RESV-G | Reserved. Do not connect to this pin. |

### 4.7 Serial Bus Levels, Speeds and Terminations

The ITG-3200 supports fast mode $I^2C$ up to 400Hz. The $I^2C$ bus open-drain pull up resistors are R2 and R3 for SDA and SCL; both are 2.2kohm connected to either 3.0V or the externally provided VCC. The pull up level is selected by JP2. Please refer to Table 2. Power Selection Jumpers.

### 4.8 Solder-Across "M" Jumpers

For fast and permanent configuration connections, a set of solder-across jumpers are provided.

### 4.9 Table 5. Solder-Across "M" Jumpers – what they do and how to connect

| M Number | M Jumper function |
|---|---|
| 1 | Shorts JP2 pins 1-2 to set ITG-3200 VLOGIC = 3.0V using on board LDO |
| 3 | Shorts JP2 pins 2-3 to set ITG-3200 VLOGIC = VCC externally supplied voltage |
| 4 | Shorts JP7 pins 2-3 to set ITG-3200 VDD = VCC externally supplied voltage |
| 5 | Shorts JP7 pins 1-2 to setITG-3200 VDD = 3.0V using on board LDO |
| 6 | Pulls ITG-3200 VLOGIC pin 8 to V_LOGIC supply. It is in parallel with R1 |
| 7 | Shorts ITG-3200 pin 11 as required by Product Specification. |

## 5. Data Gathering Options

The ITG-3200 Digital Sensor Data is available at the Main Header connector. Alternately, for connectivity with a host PC, an InvenSense ARM Interface Board may also be used.

### 5.1 Connection to ARM7 Interface EVB

For communications via USB to a host computer, the ITG-3200EVB may be connected to InvenSense's ARM7 Microprocessor Interface board, the INV-ARMEVB. It serves as an interface between a Windows PC USB port, and the ITG-3200 EVB Main header.

The following photo shows the connection of ITG-3200 to INV-ARMEVB. Connection between the two boards is made via the Main header connector.

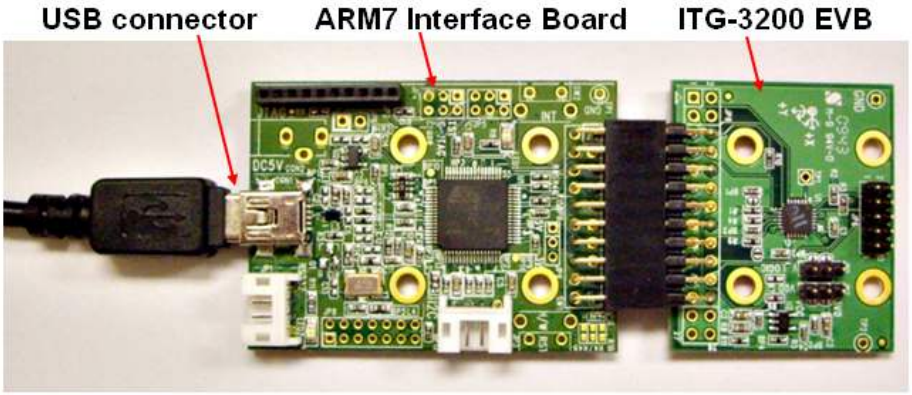



Figure 6: Connect ITG-3200 to ARM Board

### 5.2 Use of ITG-3200 without ARM EVB board

$I^2C$ signals are available on JP8. The user may develop tools to communicate with the ITG-3200. There is no bus mode selection setting required.

## 6. Special Instructions

### 6.1 Electrostatic Discharge Sensitivity

The ITG-3200 gyro can be permanently damaged by an electrostatic discharge. Proper ESD precautions for handling and storage are recommended.

## 7. Mechanical Dimensions

The ITG-3200EVB is a 4 layer PCB with 32mm x 38mm overall dimensions. The mounting holes are arranged to fit 19.56mm x 18.54 mm fixture screw centers, offset from the edge of the board by 9.22mm and 3.05mm as shown.

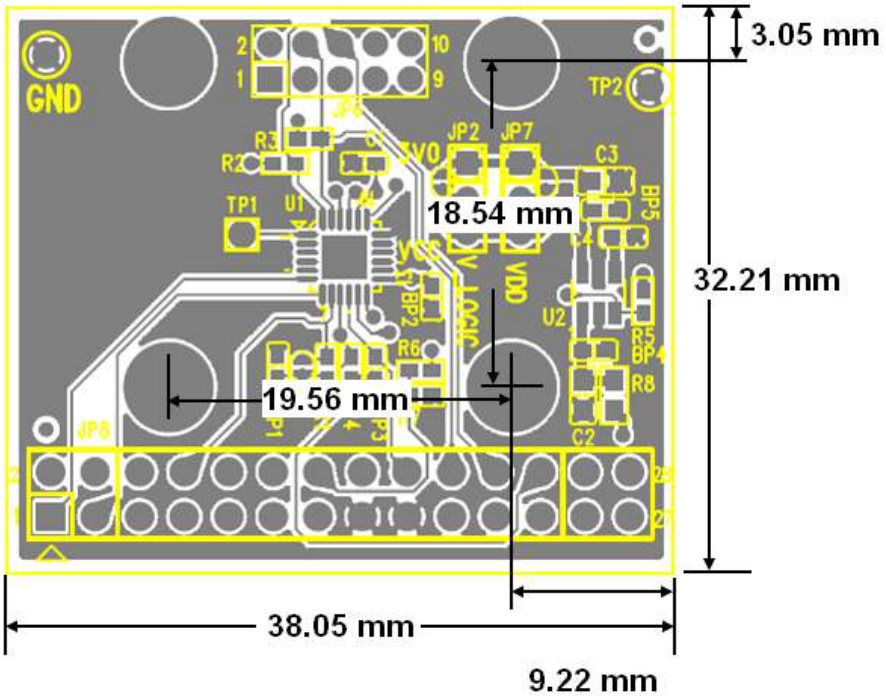



**Figure 7: ITG-3200 Dimensions, Top Side shown**