



**4-BIT D
FLIP-FLOP**

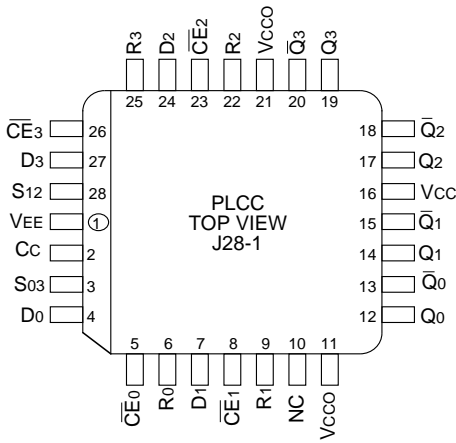
**SY10E131
SY100E131**

- 1100MHz min. toggle frequency
- Extended 100E VEE range of -4.2V to -5.5V
- Differential output
- Individual and common clocks
- Individual asynchronous reset
- Paired asynchronous sets
- Fully compatible with Industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E131
- Available in 28-pin PLCC package

The SY10/100E131 are high-speed quad master slave D-type flip-flops with differential outputs designed for use in new, high-performance ECL systems. The flip-flops may be individually clocked by holding Cc (Common Clock) at a logic LOW and then using the four individual \overline{CE} (Clock Enable $\overline{CE}_0-\overline{CE}_3$) inputs to accomplish such clocking. Alternatively, all four flip-flops can be clocked in common by holding the \overline{CE} inputs LOW and then using Cc to clock the data. In the common clock mode, the \overline{CE} input acts as a control that passes the Cc signal to the flip-flop. Data is clocked into the flip-flop on the rising edge of the output of the logical OR operation between \overline{CE} and Cc (data enters the master when both Cc and \overline{CE} are LOW and data transfers to the slave when either \overline{CE} or Cc, or both, go HIGH).

Asynchronous set and reset controls are provided. The reset controls are individual and the set controls are pairwise.

Pin	Function
D0-D3	Data Inputs
$\overline{CE}_0-\overline{CE}_3$	Clock Enables (Individual)
R0-R3	Resets
Cc	Common Clock
S03, S12	Sets (paired)
Q0-Q3	True Outputs
$\overline{Q}_0-\overline{Q}_3$	Inverting Outputs
Vcco	Vcc to Output



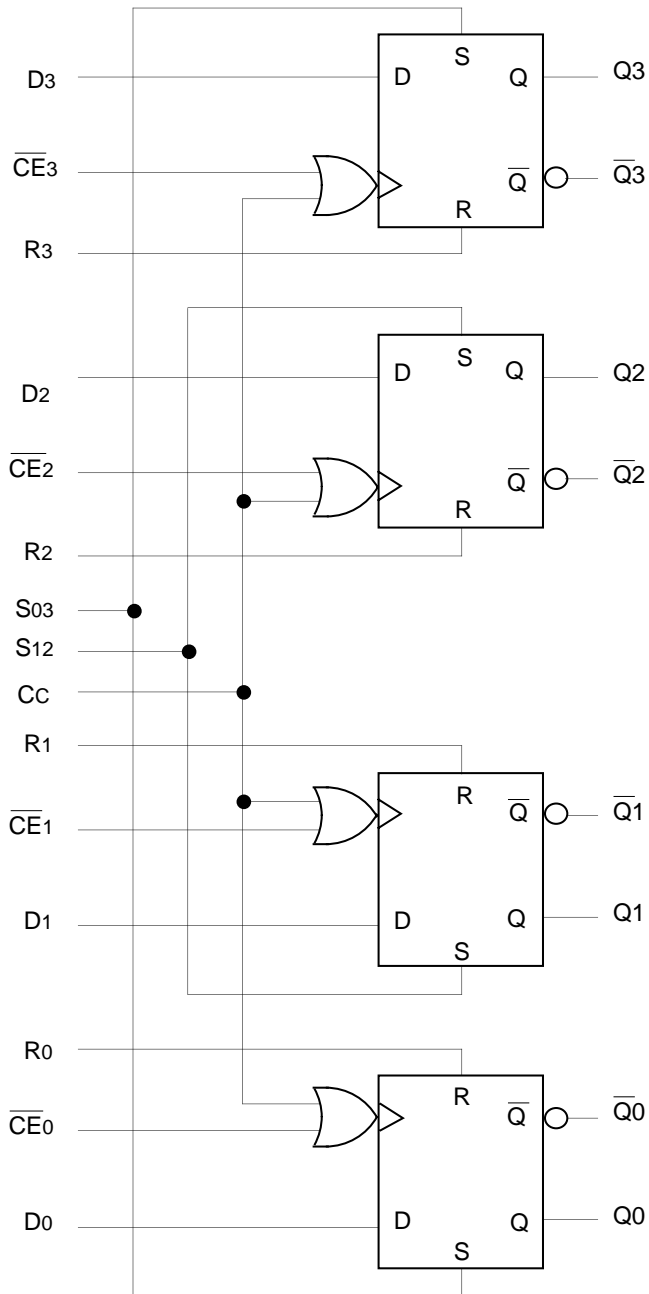
28-Pin PLCC (J28-1)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E131JI	J28-1	Industrial	SY10E131JI	Sn-Pb
SY10E131JITR ⁽²⁾	J28-1	Industrial	SY10E131JI	Sn-Pb
SY100E131JI	J28-1	Industrial	SY100E131JI	Sn-Pb
SY100E131JITR ⁽²⁾	J28-1	Industrial	SY100E131JI	Sn-Pb
SY10E131JC	J28-1	Commercial	SY10E131JC	Sn-Pb
SY10E131JCTR ⁽²⁾	J28-1	Commercial	SY10E131JC	Sn-Pb
SY100E131JC	J28-1	Commercial	SY100E131JC	Sn-Pb
SY100E131JCTR ⁽²⁾	J28-1	Commercial	SY100E131JC	Sn-Pb
SY10E131JY ⁽³⁾	J28-1	Industrial	SY10E131JY with Pb-Free bar-line indicator	Matte-Sn
SY10E131JYTR ^(2, 3)	J28-1	Industrial	SY10E131JY with Pb-Free bar-line indicator	Matte-Sn
SY100E131JY ⁽³⁾	J28-1	Industrial	SY100E131JY with Pb-Free bar-line indicator	Matte-Sn
SY100E131JYTR ^(2, 3)	J28-1	Industrial	SY100E131JY with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.



Pin	State	Mode
Cc	L	Individual clocking with \overline{CEn}
\overline{CE}	L	Common clocking with Cc

VEE = VEE(Min.) to VEE(Max.); VCC = VCCO = GND

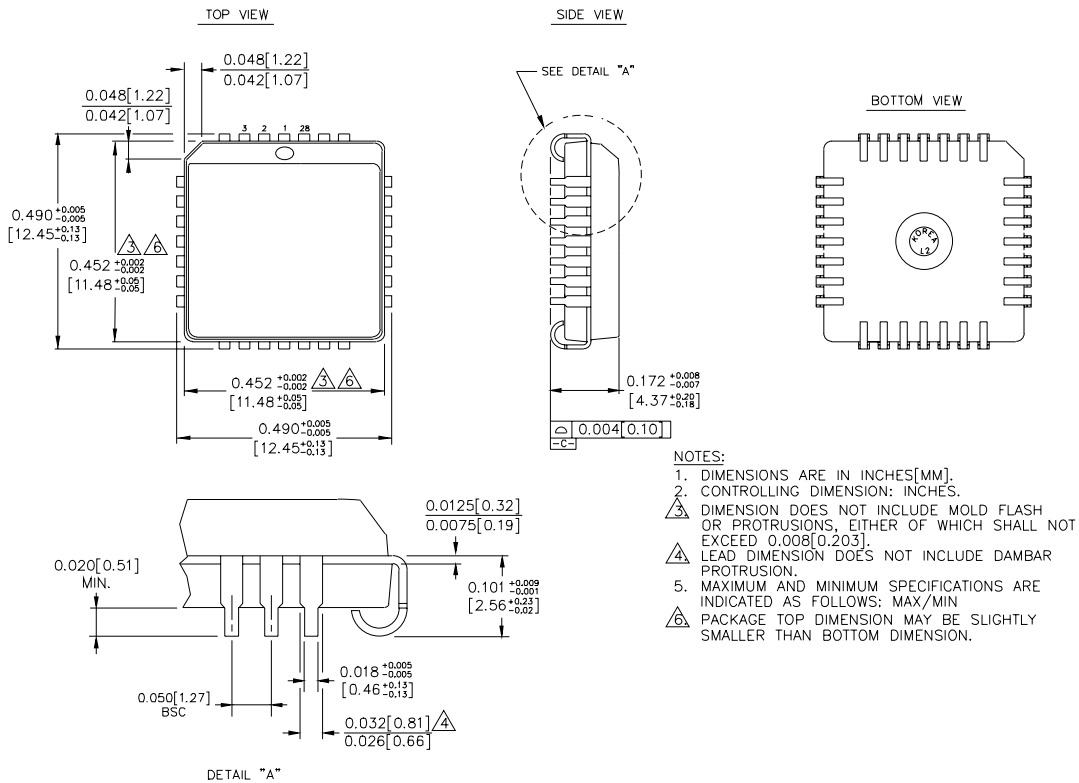
Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
IIH	Input HIGH Current													μA
	Cc	—	—	350	—	—	350	—	—	350	—	—	350	
	S	—	—	450	—	—	450	—	—	450	—	—	450	
	R	—	—	300	—	—	300	—	—	300	—	—	300	
	CE	—	—	300	—	—	300	—	—	300	—	—	300	
	D	—	—	150	—	—	150	—	—	150	—	—	150	
IEE	Power Supply Current													mA
	10E	—	58	70	—	58	70	—	58	70	—	58	70	
	100E	—	58	70	—	58	70	—	58	70	—	67	81	

VEE = VEE(Min.) to VEE(Max.); VCC = VCCO = GND

Symbol	Parameter	TA = -40°C			TA = 0°C			TA = +25°C			TA = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
fMAX	Max. Toggle Frequency	1100	1400	—	1100	1400	—	1100	1400	—	1100	1400	—	MHz
tPD	Propagation Delay to Output													ps
	CE	310	600	750	360	500	700	360	500	700	360	500	700	
	Cc	275	600	725	325	500	675	325	500	675	325	500	675	
	R	300	625	775	350	550	725	350	550	725	350	550	725	
	S	300	550	775	350	550	725	350	550	725	350	550	725	
ts	Set-up Time, D ⁽²⁾	200	20	—	150	20	—	150	20	—	150	20	—	ps
th	Hold Time, D ⁽²⁾	225	-20	—	175	-20	—	175	-20	—	175	-20	—	ps
tRR	Reset Recovery Time	450	150	—	400	150	—	400	150	—	400	150	—	ps
tPW	Minimum Pulse Width													ps
	Clk	400	—	—	400	—	—	400	—	—	400	—	—	
	R, S	400	—	—	400	—	—	400	—	—	400	—	—	
t _{skew}	Within-Device Skew ⁽¹⁾	—	60	—	—	60	—	—	60	—	—	60	—	ps
tr	Rise/Fall Time	275	460	725	300	480	675	300	480	675	300	480	675	ps
tf	20% to 80%													

Notes:

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Set-up/hold times guaranteed for both Cc and CE.



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