DIGITAL MULTI-PHASE BUCK CONTROLLER

FEATURES

- Intel VR11.x compliant Digital PWM Controller
- Programmable 1-phase to 8-phase operation
- Configurable switching frequency from 200 kHz to 1MHz per phase with accuracy better than 2%
- Customized Digital Over-Clocking Features
  - Easy-to-use SMBus Gamer command
  - Gamer VID control up to 2.3V, Gamer Vmax, VID Override or Track, Digital Load-Line Adjust, Gamer OC/OVP, Gamer OFF pin, Gamer OTP
- CHiL Efficiency Shaping Features
  - Variable Gate Drive
  - Dynamic Phase Control
- 1-phase to 4-phase PSI for Light Loads
- Adaptive Transient Algorithm minimizes output bulk capacitors
- Designed for use with coupled inductors
- Enables Thermal Phase Balancing
- SMBus Fault Indicators: OVP, UVP, OCP, OTP
- SMBus interface for configuring and monitoring; SMBus commands include monitoring input current and power
- Compatible with CHiL ATL Drivers and tri-state Drivers
- Nine bytes of NVM storage available for customer use
- +3.3V supply voltage; 0ºC to 85ºC Ambient operation
- RoHS Compliant, MSL level 1 package

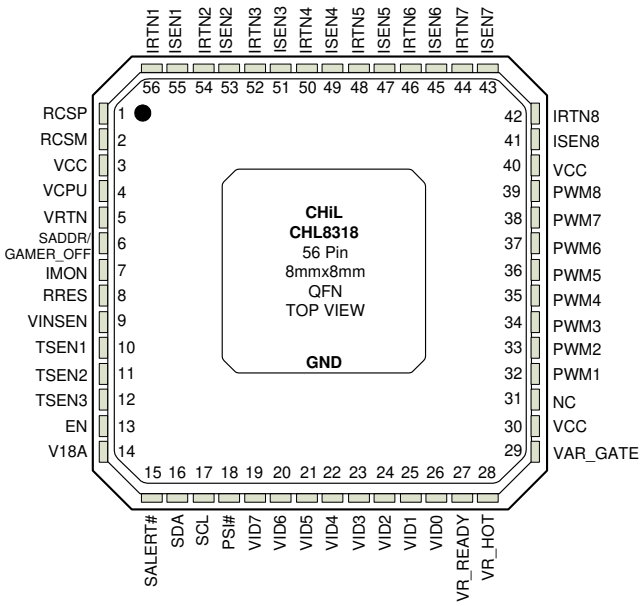

Figure 1. CHL8318 56 Pin QFN Package

DESCRIPTION

The CHL8318 is a 8-phase digital synchronous buck controller for core regulation of high-performance INTEL® VR11.1 and VR11.0 platforms. The CHL8318 is fully compliant with VR11.1 including Power Status Indicator (PSI) and for improved light load efficiency and accurate current output (IMON).

The CHiL CHL8318 includes a customized set of digital over-clocking features which require no external components. Gaming applications can use the SMBus interface to place the VRD into “Gamer Mode”. Gamer Mode features include Extended Gamer VID up to 2.3V with 6.25 mV resolution, Gamer Vmax, CPU VID Override or Track, Digital Load-Line adjust, Gamer OC/OVP and Gamer OFF pin.

The CHL8318 deploys a number of efficiency shaping features. The CHL8318 can be configured to optimize MOSFET gate drive versus load current, PSI can be programmed to be up to four phases for optimum light-load efficiency, and the controller can autonomously add/drop phases in low-current and mid-current regions to deliver 90+% efficiency across the entire load range.

CHiL’s unique Adaptive Transient Algorithm, based on non-linear digital PWM algorithms, minimizes output bulk capacitors. Coupled inductor mode of operation allows two phase PSI and add/drop of phases which are 180°out of phase for further improvement in transient response and form factor.

CHL8318 supports three NTC temperature sensors to report temperature and trigger VR HOT and OTP faults. Digital thermal balancing allows proportional current imbalance between phases.

The CHL8318 provides extensive OVP, UVP, OCP and OTP fault protection. Device and fault configuration parameters are easily defined using the CHiL Intuitive Power Designer (IPD) GUI and stored in on-chip non-volatile memory (NVM).

The 3-pin SMBus interface can be used to monitor a variety of operating parameters on up to seven CHL8318 based VRs. The controller includes a unique sensorless and lossless input current monitoring capability.

The CHL8318 truly simplifies VRD design and enables fastest time-to-market with its “set-and-forget” methodology.

APPLICATIONS

- Intel® VR11.x CPU VRD and VRM; DDR Memory
- High Performance Desktops and Servers
- Over-clocking and High-Efficiency Applications

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FUNCTIONAL BLOCK DIAGRAM

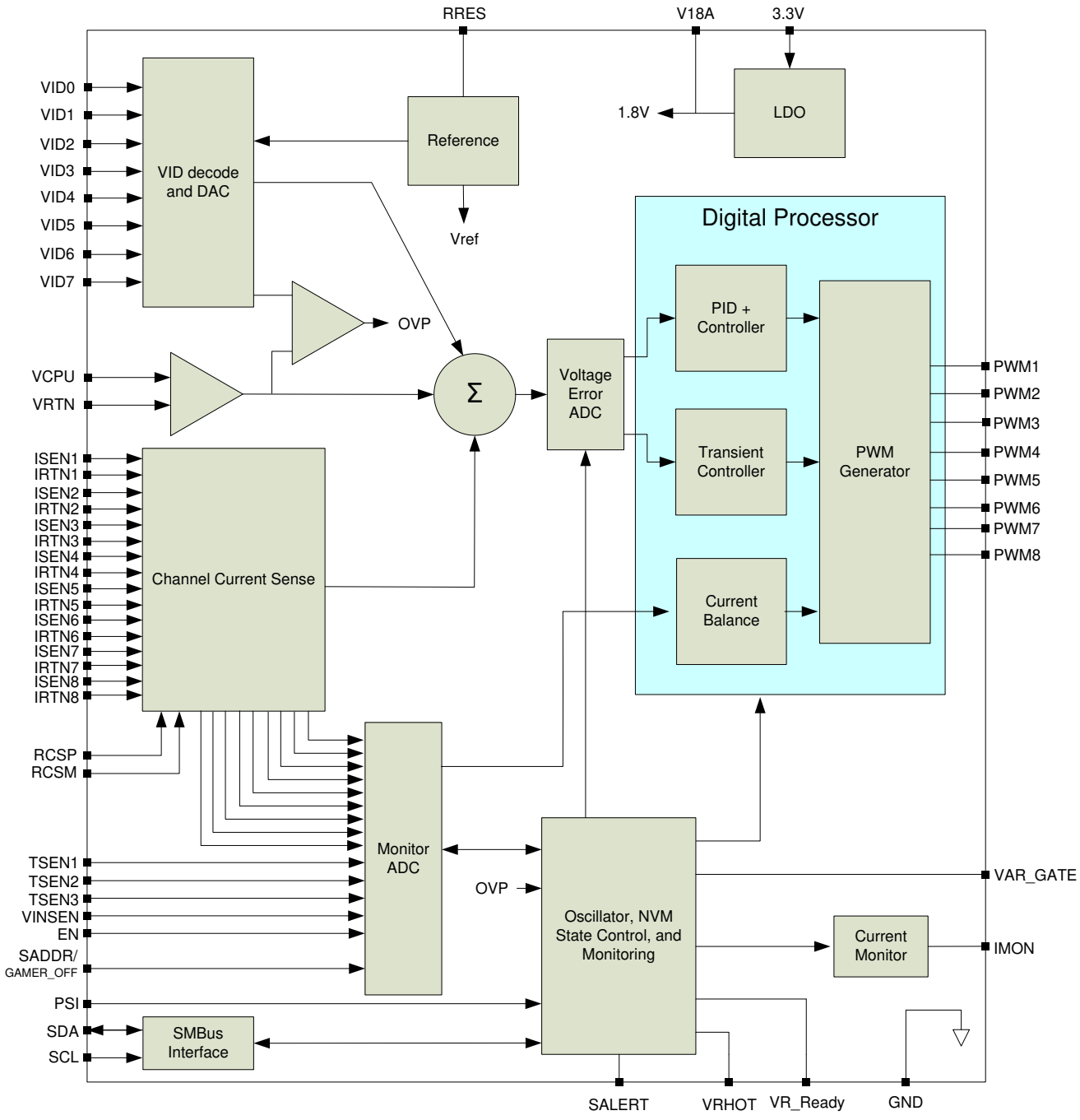


Figure 2. Functional Block Diagram

TYPICAL APPLICATIONS

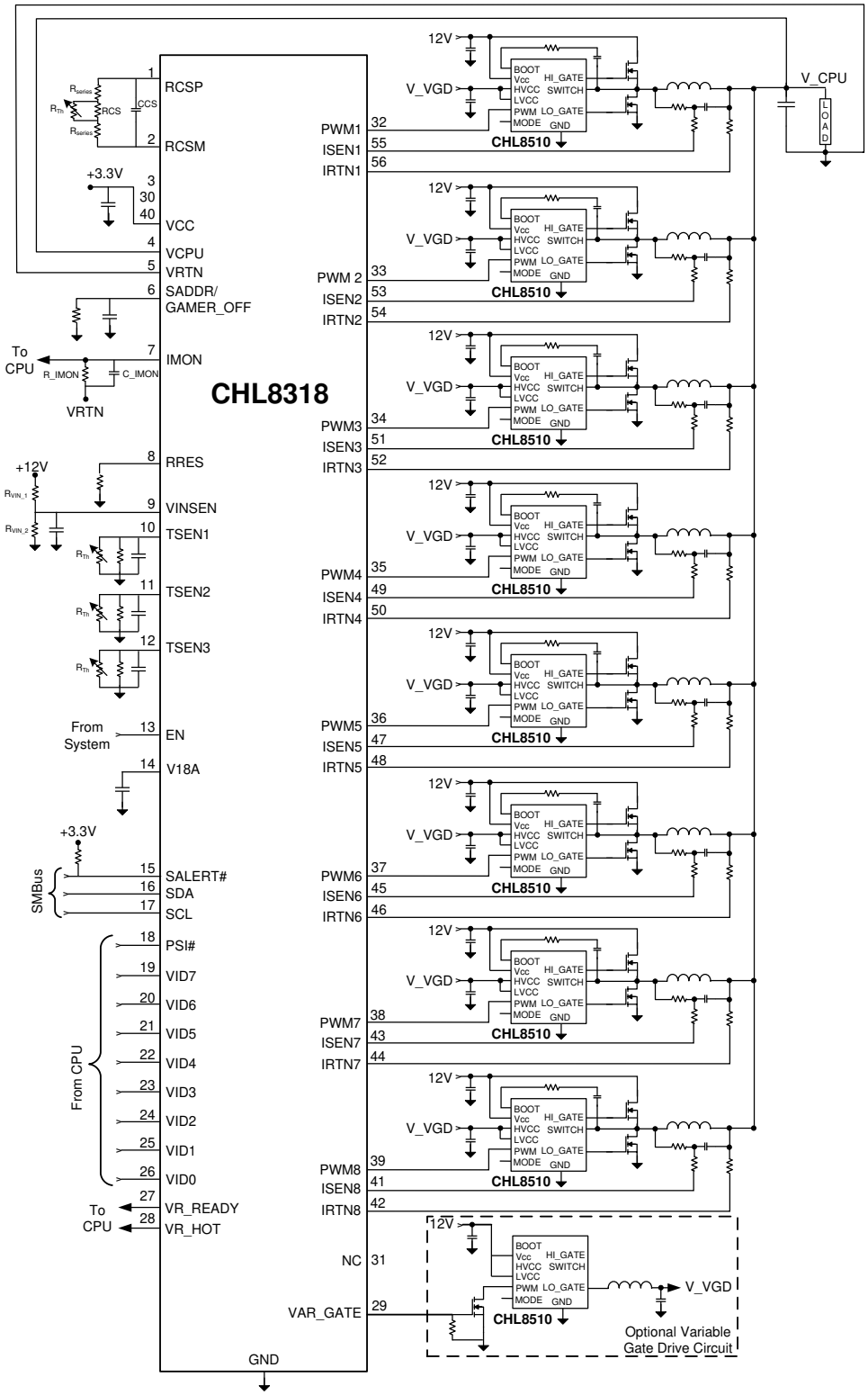


Figure 3. 8-phase VRD using CHL8318 Controller and CHL8510 MOSFET drivers

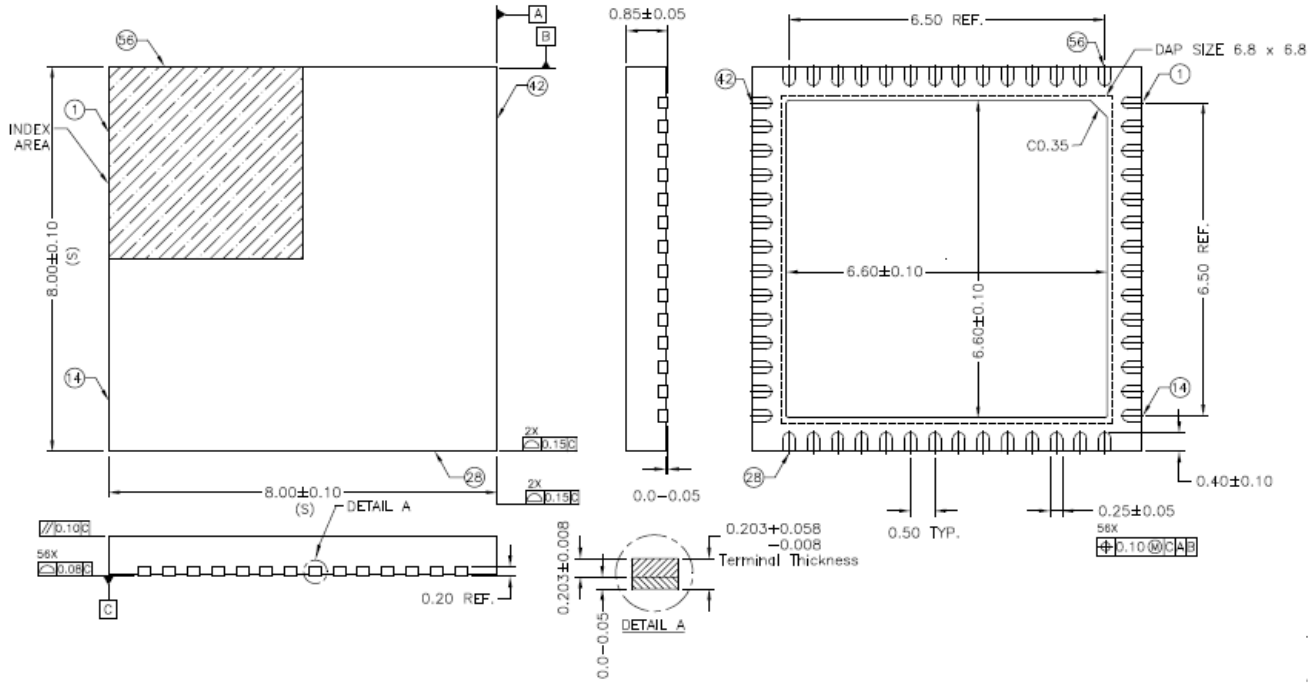
ORDERING INFORMATION

CHL8318 □ □ □

- T: Tape & Reel
- Package type
  R : QFN
- Operating Temperature Range
  C: Commercial Standard

Package	Tape & Reel Qty	Part Number
QFN	3000	CHL8318CRT

PACKAGE INFORMATION



1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. REFER JEDEC MO-220.