

LCD Module Technical Specification

First Edition
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Final Revision

Type No. **T-55149GD030J-MLW-AJN**

Customer : **OPTREX STANDARD**

Customer's Product No : -----

OPTREX CORPORATION

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APPROVED

By _____

Signature :

Date :

Please return this specification within two month with your signature.
If not returned within two month, specification will be
considered as having been accepted.

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Revision History

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1.Application

This specification applies to 3.0"color TFT-LCD module (T-55149GD030J-MLW-AJN).

2.General Specifications

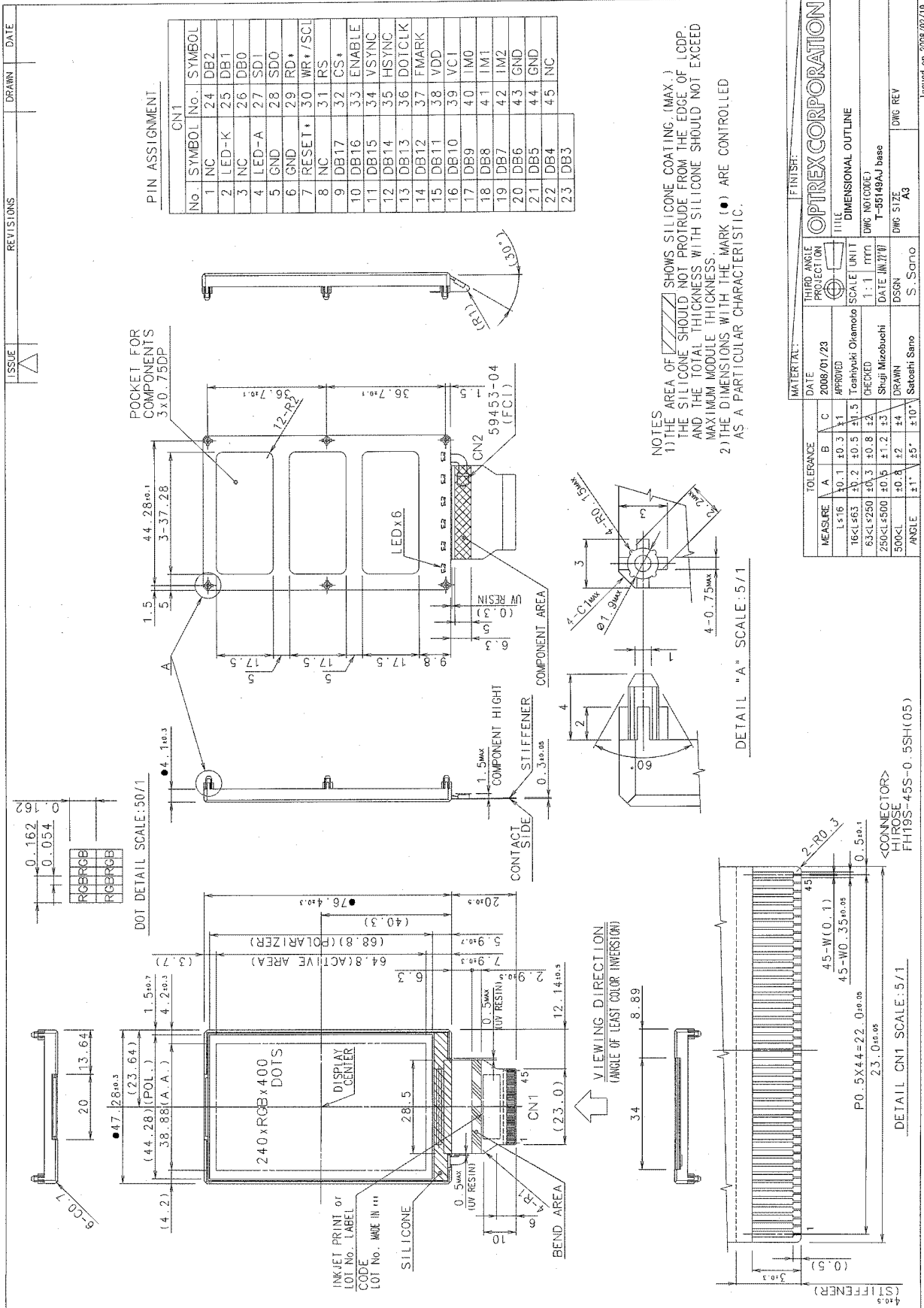
Dot Pixels	:	240×3 [R.G.B] (W) × 400 (H) dots
Dot Size	:	0.054 (W) × 0.162 (H) mm
Pixel Arrangement	:	RGB-Stripe
Color Depth	:	262144 color
Viewing Area	:	38.88 (W) × 64.8 (H) mm
Outline Dimensions*	:	47.28 (W) × 76.4* (H) × 4.4max.** (D) mm
		* Without FPC
		**Without Hook
Weight	:	24.3g max.
LCD Type	:	ASS-25521 (TFT / Normally white-mode / Transflective)
Viewing Direction	:	6:00
TFT Driver	:	Controler driver R61509(RENESAS)
Data Transfer	:	18 / 16 / 9 / 8-bit 80 system, Serial 18 / 16 / 6 RGB I/F
Back-light	:	LED Back-light / White
RoHS regulation	:	To our best knowledge, this product satisfies material requirement of RoHS regulation. Our company is doing the best efforts to obtain the equivalent certificate from our suppliers.

3.Operating Conditions

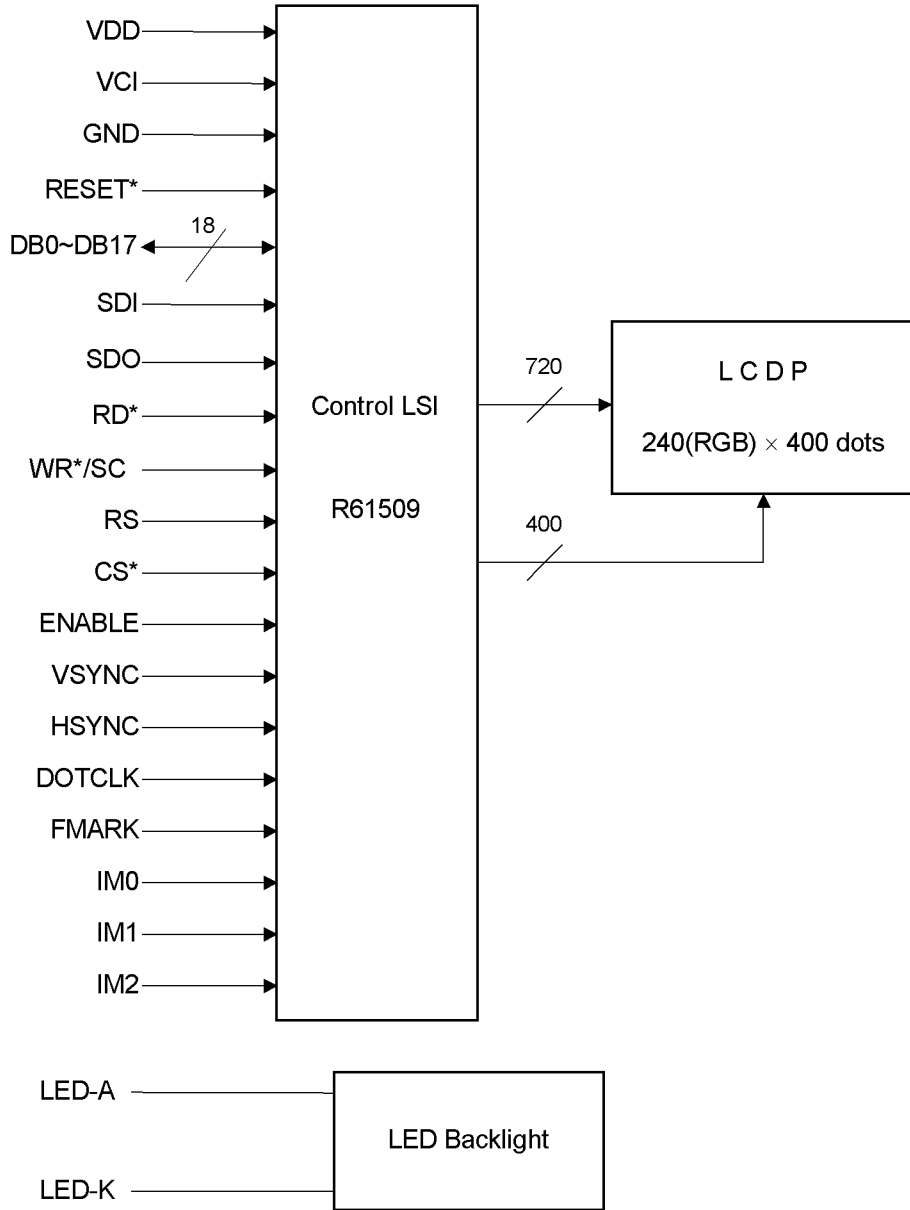
Item	Conditions	Temperature Range	Remark
Operating Temperature Range	PNL Surface	-20~70°C	Note1
Storage Temperature Range	PNL Surface	-30~80°C	

Note1: Operating temperature range defines the operation only and the contrast, response time and other display optical characteristics are set at Ta=+25°C.

4. Dimensional Outline



5. Block Diagram



6. I/O Terminal

6.1. CN1 Pin Assignment

Corresponding Connector: HIROSE: FH19S-45S-0.5SH (05)

No.	Symbol	Functional Description
1	NC	Non Connection
2	LED-K	LED Cathode
3	NC	Non Connection
4	LED-A	LED Anode
5	GND	GND
6	GND	GND
7	RESET*	Reset Signal Input L:Active
8	NC	Non Connection
9	DB17	<p>18-bit parallel bi-directional data bus for 80-system interface (Amplitude : IOVCC1-GND)</p> <p>8 bit I/F : DB17-DB10 are used. 9 bit I/F : DB17-DB9 are used. 16 bit I/F : DB17-DB10 and DB8-1 are used. 18 bit I/F : DB17-DB0 are used.</p> <p>18-bit parallel bi-directional data bus for RGB interface operation (Amplitude : IOVCC1-GND)</p> <p>6 bit I/F : DB17-DB12 are used. 16 bit I/F : DB17-DB13 and DB11-1 are used. 18 bit I/F : DB17-DB0 are used.</p>
10	DB16	
11	DB15	
12	DB14	
13	DB13	
14	DB12	
15	DB11	
16	DB10	
17	DB9	
18	DB8	
19	DB7	
20	DB6	
21	DB5	
22	DB4	
23	DB3	
24	DB2	
25	DB1	
26	DB0	
27	SDI	Input for Serial Data
28	SDO	Output for Serial Data
29	RD*	Read Control Input L:Active
30	WR*/SCL	Write Control Input L:Active / Input for Serial Clock
31	RS	Reister Select Input
32	CS*	Chip Select Input L:Active
33	ENABLE	Data enable signal for RGB interface
34	VSYNC	Vertical sync signal for RGB interface
35	HSYNC	Horizontal sync signal for RGB interface

36	DOTCLK	Clock signal for sampling catch data signal					
37	FMARK	First Line Marker(Indicates Start of Frame)					
38	VDD	Power Supply to the Intrinsic Pins					
39	VCI	Power Supply to the LCD and Internal Logic					
40	IM0	Select a mode to Interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.					
41	IM1						
42	IM2	IM2	IM1	IM0	Interface Mode	DB Pin	Colors
		0	0	0	80-system 18-bit interface	DB17-0	262,144
		0	0	1	80-system 9-bit interface	DB17-9	262,144
		0	1	0	80-system 16-bit interface	DB17-10 DB8-1	262,144
		0	1	1	80-system 8-bit interface	DB17-10	262,144
		1	0	(*ID)	Clock synchronous serial interface	-	65,536
		1	1	0	Setting Disabled	-	-
		1	1	1	Setting Disabled	-	-
43	GND	GND					
44	GND	GND					
45	NC	Non Connection					

7. Electrical Specifications

7.1. Absolute Maximum Ratings

Ta=-20~70°C, GND=0V

Parameter	Symbol	Conditions	Min.	Max.	Units
Supply Voltage	VDD	-	-0.3	4.6	V
Supply for step-up Voltage	VCI	-	-0.3	4.6	V
Input Voltage	V _{IN}	-	-0.3	VDD+0.3	V

7.2. DC Characteristics

Ta=-20~70°C, VSS=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	VDD	-	1.7	1.8	1.9	V
Supply for step-up Voltage	VCI	-	2.6	2.8	3.0	V
High Level Input Voltage	V _{IH}	-	0.8VDD	-	VDD	V
Low Level Input Voltage	V _{IL}	-	GND	-	0.2VDD	V
High Level Output Voltage	V _{OH}	I _{OH} =2.0mA	VDD-0.5	-	VDD	V
Low Level Output Voltage	V _{OL}	I _{OL} =2.0mA	GND	-	0.5	V
Supply Current	IDD	Still picture VDD - GND = 1.8V without back-light (Note 1) I _{OL} =2.0mA	-	2.1	5.0	μA
Supply Current	ICI	Still picture VCI - GND = 2.8V without back-light (Note 1)	-	10.5	15.8	mA
VCOM High Level	V _{COMH}	Still picture VCI - GND = 2.8V	-	(3.1)	-	V
VCOM Low Level	V _{COML}	Still picture VCI - GND = 2.8V	-	(-0.8)	-	V

Note1: The driving conditions are to be described.

Note2: Please keep VCI VDD

: DB17~DB0, RESET, RD, WR/SCL, RS, CS, ENABLE, VSYNC, HSYNC, DOTCLK, FMARK

7.3.AC Characteristics

7.3.1. 80-system Bus Interface Timing Characteristics

(1) 16 or 18bit Inetrface (Normal write mode: R003h; IB9=0)

Condition: Ta=-20~70°C, VDD=1.7V~1.9V

Parameter		Symbol	Min.	Typ.	Max.	Units
Bus cycle Time	Write	t_{CYCW}	110	-	-	ns
	Read	t_{CYCR}	450	-	-	ns
Write low-level pulse width		PW_{LW}	30	-	-	ns
Read low-level pulse width		PW_{LR}	170	-	-	ns
Write High-level pulse width		PW_{HW}	30	-	-	ns
Read High-level pulse width		PW_{HR}	250	-	-	ns
Write Read Rise/Fall Time		t_{WRR}, t_{WRF}	-	-	10	ns
SetupTime	Write (RS to CS*,WR*)	t_{AS}	0	-	-	ns
	Read (RS to CS*,RD*)		10	-	-	
Address hold Time		t_{AH}	2	-	-	ns
Write Data Setup Time		t_{DSW}	20	-	-	ns
Write Data Hold Time		t_{HWR}	10	-	-	ns
Read Data Delay Time		t_{DDR}	-	-	150	ns
Read Data Hold Time		t_{DHR}	5	-	-	ns

(2) 16 or 18bit Inetrface (High speed write mode: R003h; IB9=1)

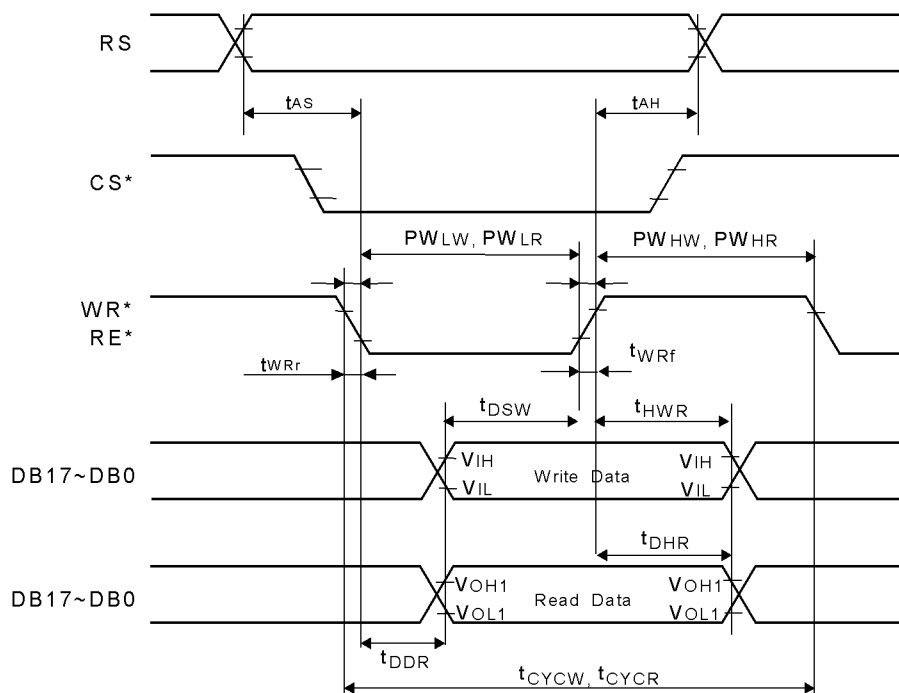
Condition: Ta=-20~70°C, VDD=1.7V~1.9V

Parameter		Symbol	Min.	Typ.	Max.	Units
Bus cycle Time	Write	t_{CYCW}	65	-	-	ns
	Read	t_{CYCR}	450	-	-	ns
Write low-level pulse width		PW_{LW}	30	-	-	ns
Read low-level pulse width		PW_{LR}	170	-	-	ns
Write High-level pulse width		PW_{HW}	20	-	-	ns
Read High-level pulse width		PW_{HR}	250	-	-	ns
Write Read Rise/Fall Time		t_{WRR}, t_{WRF}	-	-	10	ns
SetupTime	Write (RS to CS*,WR*)	t_{AS}	0	-	-	ns
	Read (RS to CS*,RD*)		10	-	-	
Address hold Time		t_{AH}	2	-	-	ns
Write Data Setup Time		t_{DSW}	20	-	-	ns
Write Data Hold Time		t_{HWR}	10	-	-	ns
Read Data Delay Time		t_{DDR}	-	-	150	ns
Read Data Hold Time		t_{DHR}	5	-	-	ns

(3) 8 or 9bit Inetrface (Normal / High speed write mode: R003h; IB9=0/1)

Condition: Ta=-20~70°C, VDD=1.7V~1.9V

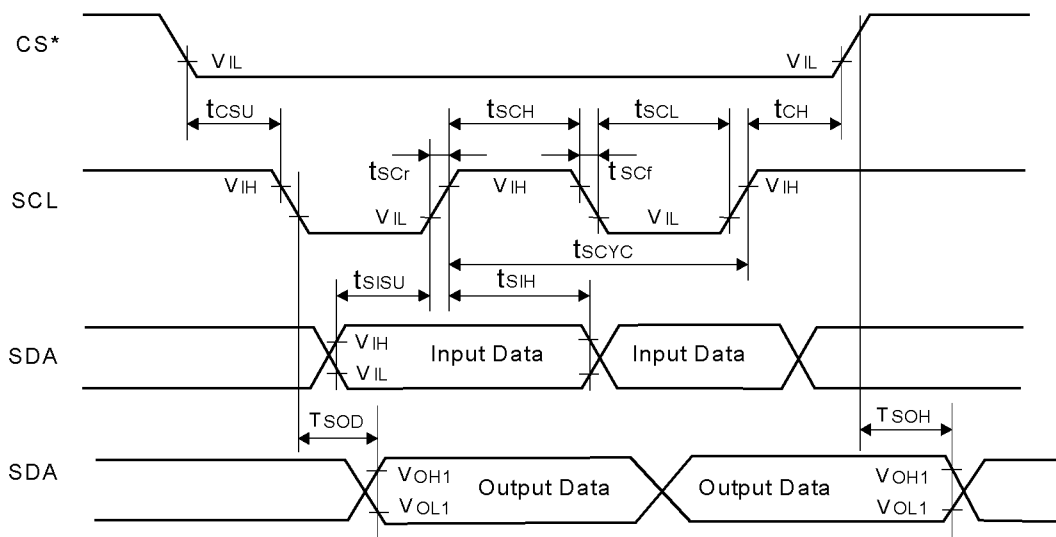
Parameter		Symbol	Min.	Typ.	Max.	Units
Bus cycle Time	Write	t_{CYCW}	60	-	-	ns
	Read	t_{CYCR}	450	-	-	ns
Write low-level pulse width		PW_{LW}	30	-	-	ns
Read low-level pulse width		PW_{LR}	170	-	-	ns
Write High-level pulse width		PW_{HW}	20	-	-	ns
Read High-level pulse width		PW_{HR}	250	-	-	ns
Write Read Rise/Fall Time		t_{WRr}, t_{WRf}	-	-	10	ns
SetupTime	Write (RS to CS*,WR*)	t_{AS}	0	-	-	ns
	Read (RS to CS*,RD*)		10	-	-	
Address hold Time		t_{AH}	2	-	-	ns
Write Data Setup Time		t_{DSW}	20	-	-	ns
Write Data Hold Time		t_{HWR}	10	-	-	ns
Read Data Delay Time		t_{DDR}	-	-	150	ns
Read Data Hold Time		t_{DHR}	5	-	-	ns



7.3.2.Clock-synchronized Serial Interface Timing Characteristics

Condition: Ta=-20~70°C, VDD=1.7V~1.9V

Parameter	Symbol	Min.	Typ.	Max.	Units
Serial Clock Cycle time (Write)	t_{SCYC}	100	-	20000	ns
Serial Clock Cycle time (Read)	t_{SCYC}	350	-	20000	ns
Serial Clock (High Level Width) (Write)	t_{SCH}	40	-	-	ns
Serial Clock (High Level Width) (Read)	t_{SCH}	150	-	-	ns
Serial Clock (Low Level Width) (Write)	t_{SCL}	40	-	-	ns
Serial Clock (Low Level Width) (Read)	t_{SCL}	150	-	-	ns
Serial Clock Rise/Fall Time	t_{SCr}, t_{SCf}	-	-	20	ns
Chip Select Set-up Time	t_{CSU}	20	-	-	ns
Chip Select Hold Time	t_{CH}	60	-	-	ns
Serial Input Data Set-up Time	t_{SISU}	30	-	-	ns
Serial Input Data Hold Time	t_{SIH}	30	-	-	ns
Serial Output Data Delay Time	t_{SOD}	-	-	130	ns
Serial Output Data Hold Time	t_{SOH}	5	-	-	ns



7.3.3.RGB Interface

(1) 16 or 18bit RGB Inetrface (High speed write mode: R003h; IB9=1)

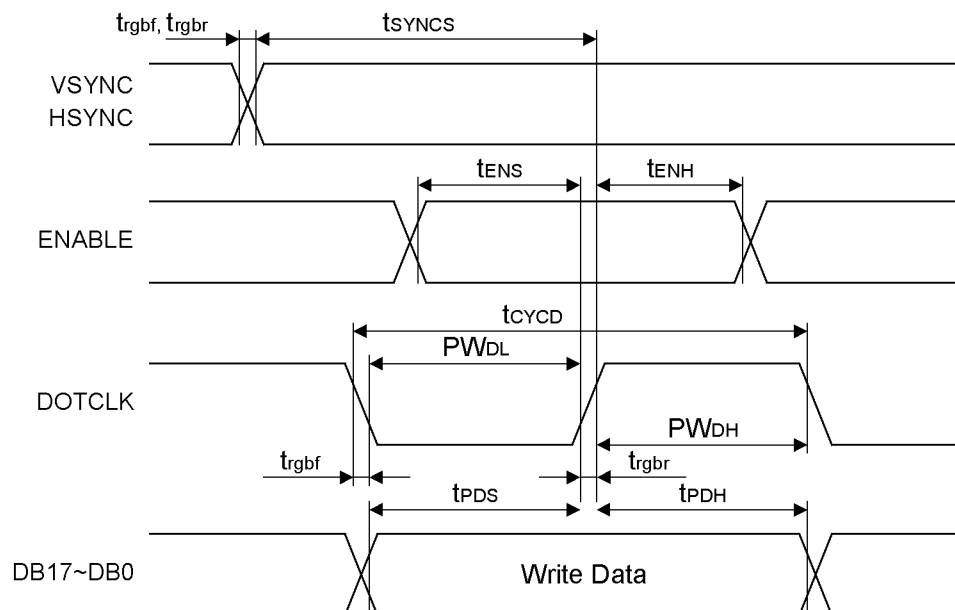
$T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 1.7\text{V} \sim 1.9\text{V}$

Parameter	Symbol	Min.	Typ.	Max.	Units
VSYNC/HSYNC Setup Time	t_{SYNCS}	0	-	1	clock
Enable Setup Time	t_{ENS}	10	-	-	ns
Enable Hold Time	t_{ENH}	20	-	-	ns
DOTCLK Low-level pulse width	PW_{DL}	40	-	-	ns
DOTCLK High-level pulse width	PW_{DH}	40	-	-	ns
DOTCLK Cycle Time	t_{CYCD}	100	-	-	ns
Data Setup Time	t_{PDS}	10	-	-	ns
Data Hold Time	t_{PDH}	40	-	-	ns
DOTCLK, VSYNC, HSYNC Rise/Fall Time	t_{rgr}, t_{rgbr}	-	-	25	ns

(2) 6bit RGB Inetrface (High speed write mode: R003h; IB9=1)

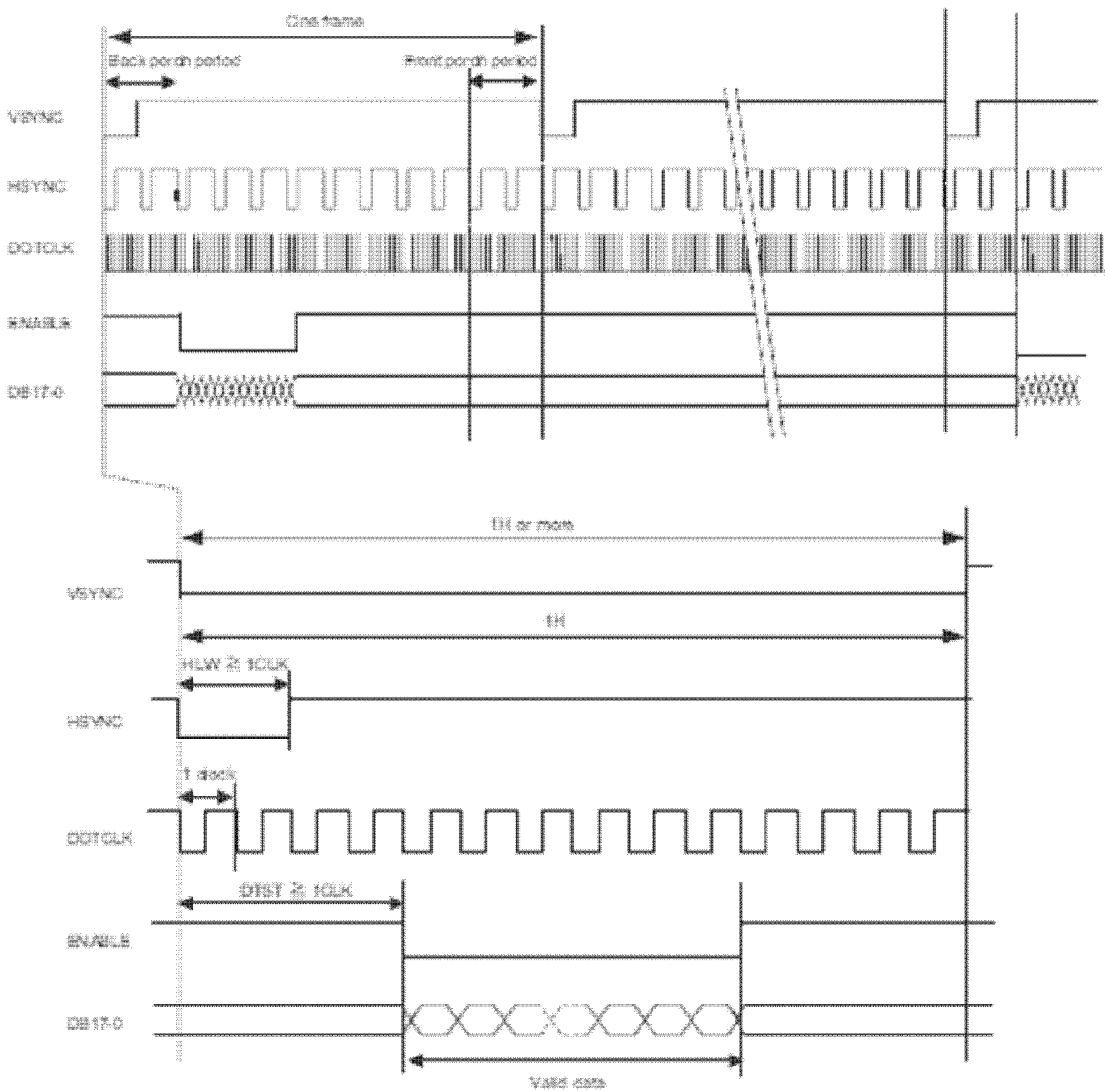
$T_a = -20 \sim 70^\circ\text{C}$, $V_{DD} = 1.7\text{V} \sim 1.9\text{V}$

Parameter	Symbol	Min.	Typ.	Max.	Units
VSYNC/HSYNC Setup Time	t_{SYNCS}	0	-	1	clock
Enable Setup Time	t_{ENS}	10	-	-	ns
Enable Hold Time	t_{ENH}	25	-	-	ns
DOTCLK Low-level pulse width	PW_{DL}	25	-	-	ns
DOTCLK High-level pulse width	PW_{DH}	25	-	-	ns
DOTCLK Cycle Time	t_{CYCD}	60	-	-	ns
Data Setup Time	t_{PDS}	10	-	-	ns
Data Hold Time	t_{PDH}	25	-	-	ns
DOTCLK, VSYNC, HSYNC Rise/Fall Time	t_{rgr}, t_{rgbr}	-	-	25	ns

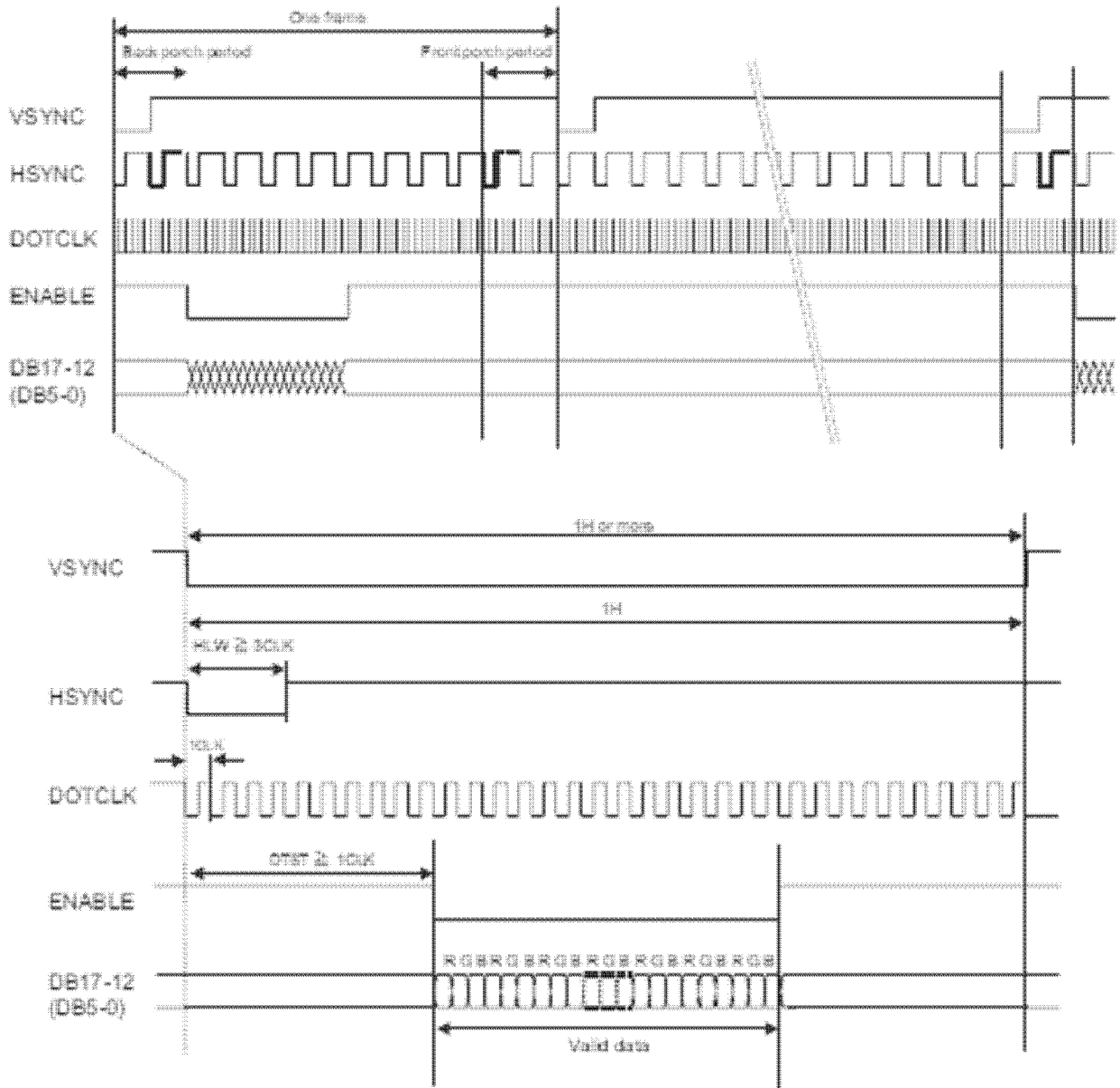


7.3.4.RGB Interface Timing

(1) 16 or 18bit RGB Interface Timing



(2) 6bit RGB Interface Timing



7.3.5.Reset Timing Characteristics

Ta=-20~70°C, VDD=1.7V~1.9V

Parameter	Symbol	Min.	Max.	Units
Reset "L" Pulse Width	t _{RES}	1	-	ms
Reset Rise Time	tr _{RES}	-	10	μs

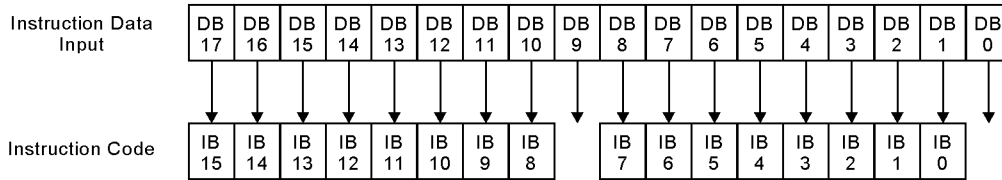


7.4.Data Format

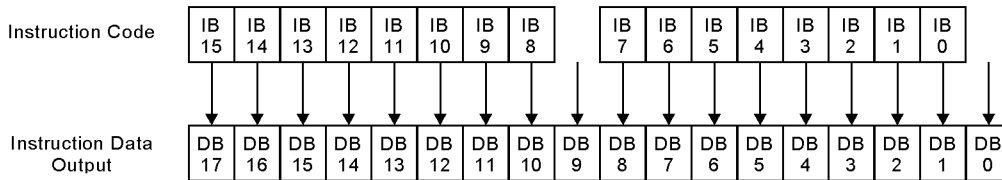
7.4.1.80-system Interface Data Format

(1) 18Bit Interface (IM2=0, IM1=0, IM0=0)

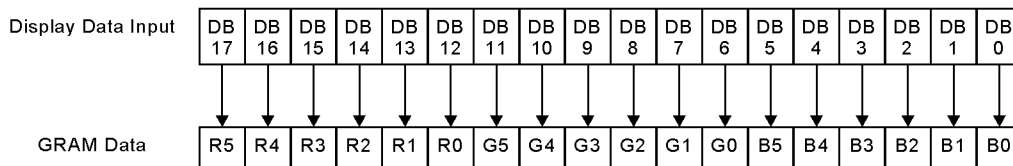
◆ Instruction Write



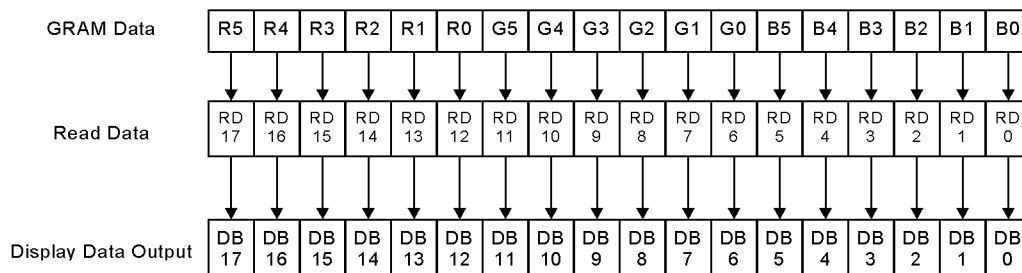
◆ Device Code Read



◆ RAM Data Write

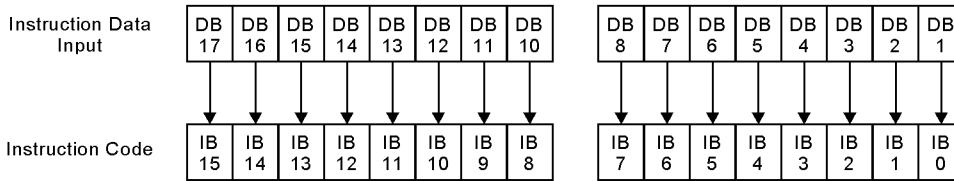


◆ RAM Data Read

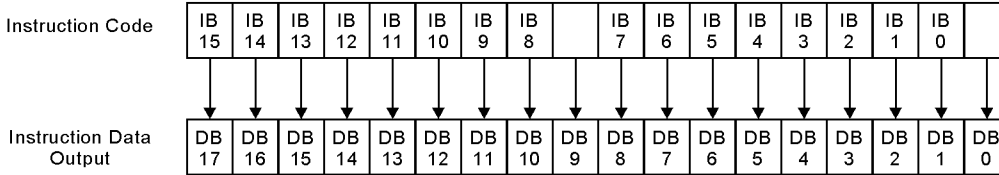


(2) 16Bit Interface (IM2=0, IM1=1, IM0=0)

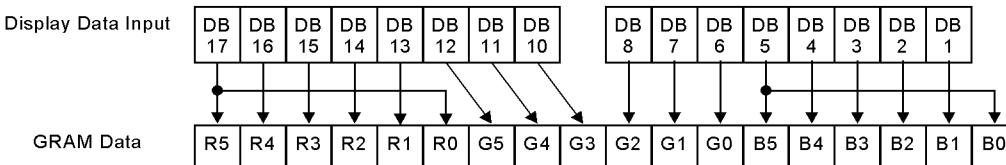
◆ Instruction Write



◆ Device Code Read

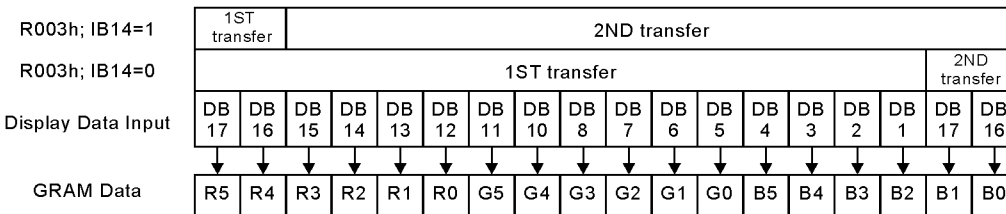


◆ RAM Data Write (1 time data transfer Mode: R003h; IB15=0) 65,536 colors

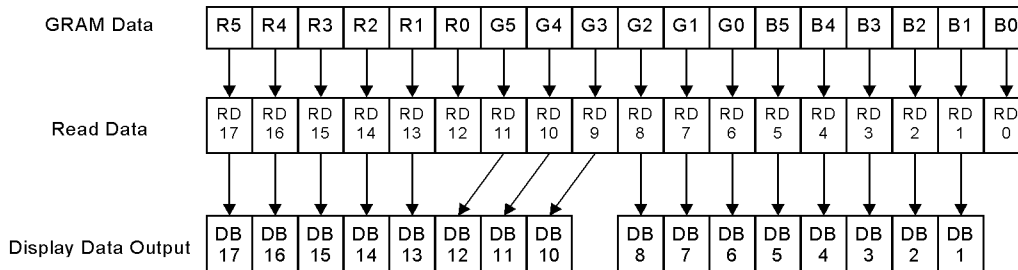


◆ RAM Data Write (2 times data transfer Mode: R003h; IB15=0) 262,144 colors

Note: Please refer to (5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation



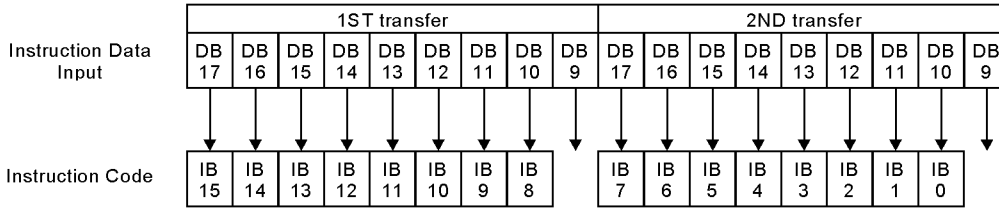
◆ RAM Data Read (1 time data transfer Mode: R003h; IB15=0) 65,536 colors



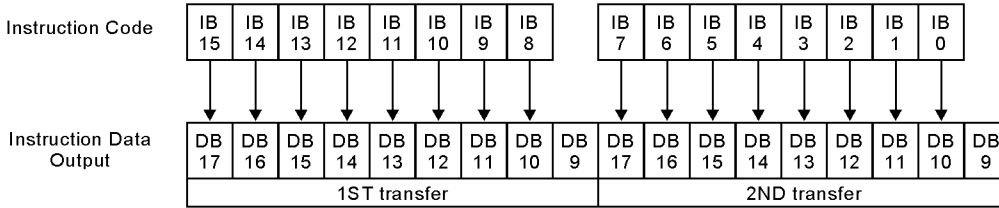
RAM Data Read in 2 times transfer mode cannot be performed.

(3) 9Bit Interface (IM2=0, IM1=0, IM0=1)

◆ Instruction Write

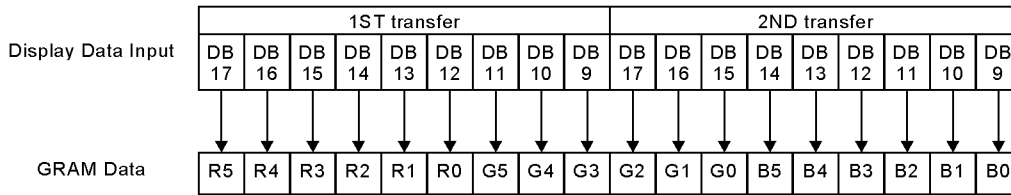


◆ Device Code Read

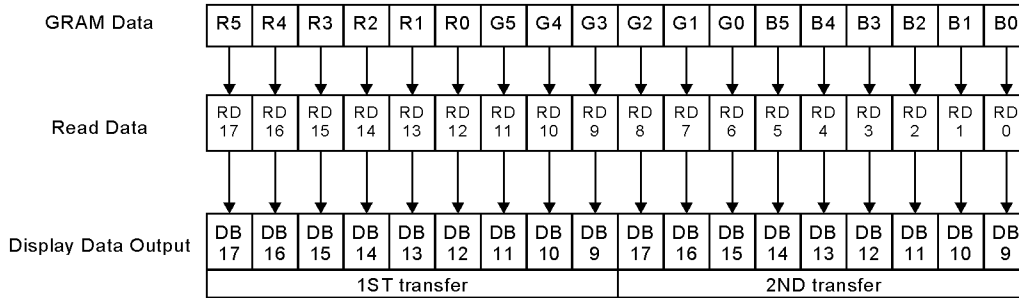


◆ RAM Data Write

Note: Please refer to (5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation

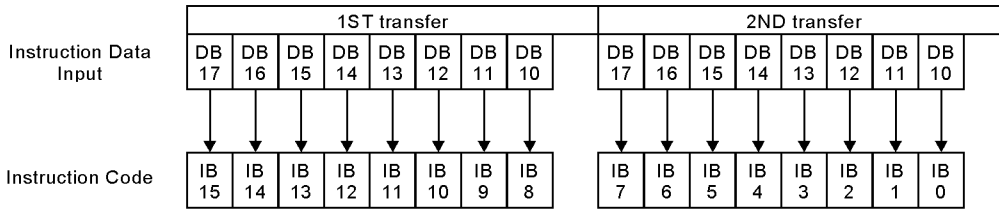


◆ RAM Data Read

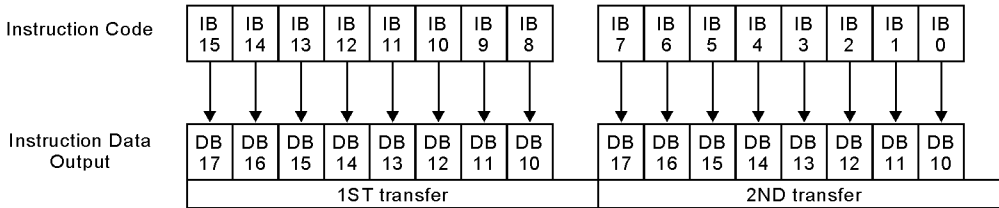


(4) 8Bit Interface (IM2=0, IM1=1, IM0=1)

◆ Instruction Write

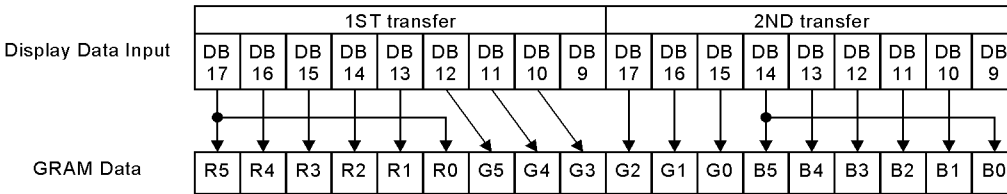


◆ Device Code Read



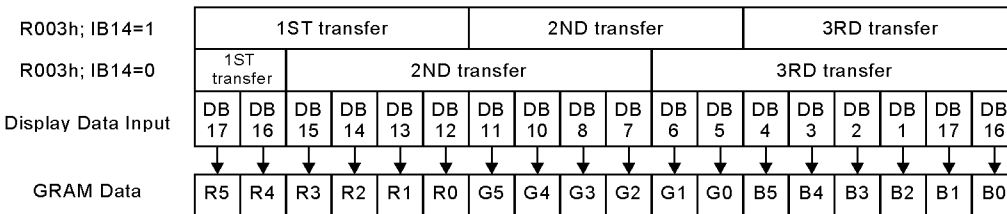
◆ RAM Data Write (2 times data transfer Mode:R003h; IB15=0) 65,536 colors

Note: Please refer to (5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation

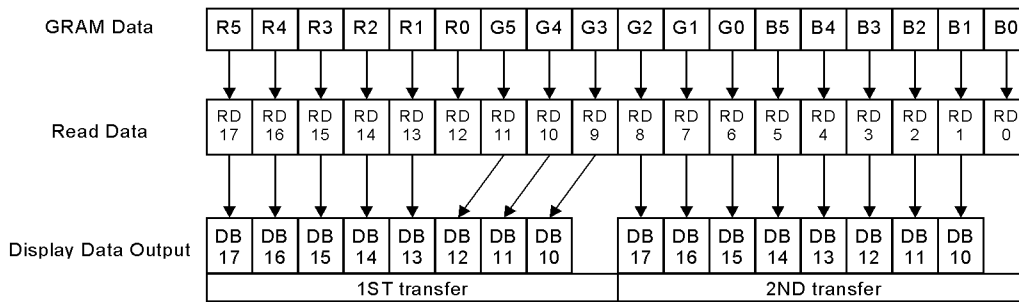


◆ RAM Data Write (3 times data transfer Mode:R003h; IB15=1) 262,144 colors

Note: Please refer to (5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation



◆ RAM Data Read



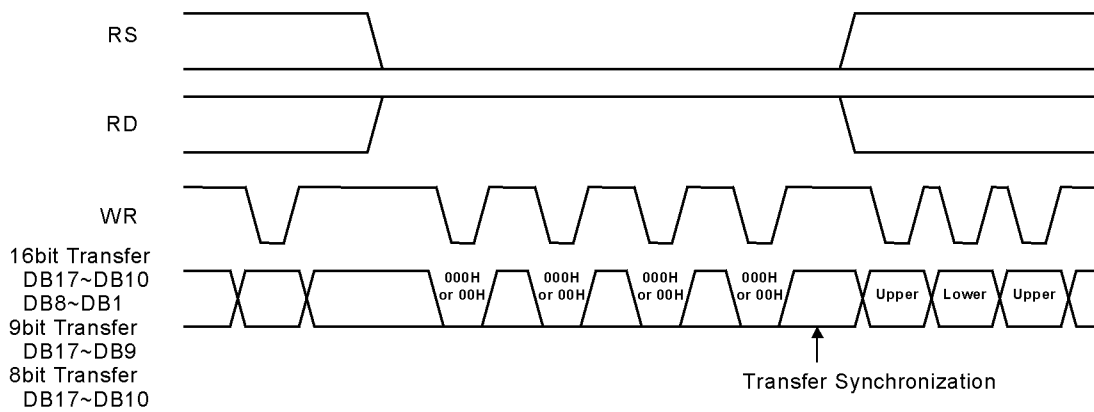
RAM Data Read in 3 times transfer mode cannot be performed.

(5) Data Transfer Synchronization in 16, 9, 8-Bit Bus Interface Operation

When a mismatch occurs in upper and lower data transfers due to noise and so on, the 000H (or 00H) instruction is written four times consecutively to reset the upper and lower counters in order to restart the data transfer from upper bits.

The data transfer synchronization, when executed periodically, can help the display system recover from runaway.

Make sure to execute data transfer synchronization after reset operation before transferring instruction.



7.4.2. Clock-synchronized Serial Interface (IM2=1, IM1=0, IM0=ID)

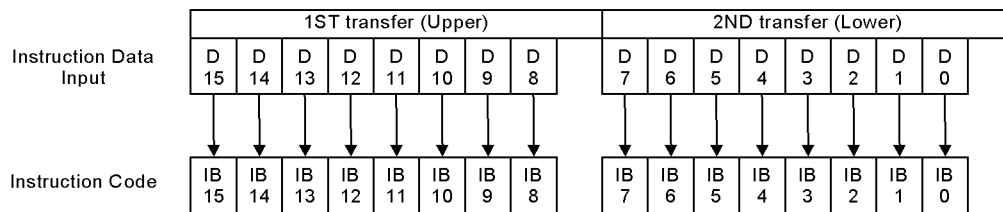
◆ Start Byte Format

Bit	1	2	3	4	5	6	7	8
Start Byte Format	0	1	1	1	0	ID	RS	R/W
IM=0	0	1	1	1	0	0	RS	R/W
IM=1	0	1	1	1	0	1	RS	R/W

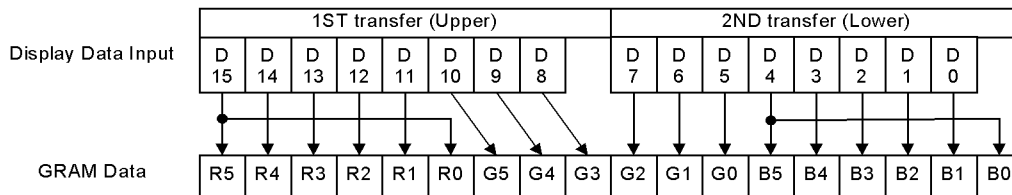
◆ Function of RS, R/W

RS	R/W	Function
0	0	Setting of Instruction Code
0	1	Prohibition
1	0	Write Instruction data
1	1	Read Instruction data

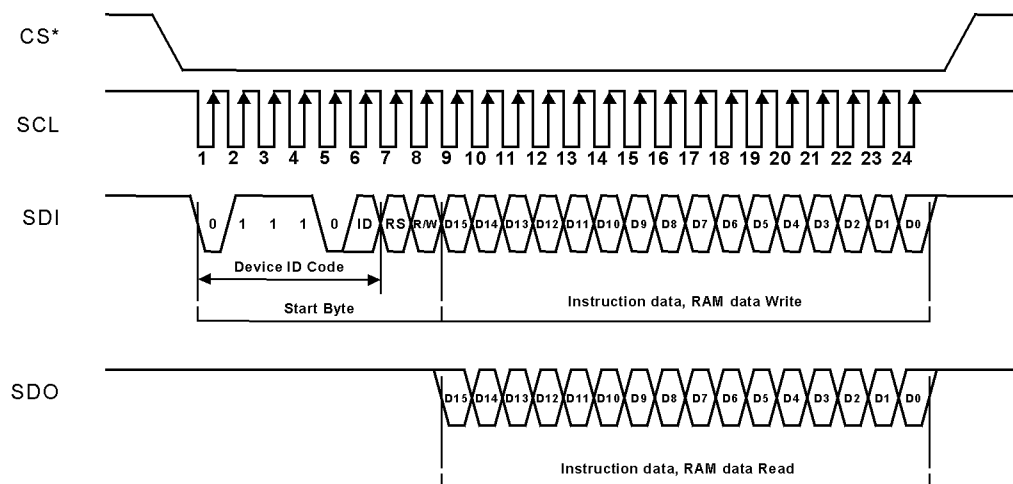
◆ Instruction Write



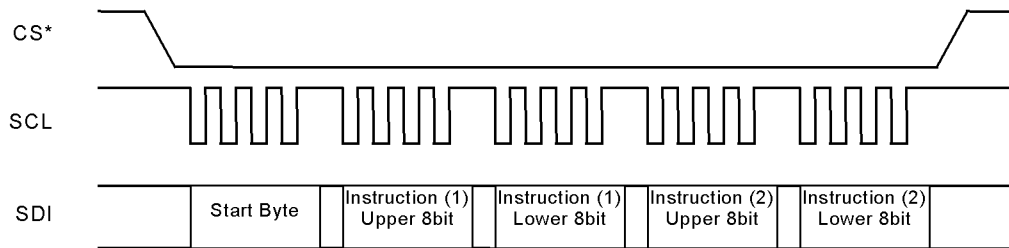
◆ RAM Data Write 65,536 colors



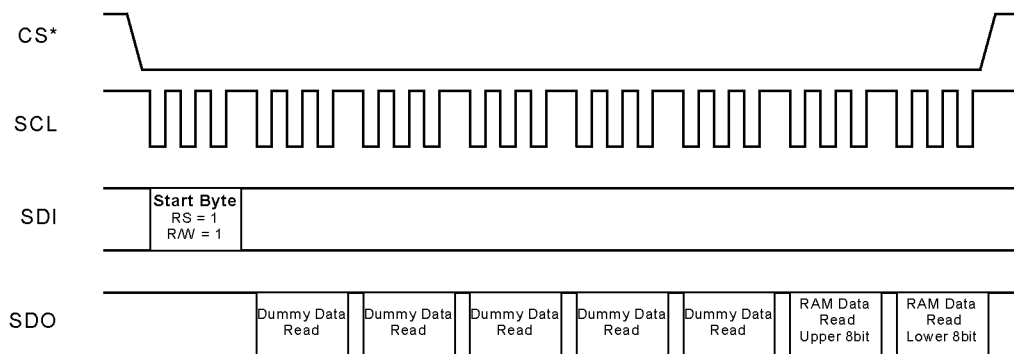
◆ Transfer of Clock-synchronized Serial Interface



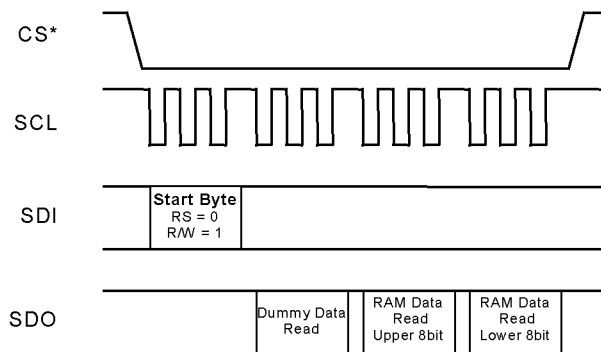
◆ **Transfer of Continuous Data**



◆ **RAM Data Read**



◆ **Instruction Data Read**



7.5. Power ON / OFF Sequence

7.5.1. Relationship of Instruction Code and Hexadecimal Number

Instruction Code	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	
Example (Binary)	0	0	0	1	1	0	1	1	1	0	0	0	1	1	1	0	Bin
Example (Hexadecimal)	1				B				8				E				Hex

7.5.2.Command List for Power ON (Recommended Setting)

Setting Item	Index (Value)	Value(2byte Setting)	Remark
Power ON			
Power ON	Input VDD=1.80V VDD2=2.80V		
Reset			
Reset	RESET Pulse "L"		Reset
Wait	10msec		
Release Reset	RESET Pulse "H"		Release Reset
Wait	10msec		
Application Setup			
Device Cord Read (/RD)	0000 h	1509 h	Access check
Base Image Number of Line	0400 h	3100 h	NL0=400Lines, SCN=0
Driver Output	0001 h	0100 h	S720→S1
LCD Driving Wave Control	0002 h	0100 h	C Pattern Waveform
Entry Mode	0003 h	1230 h	BGR=1, HMW=1, I/D=11
Display Control 2	0008 h	0808 h	FP=BP=8Lines
Low Power Control 2	000b h	0010 h	VEM=1, 262,144color
External Display Interface Control 2	000F h	0000 h	DOTCLK ↓ , ENABLE=L(Valid), HSYNC=VSYNC=Low Active
PNL Interface Control 1	0010 h	001F h	Div ratio = 1/2 1H(Line)=16clock
PNL Interface Control 2	0011 h	0000 h	1clock
PNL Interface Control 3	0012 h	0000 h	0clock
PNL Interface Control 4	0020 h	021E h	30clock/8
PNL Interface Control 5	0021 h	0000 h	0clock
PNL Interface Control 6	0022 h	0000 h	0clock
Window Horizontal RAM Address 1	0210 h	0000 h	Start Address X=00h
Window Horizontal RAM Address 2	0211 h	00EF h	End Address X=EFh
Window Vertical RAM Address 1	0212 h	0000 h	Start Address Y=00h
Window Vertical RAM Address 2	0213 h	018F h	Start Address Y=18Fh
Gamma Control 1	0300 h	0706 h	Gamma Setting
Gamma Control 2	0301 h	0607 h	Gamma Setting
Gamma Control 3	0302 h	0301 h	Gamma Setting
Gamma Control 4	0303 h	0202 h	Gamma Setting
Gamma Control 5	0304 h	0303 h	Gamma Setting
Gamma Control 6	0305 h	0207 h	Gamma Setting
Gamma Control 7	0306 h	0808 h	Gamma Setting
Gamma Control 8	0307 h	0706 h	Gamma Setting
Gamma Control 9	0308 h	0607 h	Gamma Setting
Gamma Control 10	0309 h	0301 h	Gamma Setting
Gamma Control 11	030A h	0303 h	Gamma Setting
Gamma Control 12	030B h	0202 h	Gamma Setting
Gamma Control 13	030C h	0207 h	Gamma Setting
Gamma Control 14	030D h	1f1f h	Gamma Setting
Base Image Display Control	0401 h	0001h	Reversed Image
Base Image Vertical Scroll Control	0404 h	0000 h	Non-Scroll
LCD Power Setup			
Display Control 1	0007 h	0001 h	FMARK = IC internal = Operating
Power Control 6	0110 h	0001 h	LCD Power ON
Power Sequence Control 1	0112 h	0060 h	
Power Control 1	0100 h	17B0 h	G/S=ON, Booster: VGH=6times, VGL=3times, AMP=1
Power Control 2	0101 h	0007 h	Booster Clock: 1st=1, 2nd=1/16, x1.00
Power Control 3	0102 h	01A8 h	Internal reference voltage = 4.0V
Power Control 4	0103 h	2e00 h	x0.98
VCOM High Voltage 1	0281 h	0015 h	x0.90
Power Control 2	0101 h	0014 h	Booster Clock: 1st=1, 2nd=1/32, x0.70
Power Control 3	0102 h	01AC h	Internal reference voltage = 4.5V, PSON =0, PON=1
Wait	150msec		

Display ON			
Display Control 1	0007 h	0021 h	Gatr = ON, Source = OFF VCOM=OFF
Wait	1msec		
Power Control 6	0110 h	0001 h	LCD Power ON
Power Control 1	0100 h	16B0 h	G/S=ON, Booster: VGH=6times, VGL=4times, AMP=1
Power Control 2	0101 h	0117 h	Booster Clock: 1st=1/2, 2nd=1/32, x1.00
Power Control 3	0102 h	01B8 h	Internal reference voltage = 4.0V, PSON =1, PON=1
Power Control 4	0103 h	2e00 h	x0.98
VCOM High Voltage 1	0281 h	0015 h	x0.90
Display Control 1	0007 h	0061 h	Gatr = ON, Source = OFF VCOM=ON
Wait	50msec		
Display Control 1	0007 h	0173 h	Base Image Display

7.5.3.Command List for Power OFF (Recommended Setting)

Setting Item	Index (Value)	Value(2byte Setting)	Remark
Display OFF			
Display Control 1	0007 h	0072 h	Display OFF
Wait	(50msec)		
Display Control 1	0007 h	0001 h	Display OFF
Wait	(150msec)		
Display Control 1	0007 h	0000 h	Display OFF
Power ON1			
Power Control 1	0100 h	0680 h	G/S=ON, Booster: VGH=6times, VGL=4times, AMP=1
Power Control 2	0101 h	0667 h	Booster Clock: 1st=1/2, 2nd=1/32, x1.00
Power Control 3	0102 h	01A8 h	Internal reference voltage = 4.5V, PSON =1, PON=0
Power Control 4	0103 h	0e00 h	VCOMG=0
Wait	(10msec)		
Power Control 1	0100 h	0600 h	G/S=ON, Booster: VGH=6times, VGL=4times, AMP=0
Power OFF2			
Power OFF			-

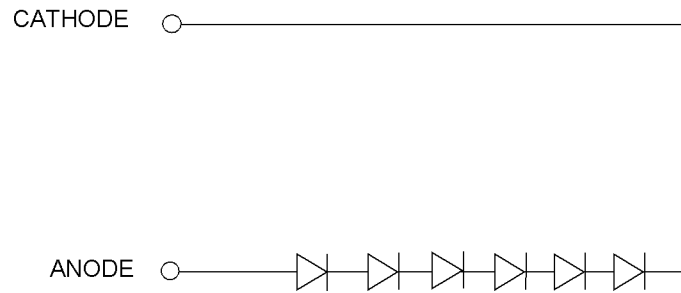
7.6.Back-light Specifications

7.6.1.Absolute Maximum Ratings (6 chips)

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Current	I _F	-	-	-	30	mA
Reverse Voltage	V _R	Note1	-	-	2.0	V
LED Power Dissipation	P _D	-	-	-	115	mW

Note 1 : I_R=10mA



7.6.2.Operating Characteristics

Ta=25°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Foward Voltage	V _F	I _F =20mA	18.0	19.2	20.4	V

8. Optical Specifications

8.1. Back-light Off

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Contrast Ratio	CR	Optimal	-	13	-	-	Note1
Reflectivity	R	Optimal	15	20	-	%	Note1,2
White Chromaticity	X	CIE	0.29	0.32	0.35	-	Note1
	Y		0.31	0.34	0.37	-	Note1,8
Red Chromaticity	X	CIE	0.37	0.40	0.43	-	Note1,8
	Y		0.31	0.34	0.37	-	Note1,8
Green Chromaticity	X	CIE	0.29	0.32	0.35	-	Note1,8
	Y		0.37	0.40	0.43	-	Note1,8
Blue Chromaticity	X	CIE	0.15	0.18	0.21	-	Note1,8
	Y		0.18	0.21	0.24	-	Note1,8

8.2. Back-light On

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	θ_{LEFT}	CR \geq 5	-	70	-	Degrees	Note3,4,5,12
	θ_{UP}		-	80	-	Degrees	Note3,4,5,12
	θ_{RIGHT}		-	70	-	Degrees	Note3,4,5,12
	θ_{DOWN}		-	58	-	Degrees	Note3,4,5,12
Contrast Ratio	CR	Optimal	-	105	-	-	Note4,8,11,12
Brightness	Y	Optimal	-	400	-	cd/m ²	Note8,10,11,12
Brightness Uniformity	Y	Optimal	70	-	-	%	Note7,10,11,12
Viewing Direction				6:00		o'clock	Note7,11
Response Rise Time	τ_r	$\theta=0^\circ$	-	23.0	-	ms	Note7,11,12
Response Fall Time	τ_d	Ta=25°C	-	53.0	-	ms	Note7,11,12
White Chromaticity	X	CIE	0.25	0.30	0.35	-	Note8,11,12
	Y		0.29	0.34	0.39	-	Note8,11,12
Red Chromaticity	X	CIE	0.48	0.53	0.58	-	Note8,11,12
	Y		0.32	0.37	0.42	-	Note8,11,12
Green Chromaticity	X	CIE	0.28	0.33	0.38	-	Note8,11,12
	Y		0.47	0.52	0.57	-	Note8,11,12
Blue Chromaticity	X	CIE	0.10	0.15	0.20	-	Note8,11,12
	Y		0.10	0.15	0.20	-	Note8,11,12

Note 1: Ring light measurement. (15deg. incident light detected at normal direction.)
 The reflection of white calibration plate is 100%. (Fig.1)

Schematic diagram of instrument

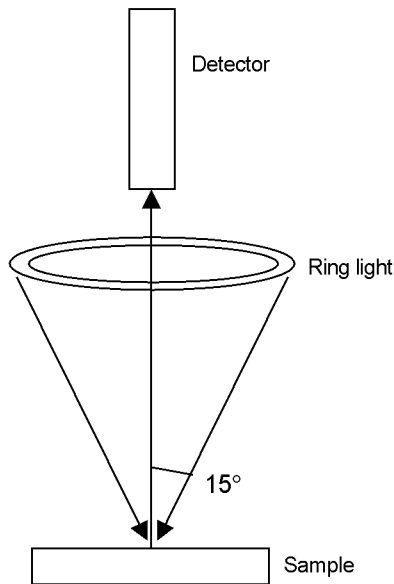


Fig. 1

Note 2 : The definition of Reflectivity is below.

$$\text{Reflectivity} = \frac{\text{Light detected level of the reflection by the display with all pixels white}}{\text{Light detected level of the reflection by the reflective standard}}$$

Note 3: The testing conditions are illustrated in Fig.2 and taken at Ta=25°C in a dark room
 Using ELDIM EZ contrast 160R system. The display is oriented landscape with the driver on the right. (Fig.2)

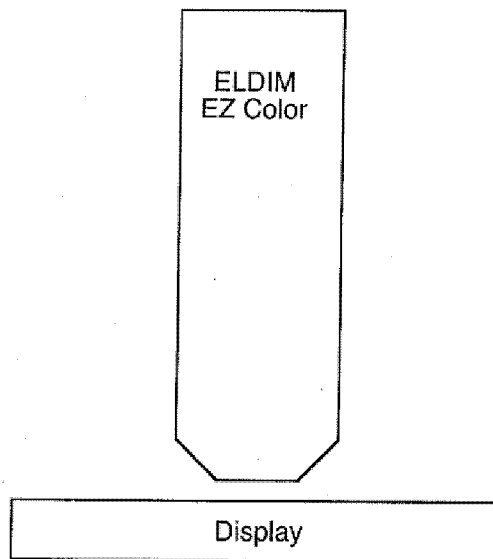


Fig. 2

Note 4 : The definition of contrast ratio is below.

$$\text{Contrast Ratio (CR)} = \frac{\text{Photo detector output with all pixels white}}{\text{Photo detector output with all pixels black}}$$

Note 5 : The definition of viewing angle is shown in Fig.4

Note 6 : The definition of response time is shown in Fig.5

Note 7 : The definition of brightness & brightness uniformity is shown in Fig.3

Note 8 : Critical optical characteristics.

Note 9 : The viewing / rubbing direction is the direction of least color inversion.

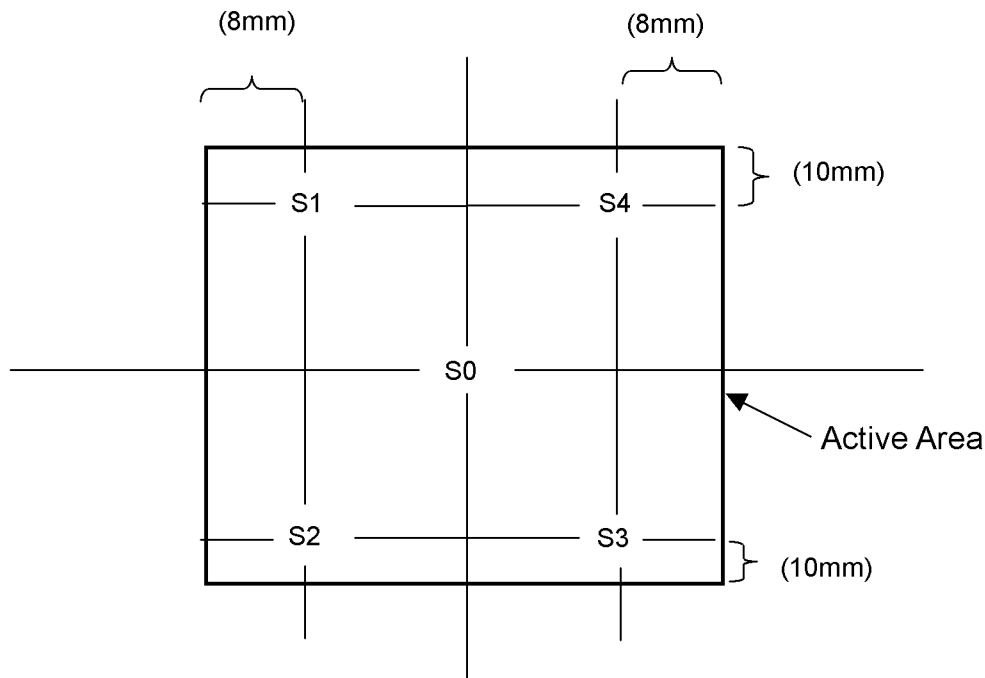
Note 10 : Brightness may also be referred to as luminance.

Note 11 : The measuring equipment are TOPCON BM-5.

Note 12 : 6LEDS back light, 20mA / chip

◆ Definition of Brightness Uniformity (Fig.3)

Definition is calculated from the 5 points (S0-S4) on the diagram below.

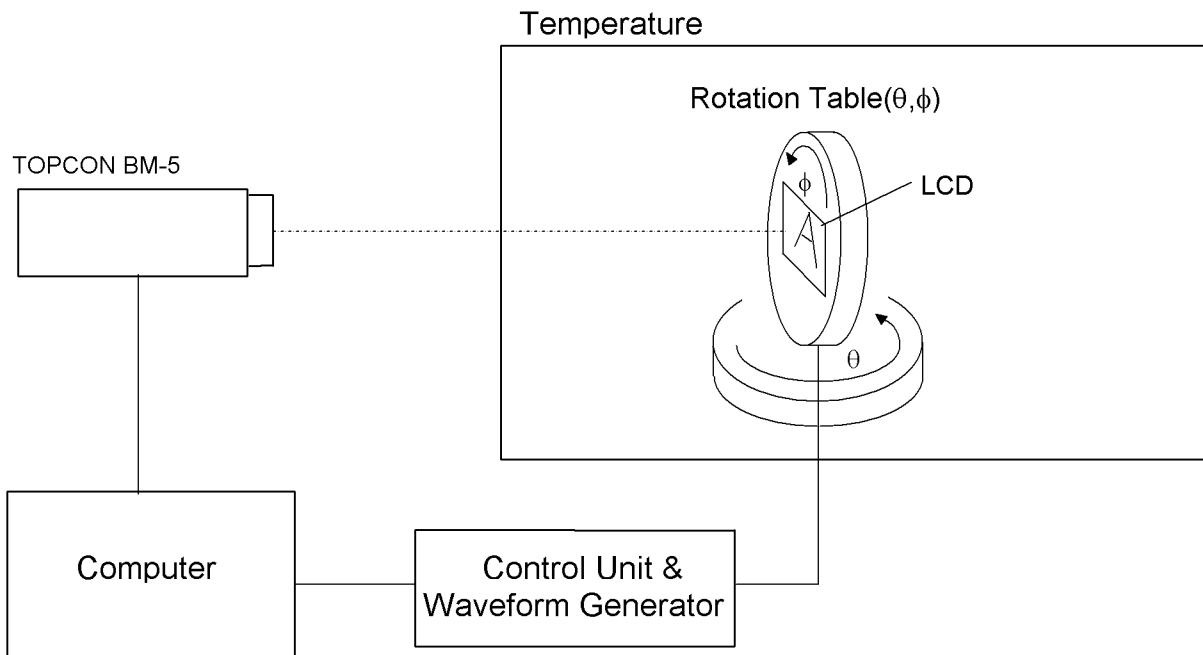


$$\text{Standard value of Brightness Uniformity [\%]} = \frac{\text{S0~S4 MIN}}{\text{S0~S4 MAX}} \times 100$$

Fig. 3

◆ Method of Viewing Angle Measurement (Fig.4)

- (1) Measuring Device
TOPCON BM-5, Measuring Field:1°
- (2) Measuring Point
Center of display: Same as Method of Brightness Measurement
- (3) Angle of Measuring
 θ : An angle vertical to perpendicular line from the viewing direction.
 ϕ : An angle horizontal to perpendicular from the viewing direction.



(4) Method of Measuring

Set rotation table to $\phi=0^\circ$ and set BM-5 to contrast 10 to measure angle $\pm\theta$ for left and right direction of horizontal viewing angle ϕ . Also set rotation table to $\phi=90^\circ$ and set BM-5 to contrast 10 to measure angle $\pm\theta$ for up and down direction of vertical viewing angle θ .

Fig. 4

◆ Measuring Response Time (Fig.5)

- (1) Measuring Device
TOPCON BM-5, Measuring Field: 1°
Tektronix Digital Oscilloscope
- (2) Measuring Point
Center of display, same as Method of Brightness Measurement
- (3) Method of Measuring
 - Set LCD panel to $\theta=0^\circ$, and $\phi=0^\circ$.
 - Input white→black→white to display by switching signal voltage.
 - If the luminance is 0% and 100% immediately before the change of signal voltage, then τ_r is optical response time during the change from 90% to 10% immediately after rise of signal voltage, and τ_d is optical response time during the change from 10% to 90% immediately after decay of signal voltage.

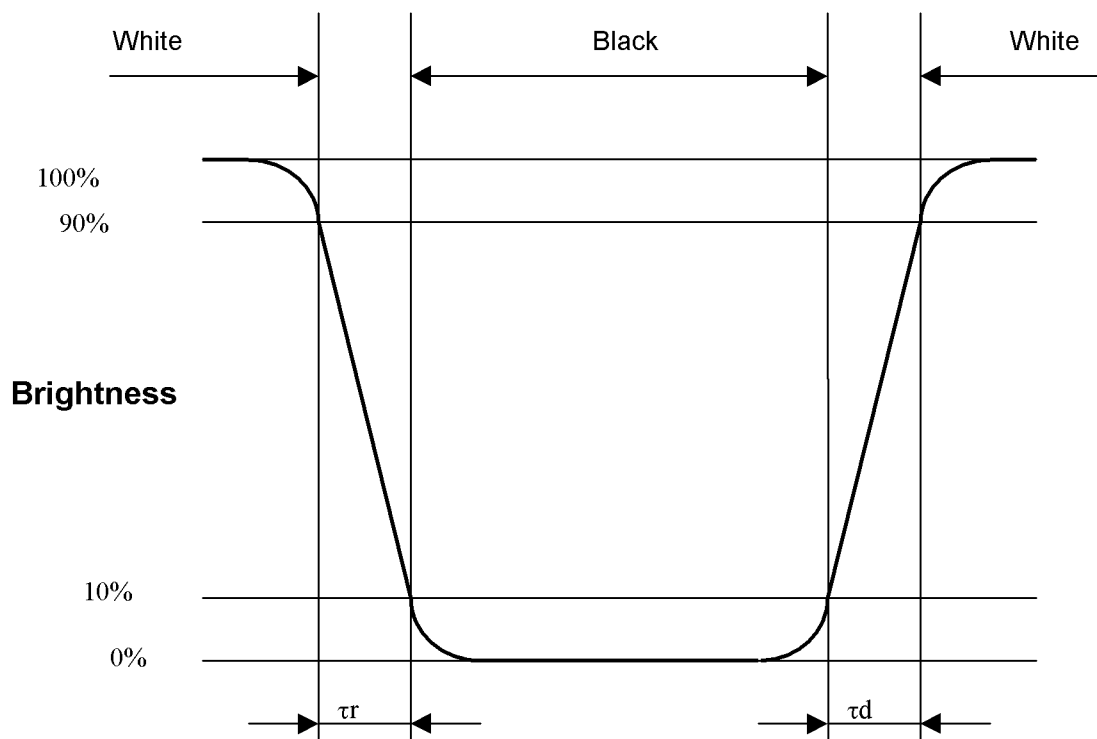
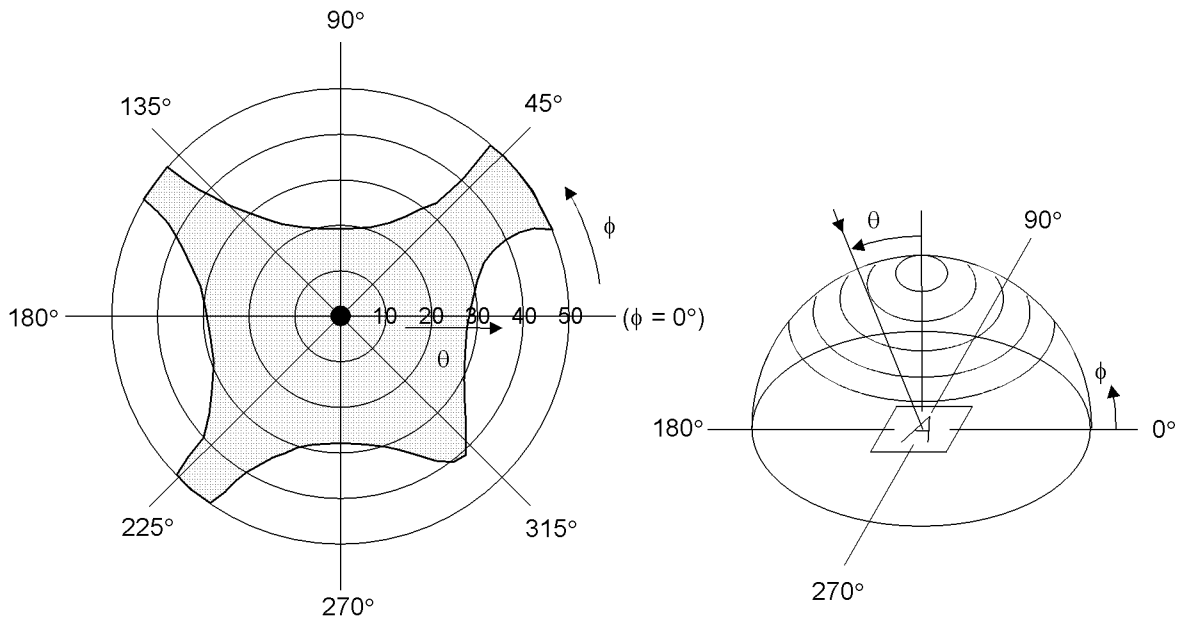



Fig. 5

8.3. Definition of Viewing Angle and Optimum Viewing Area

*Point • shows the point where contrast ratio is measured. : $\theta = 0^\circ$, $\phi = -^\circ$

*Driving condition: $f_f = 60\text{Hz}$



*Area  shows typ. $CR \geq 30$

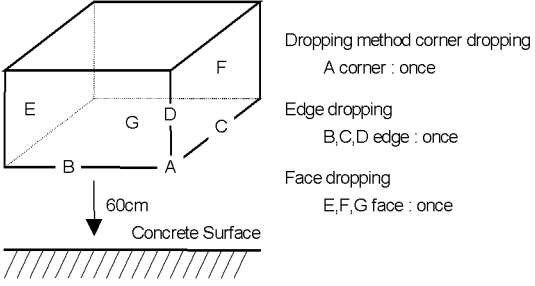
9. Test

No abnormal function and appearance are found after the following tests.

Conditions: Unless otherwise specified, tests will be conducted under the following condition.

Temperature: $20\pm 5^{\circ}\text{C}$ Humidity : $65\pm 5\% \text{RH}$

tests will be not conducted under functioning state.

No.	Parameter	Conditions	Notes
1	High Temperature Operating	$70^{\circ}\text{C}\pm 2^{\circ}\text{C}$, 240hrs (operation state)	
2	Low Temperature Operating	$-20^{\circ}\text{C}\pm 2^{\circ}\text{C}$, 240hrs (operation state)	1
3	High Temperature Storage	$80^{\circ}\text{C}\pm 2^{\circ}\text{C}$, 240hrs	2
4	Low Temperature Storage	$-30^{\circ}\text{C}\pm 2^{\circ}\text{C}$, 240hrs	1,2
5	Damp Proof Test	$40^{\circ}\text{C}\pm 2^{\circ}\text{C}$, $90\sim 95\% \text{RH}$, 240hrs	1,2
6	Heat Cycle Test	-40°C (30min) \leftrightarrow 80°C (30min) 20 cycles	2
7	Vibration Test	Total fixed amplitude : 1.5mm Vibration Frequency : 10~55Hz One cycle 60 seconds to 3 directions of X, Y, Z each 15 minutes	3
8	Shock Test	To be measured after dropping from 60cm high the concrete surface in packing state. 	
9	ESD Test	Voltage the stamp passable to each terminal. Condition: Machine model(MIL test method) Stamp passable voltage: 300V Capacity: 200pF Electric discharge resistance: 0Ω	

Note 1 :No dew condensation to be observed.

Note 2: The function test shall be conducted after 4 hours storage at the normal Temperature and humidity after removed from the test chamber.

Note 3 :Vibration test will be conducted to the product itself without putting it in a container.

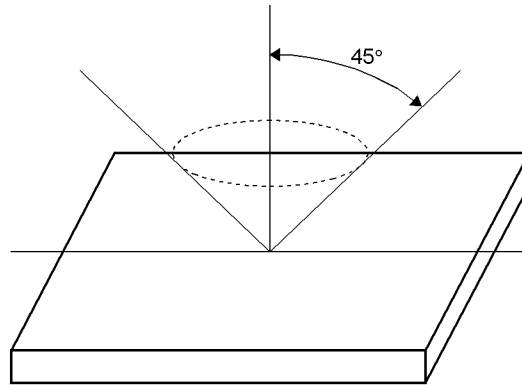
10. Appearance Standards

10.1. Viewing distance and angle

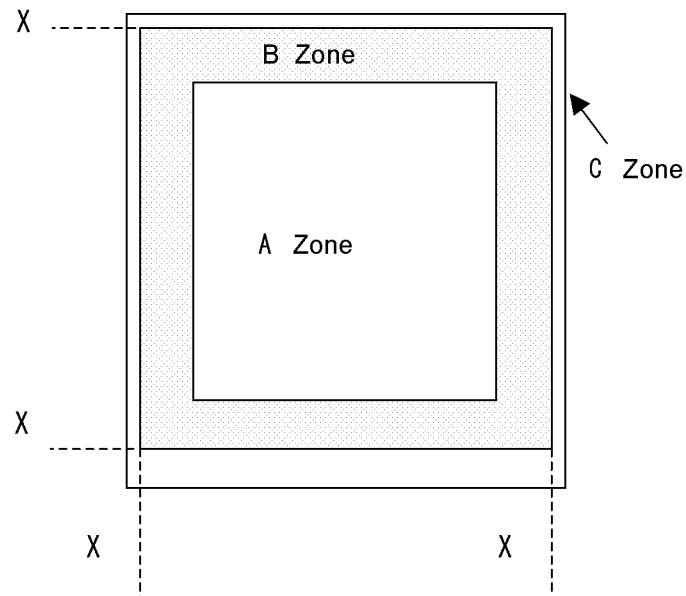
The LCD shall be inspected 300~ 750lx white fluorescent light.

The distance between the eyes and the sample shall be 35 ± 5 cm.

All directions for inspecting the sample should be within 45° against perpendicular line.



10.2. Definition of applicable Zones



A Zone: Active display area

B Zone: Out of active display area ~ Maximum seal line

C Zone: Rest parts

A Zone + B Zone = Validity viewing area

10.3.Standards

No.	Parameter	Criteria																																								
1	Black and White Spots, Foreign Substances	<p>(1) Round Shape</p> <table border="1"> <thead> <tr> <th rowspan="2">Dimension (mm) \ Zone</th> <th colspan="3">Acceptable Number</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>D < 0.1</td> <td colspan="2">Disregard</td> <td rowspan="3">Disregard</td> </tr> <tr> <td>0.1 < D ≤ 0.3</td> <td colspan="2">2</td> </tr> <tr> <td>D ≥ 0.3</td> <td colspan="2">0</td> </tr> </tbody> </table> <p>D = (Long + Short) / 2 *Each dot must keep the size ovrt 1/2.</p> <p>(2) Line Shape</p> <table border="1"> <thead> <tr> <th colspan="2">Zone</th> <th colspan="3">Acceptable Number</th> </tr> <tr> <th>X(mm) \ Y(mm)</th> <th>Y(mm)</th> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>≤ 0.1</td> <td>≤ 0.04</td> <td colspan="2">Disregard</td> <td rowspan="3">Disregard</td> </tr> <tr> <td>≤ 2.0</td> <td>≤ 0.04</td> <td colspan="2">2</td> </tr> <tr> <td>> 2.0</td> <td>-</td> <td colspan="2">0</td> </tr> </tbody> </table> <p>X : Length Y : Width</p>	Dimension (mm) \ Zone	Acceptable Number			A	B	C	D < 0.1	Disregard		Disregard	0.1 < D ≤ 0.3	2		D ≥ 0.3	0		Zone		Acceptable Number			X(mm) \ Y(mm)	Y(mm)	A	B	C	≤ 0.1	≤ 0.04	Disregard		Disregard	≤ 2.0	≤ 0.04	2		> 2.0	-	0	
Dimension (mm) \ Zone	Acceptable Number																																									
	A	B	C																																							
D < 0.1	Disregard		Disregard																																							
0.1 < D ≤ 0.3	2																																									
D ≥ 0.3	0																																									
Zone		Acceptable Number																																								
X(mm) \ Y(mm)	Y(mm)	A	B	C																																						
≤ 0.1	≤ 0.04	Disregard		Disregard																																						
≤ 2.0	≤ 0.04	2																																								
> 2.0	-	0																																								
2	Air Bubbles (between glass & polarizer), Stroke marks	<p style="text-align: right;">D = (Long + Short) / 2</p> <table border="1"> <thead> <tr> <th rowspan="2">Dimension (mm) \ Zone</th> <th colspan="3">Acceptable Number</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>D < 0.15</td> <td colspan="2">Disregard</td> <td rowspan="3">*1</td> </tr> <tr> <td>0.15 ≤ D ≤ 0.30</td> <td colspan="2">3</td> </tr> <tr> <td>0.3 < D</td> <td colspan="2">0</td> </tr> </tbody> </table> <p>*1: No progressive. No float at the edge.</p>	Dimension (mm) \ Zone	Acceptable Number			A	B	C	D < 0.15	Disregard		*1	0.15 ≤ D ≤ 0.30	3		0.3 < D	0																								
Dimension (mm) \ Zone	Acceptable Number																																									
	A	B	C																																							
D < 0.15	Disregard		*1																																							
0.15 ≤ D ≤ 0.30	3																																									
0.3 < D	0																																									
3	Polarizer Scratches	<table border="1"> <thead> <tr> <th colspan="2">Zone</th> <th colspan="3">Acceptable Number</th> </tr> <tr> <th>X(mm) \ Y(mm)</th> <th>Y(mm)</th> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>≤ 0.1</td> <td>≤ 0.04</td> <td colspan="2">Disregard</td> <td rowspan="3">Disregard</td> </tr> <tr> <td>≤ 2.0</td> <td>≤ 0.04</td> <td colspan="2">2</td> </tr> <tr> <td>> 2.0</td> <td>-</td> <td colspan="2">0</td> </tr> </tbody> </table>	Zone		Acceptable Number			X(mm) \ Y(mm)	Y(mm)	A	B	C	≤ 0.1	≤ 0.04	Disregard		Disregard	≤ 2.0	≤ 0.04	2		> 2.0	-	0																		
Zone		Acceptable Number																																								
X(mm) \ Y(mm)	Y(mm)	A	B	C																																						
≤ 0.1	≤ 0.04	Disregard		Disregard																																						
≤ 2.0	≤ 0.04	2																																								
> 2.0	-	0																																								
4	Polarizer	Not to be conspicuous defects. Limit sample shall be determined by the arising demand.																																								
5	Polarizer Dirts	If the stains are removed easily from LCDP surface, the module is not defective.																																								

No.	Parameter	Criteria																		
6	Glass Scratches	Not to be conspicuous defects. Limit sample shall be determined by the arising demand.																		
7	Distance between Different Foreign Substance Defects	$D \leq 0.2$: 20mm or more $0.2 < D$: 40mm or more																		
8	(a) Bright Dot (b) Dark Dot	<table border="1"> <thead> <tr> <th rowspan="2">Zone Dimension (mm)</th> <th colspan="3">Acceptable Number</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>Bright Dot</td> <td colspan="2">3</td> <td rowspan="2">Disregard</td> </tr> <tr> <td>Dark Dot</td> <td colspan="2">2</td> </tr> <tr> <td>TOTAL</td> <td colspan="3">4</td> </tr> </tbody> </table> <p>*Green bright dots : 2 dots or less</p>	Zone Dimension (mm)	Acceptable Number			A	B	C	Bright Dot	3		Disregard	Dark Dot	2		TOTAL	4		
Zone Dimension (mm)	Acceptable Number																			
	A	B	C																	
Bright Dot	3		Disregard																	
Dark Dot	2																			
TOTAL	4																			
9	TWO Adjacent Dot	<table border="1"> <thead> <tr> <th rowspan="2">Zone Dimension (mm)</th> <th colspan="3">Acceptable Number</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>Bright Dot</td> <td colspan="2">3 PAIRS</td> <td rowspan="2">Disregard</td> </tr> <tr> <td>Dark Dot</td> <td colspan="2">2 PAIRS</td> </tr> </tbody> </table>	Zone Dimension (mm)	Acceptable Number			A	B	C	Bright Dot	3 PAIRS		Disregard	Dark Dot	2 PAIRS					
Zone Dimension (mm)	Acceptable Number																			
	A	B	C																	
Bright Dot	3 PAIRS		Disregard																	
Dark Dot	2 PAIRS																			
10	Three or More Adjacent Dot	NOT ALLOWED																		
11	Defect Distance	Bright Dot : 5mm min Dark Dot : 5mm min																		
12	Line Defect	NOT ALLOWED																		

Note 1: Bright Dot and Dark Dots are defined as follows:

Visible through 5% transmission ND filter and not visible through 1% transmission ND filter under the condition that black image (color 0) is on the display.

Note 2: No.8,9,10,11,12 inspection criteria

Include below with the 8.2.1.conditions for common inspection

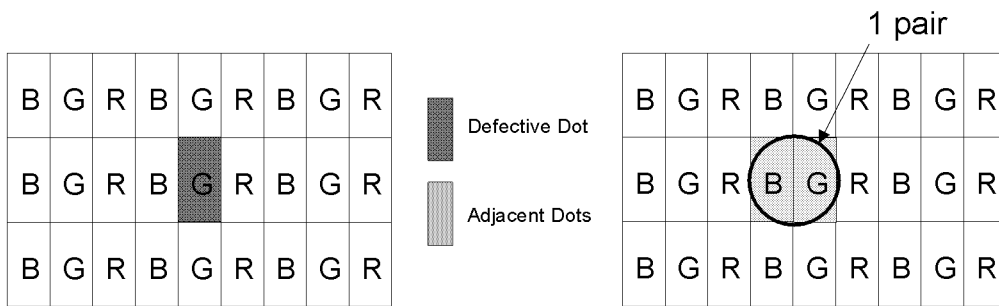
Luminance : 250 [lx](Transmission)

750 [lx](Reflection)

Distance : 30~40 [cm] (Perpendicular from panel surface)

Time : 5 [S] (After ND filter has been placed)

Note 3: Definition of adjacent



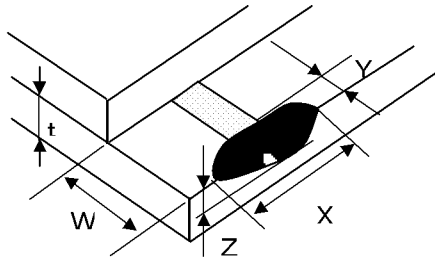
The defects that are not defined above and considered to be problem shall be reviewed and discussed by both parties.

No.	Parameter	Criteria
-----	-----------	----------

8

Chipped Glass

(1) Electrode Pad Areas and Terminal Areas



NG when chipping is produced on wiring or terminal.

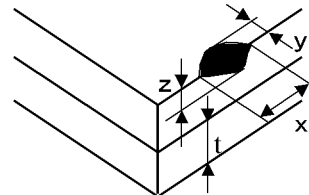
other

W	X	Y	Z
$W \leq 2.0$	Disregard	$Y \leq 0.3$	Disregard
$2.0 < W \leq 3.5$		$Y \leq 0.5$	
$3.5 < W \leq 4.0$		$Y \leq 0.8$	
$4.0 < W \leq 5.0$		$Y \leq 1.0$	
$W = 5.0 + \alpha$		$Y = 1.0 + \alpha$	

Y : depth direction to ridge line.

W : The length of FPC contact part.

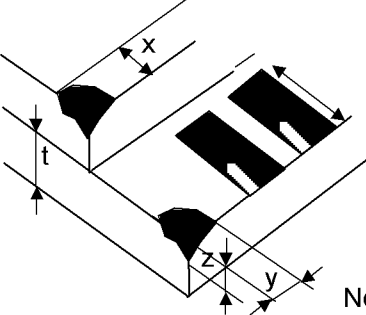
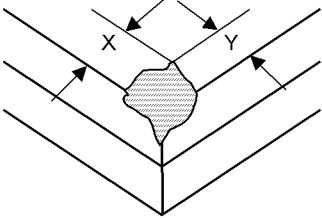
(2) Other than electrode pad areas and corner areas

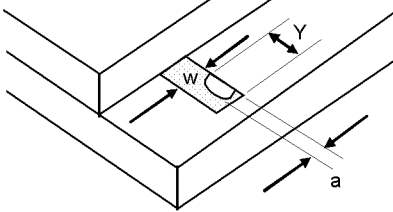


X	Y	Z
$\leq 2 \times t$	\leq	Disregard

*For LCD module with holder

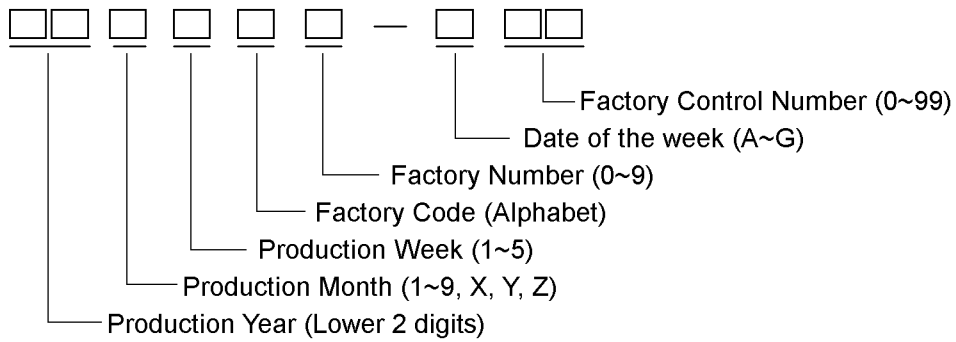
It is disregard. When it has no problem for appearance, reliability and progressiveness.

No.	Parameter	Criteria						
		<p>(3) Corner Areas</p> <p>1. Electrode Pad Areas</p> <p>NG when chipping is produced on wiring or terminal.</p> <p>other</p>  <table border="1" data-bbox="975 472 1377 568"> <thead> <tr> <th>X</th> <th>Y</th> <th>Z</th> </tr> </thead> <tbody> <tr> <td>$\leq 2 \times t$</td> <td>\leq</td> <td>Disregard</td> </tr> </tbody> </table> <p>*Penetration Crack Number: 1 When there are 2 points. $Z \leq 1/2 t$ Not covered on the marks or symbols.</p> <p>2. Other than electrode pad Areas</p>  <p>$X \leq 1.5$ & $Y \leq 0.5$ Or $X \leq 0.5$ & $Y \leq 1.5$</p> <p>*The direction of board thickness is disregarded.</p> <p>*For LCD module with holder It is disregard. When it has no problem for appearance, reliability and progressiveness.</p> <p>*It is not approved when a glass chip occurs with the part of the seal, wiring, terminal and, Polarizer.</p>	X	Y	Z	$\leq 2 \times t$	\leq	Disregard
X	Y	Z						
$\leq 2 \times t$	\leq	Disregard						

No.	Parameter	Criteria
9	Leak of terminal	 <p> $a/w \leq 1/3$ & $Y \leq 0.9$ Y :Length of pattern lack a :Width of the pattern lack w :Width of terminal </p>

11.Code System of Production Lot

The production lot of module is specified as follows.



12.Type Number

The type number of module is specified as follows.

355149AJ

13.Applying Precautions

Please contact us when questions and/or new problems not specified in this Specifications arise.

14. Precautions Relating Product Handling

The Following precautions will guide you in handling our product correctly.

- 1) Liquid crystal display devices
 1. The liquid crystal display panel used in the liquid crystal display module is made of plate glass. Avoid any strong mechanical shock. Should the glass break handle it with care.
 2. The polarizer adhering to the surface of the LCD is made of a soft material. Guard against scratching it.
- 2) Care of the liquid crystal display module against static electricity discharge.
 1. When working with the module, be sure to ground your body and any electrical equipment you may be using. We strongly recommend the use of anti static mats (made of rubber), to protect worktables against the hazards of electrical shock.
 2. Avoid the use of work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.
 3. Slowly and carefully remove the protective film from the LCD module, since this operation can generate static electricity.
- 3) When the LCD module must be stored for long periods of time:
 1. Protect the modules from high temperature and humidity.
 2. Keep the modules out of direct sunlight or direct exposure to ultraviolet rays.
 3. Protect the modules from excessive external forces.
- 4) Use the module with a power supply that is equipped with an overcurrent protector circuit, since the module is not provided with this protective feature.
- 5) Do not ingest the LCD fluid itself should it leak out of a damaged LCD module. Should hands or clothing come in contact with LCD fluid, wash immediately with soap.
- 6) Conductivity is not guaranteed for models that use metal holders where solder connections between the metal holder and the PCB are not used. Please contact us to discuss appropriate ways to assure conductivity.
- 7) For models which use CFL:
 1. High voltage of 1000V or greater is applied to the CFL cable connector area. Care should be taken not to touch connection areas to avoid burns.
 2. Protect CFL cables from rubbing against the unit and thus causing the wire jacket to become worn.
 3. The use of CFLs for extended periods of time at low temperatures will significantly shorten their service life.
- 8) For models which use touch panels:
 1. Do not stack up modules since they can be damaged by components on neighboring modules.
 2. Do not place heavy objects on top of the product. This could cause glass breakage.
- 9) For models which use COG, TAB, or COF:
 1. The mechanical strength of the product is low since the IC chip faces out unprotected from the rear. Be sure to protect the rear of the IC chip from external forces.
 2. Given the fact that the rear of the IC chip is left exposed, in order to protect the unit from electrical damage; avoid installation configurations in which the rear of the IC chip runs the risk of making any electrical contact.

- 10) Models which use flexible cable, heat seal, or TAB:
 1. In order to maintain reliability, do not touch or hold by the connector area.
 2. Avoid any bending, pulling, or other excessive force, which can result in broken connections.

- 11) In case of buffer material such as cushion / gasket is assembled into LCD module, it may have an adverse effect on connecting parts (LCD panel-TCP / HEAT SEAL / FPC / etc., PCB-TCP / HEAT SEAL / FPC etc., TCP-HEAT SEAL, TCP-FPC, HEAT SEAL-FPC, etc.) depending on its materials.
Please check and evaluate these materials carefully before use.

- 12) In case of acrylic plate is attached to front side of LCD panel, cloudiness (very small cracks) can occur on acrylic plate, being influenced by some components generated from polarizer film.
Please check and evaluate those acrylic materials carefully before use.

15. Warranty

This product has been manufactured to your company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. When the product is in CFL models, CFL service life and brightness will vary according to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.
5. We cannot accept responsibility for intellectual property of a third party, which may arise through the application of our product to your assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.
6. Optrex will not be held responsible for any quality guarantee issue for defect products judged as Optrex-origin in 2 (two) years from Optrex production or 1 (one) year from Optrex Group delivery whichever is shorter.