DAC1653Q/DAC1658Q

Quad 16-bit DAC: 10 Gbps JESD204B interface: x2, x4 and x8 interpolating

Advance data sheet

Revision 2.3.1

1. General description

DAC1653Q and DAC1658Q are high-speed, high-performance 16-bit quad channel Digital-to-Analog Converters (DACs). The devices provide sample rates up to 2 Gsps with selectable ×2, ×4 and ×8 interpolation filters optimized for multi-carrier and broadband wireless transmitters.

When both devices are referred to in this data sheet, the following convention will be used: DAC165xQ.

The DAC165xQ integrates a JEDEC JESD204B compatible high-speed serial input data interface running up to 10 Gbps over eight differential lanes. It offers numerous advantages over traditional parallel digital interfaces:

- Easier Printed-Circuit Board (PCB) layout
- Lower radiated noise
- Lower pin count
- Self-synchronous link
- Skew compensation
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compatible
- Harmonic clocking support
- Assured FPGA interoperability

There are two versions of the DAC165xQ:

- Low common-mode output voltage (part identification DAC1653Q)
- High common-mode output voltage (part identification DAC1658Q)

Two optional on-chip digital modulator converts the complex I/Q patterns from baseband to IF. The mixer frequency is set by writing to the Serial Peripheral Interface (SPI) control registers associated with the on-chip 40-bit Numerically Controlled Oscillator (NCO). This accurately places the IF carrier in the frequency domain. The 13-bit phase adjustment feature, the 12-bit digital gain and the 16-bit digital offset enable full control of the analog output signals.

The DAC165xQ is fully compatible with device subclass 1 of the JEDEC JESD204B standard, guaranteeing deterministic and repeatable interface latency using the differential SYSREF signal.

Multiple Device Synchronization (MDS) enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period. MDS is ideal for LTE and LTE-A MIMO transceiver applications.

The DAC165xQ includes a very low noise bypass-able integrated Phase-Locked Loop (PLL). This PLL is fully integrated and does not need any external passive components. The device also supports harmonic clocking. Both features are useful to reduce system-level clock synthesis and distribution challenges.

The internal regulator adjusts the full-scale output current between 10 mA and 30 mA.

The device is available in a HLA72 package (10 mm × 10 mm).

2. Features and benefits

- Quad channel 16-bit resolution
- 2 GSps maximum output update rate
- JEDEC JESD204B device subclass I compatible: SYSREF based deterministic and repeatable interface latency
- Multiple device synchronization enables multiple DAC channels to be sample synchronous and phase coherent to within one DAC clock period
- Up to 8 configurable JESD204B serial input lanes running up to 10 Gbps with embedded termination and programmable equalization gain (CTLE)
- SPI interface (3-wire or 4-wire mode) for control setting and status monitoring
- Flexible SPI power supply (1.8 V or 1.2 V) ensuring compatibility with on-board SPI bus
- Differential scalable output current from 10 mA to 30 mA
- Two embedded NCO with 40-bit programmable frequency and 16-bit phase adjustment
- Embedded complex (IQ) digital modulator
- Very low noise bypass-able integrated Phase-Locked Loop (PLL); no external capacitors
- 1.2 V and 3.3 V power supplies (for DAC1653Q series, the 3.3V supply voltage can be lowered to 2.8V for lower power consumption)
- Flexible differential SYNC signals power supply (1.8 V or 1.2 V) ensuring compatibility with on-board devices
- Embedded Temperature Sensor
- Configurable IOs pins for monitoring, interrupt
- XBERT features (PRBS31, 23, 15, 7, JTSPAT, STLTP)
- SFDR = 87 dBc typical (band = Nyquist, f_s = 1.50 Gsps; interpolation ×2; f_{out} = 50 MHz)
- NSD = −164 dBm/Hz typical (f_o = 20 MHz)
- IMD3 = 86 dBc typical (f_s = 1.50 Gsps; interpolation ×2; f_{o1} = 150 MHz; f_{o2} = 151 MHz)
- Four carriers WCDMA ACLR = 75 dBc typical (f_s = 1.50 Gsps; f_{NCO} = 350 MHz)
- RF enable/disable pin and RF automatic mute
- Clock divider by 2, 4, 6 and 8 available at the input of the clock path
- Group delay compensation
- Embedded Power On Reset
- Power-down mode controls
- On-chip 0.7 V reference
- Industrial temperature range −40 °C to +85 °C
- Low (DAC1653Q) or high (DAC1658Q) common-mode output voltage
- HLA 72 pins package (10 mm ´ 10 mm)
- Lane swapping and polarity swapping
- Signal Power Detector, IQ-Range detector, Level detectors with Auto-Mute feature

3. Applications

- Wireless infrastructure radio base station transceivers, including: LTE-A, LTE, MC-GSM, W-CDMA, TD-SCDMA
- LMDS/MMDS, point-to-point microwave back-haul
- Direct Digital Synthesis (DDS) instruments
- High-definition video broadcast production equipment
- Automated Test Equipment (ATE)

4. ORDERING INFORMATION

Table 1. Ordering information

Type number	Package			
	Name	Description	Shipping Packaging	Version
DAC1653Q2G0NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1653Q1G5NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1653Q1G0NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1658Q2G0NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1658Q1G5NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1658Q1G0NAGA8	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tape & Reel	PSC-4438
DAC1653Q2G0NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1653Q1G5NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1653Q1G0NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1658Q2G0NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1658Q1G5NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438
DAC1658Q1G0NAGA	HLA72	HLA 10.0 × 10.0 × 0.85 mm; no lead	Tray	PSC-4438

5. BLOCK DIAGRAM

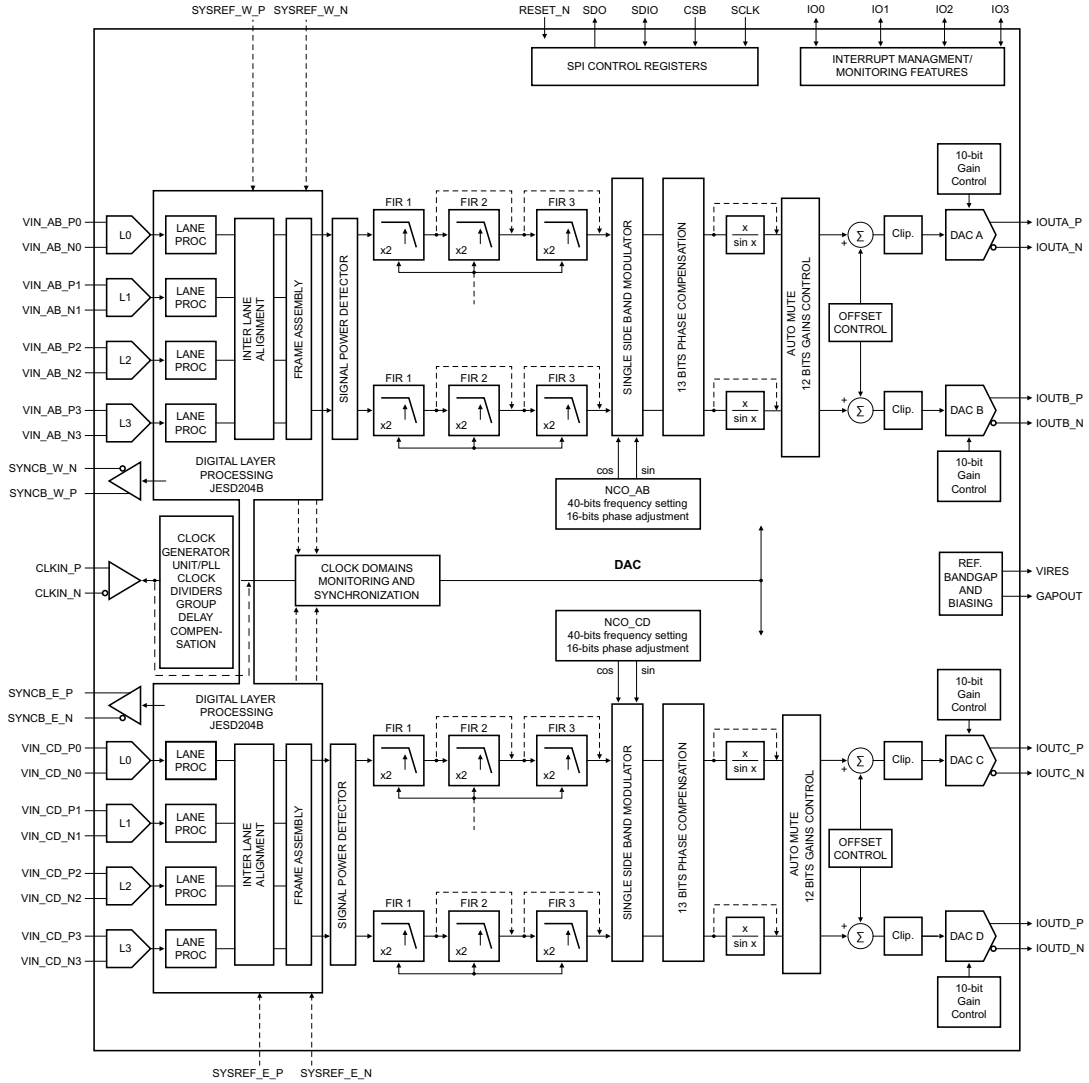


Fig 1. Block diagram

6. PINNING INFORMATION

6.1 Pinning

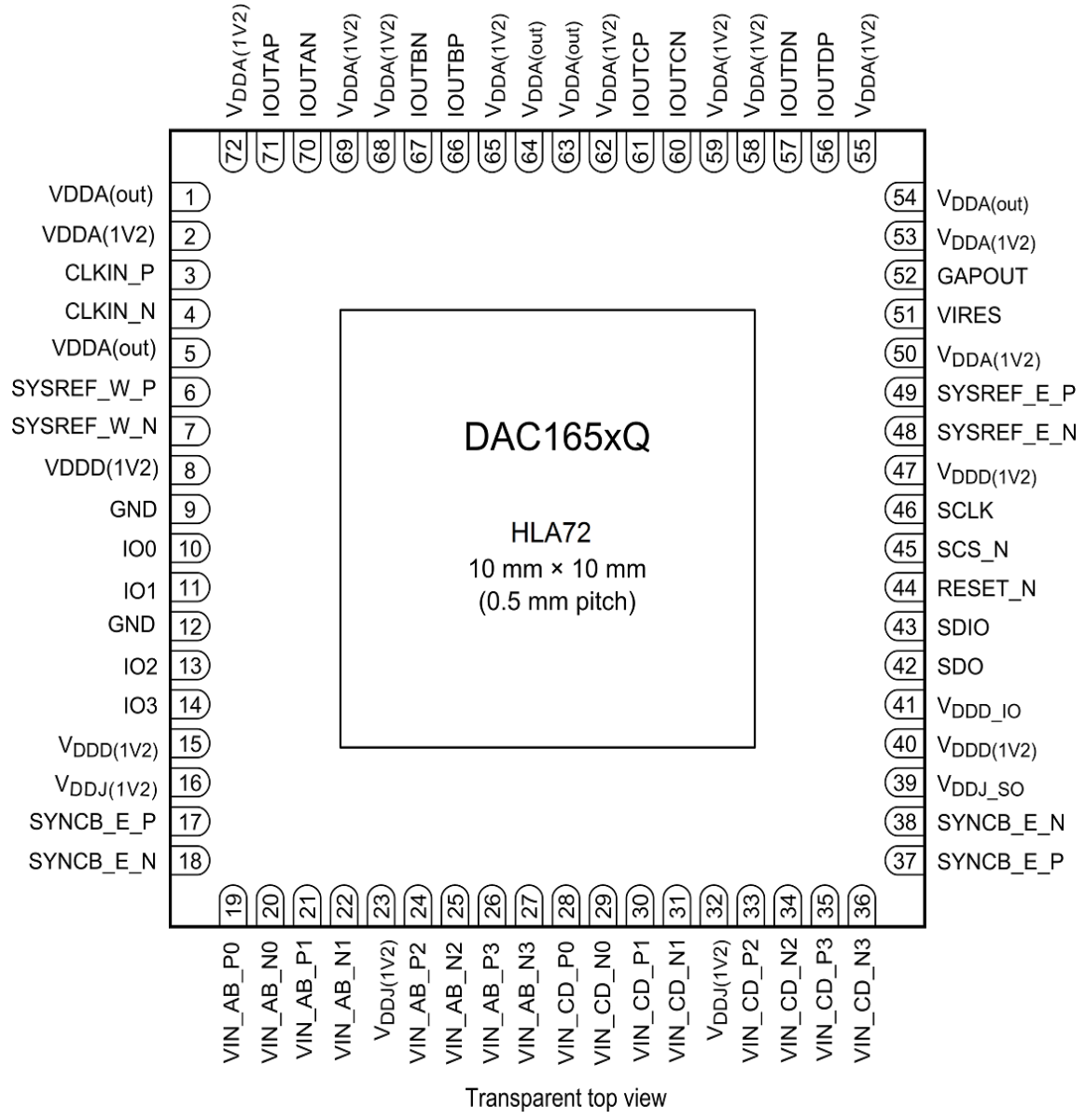


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
$V_{DDA(out)}$	1	P	DAC output analog power supply
$V_{DDA(1V2)}$	2	P	1.2 V analog power supply
CLKIN_P	3	I	positive clock input (AC coupling recommended ;internal biasing and resistor load included)
CLKIN_N	4	I	negative clock input (AC coupling recommended; internal biasing and resistor load included)
$V_{DDA(out)}$	5	P	DAC output analog power supply
SYSREF_W_P	6	I/O	multiple devices synchronization positive signal, west side (DC coupling recommended)
SYSREF_W_N	7	I/O	multiple devices synchronization negative signal, west side (DC coupling recommended)
$V_{DDD(1V2)}$	8	P	1.2 V digital power supply
GND	9	G	ground
IO0	10	I/O	IO port bit 0
IO1	11	I/O	IO port bit 1
GND	12	G	ground
IO2	13	I/O	IO port bit 2
IO3	14	I/O	IO port bit 3
$V_{DDD(1V2)}$	15	P	1.2 V digital power supply
$V_{DDJ(1V2)}$	16	P	1.2 V JESD204B interface power supply
SYNCB_W_P	17	O	JESD204B SYNC signal, west side positive output (DC coupling recommended)
SYNCB_W_N	18	O	JESD204B SYNC signal, west side negative output (DC coupling recommended)
VIN_AB_P0	19	I	DAC A/B lane 0 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_N0	20	I	DAC A/B lane 0 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_P1	21	I	DAC A/B lane 1 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_N1	22	I	DAC A/B lane 1 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
$V_{DDJ(1V2)}$	23	P	1.2 V JESD204B interface power supply
VIN_AB_P2	24	I	DAC A/B lane 2 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_N2	25	I	DAC A/B lane 2 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_P3	26	I	DAC A/B lane 3 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_AB_N3	27	I	DAC A/B lane 3 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_P0	28	I	DAC C/D lane 0 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_N0	29	I	DAC C/D lane 0 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_P1	30	I	DAC C/D lane 1 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)

Table 2. Pin description

Symbol	Pin	Type[1]	Description
VIN_CD_N1	31	I	DAC C/D lane 1 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
$V_{DDJ(1V2)}$	32	P	1.2 V JESD204B interface power supply
VIN_CD_P2	33	I	DAC C/D lane 2 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_N2	34	I	DAC C/D lane 2 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_P3	35	I	DAC C/D lane 3 serial interface, positive input (AC coupling recommended, internal biasing and resistor load included)
VIN_CD_N3	36	I	DAC C/D lane 3 serial interface, negative input (AC coupling recommended, internal biasing and resistor load included)
SYNCB_E_P	37	O	JESD204B SYNC signal, east side positive output (DC coupling recommended)
SYNCB_E_N	38	O	JESD204B SYNC signal, east side negative output (DC coupling recommended)
V_{DDJ_SO}	39	P	JESD204B SYNC output buffer power supply (1.2 V or 1.8 V)
$V_{DDD(1V2)}$	40	P	1.2 V digital power supply
V_{DDD_IO}	41	P	digital IO power supply (1.2 V or 1.8 V) (including SPI)
SDO	42	O	SPI data output
SDIO	43	I/O	SPI data input/output
RESET_N	44	I	general reset (active LOW)
SCS_N	45	I	SPI chip select (active LOW)
SCLK	46	I	SPI clock input
$V_{DDD(1V2)}$	47	P	1.2 V digital power supply
SYSREF_E_N	48	I/O	multiple devices synchronization negative signal, east side (DC coupling recommended)
SYSREF_E_P	49	I/O	multiple devices synchronization positive signal, east side (DC coupling recommended)
$V_{DDA(1V2)}$	50	P	1.2 V analog power supply
VIRES	51	I/O	biasing resistor (connect this pin to GND through 562ohm resistor)
GAPOUT	52	I/O	bandgap output voltage
$V_{DDA(1V2)}$	53	P	1.2 V analog power supply
$V_{DDA(out)}$	54	P	DAC output analog power supply
$V_{DDA(1V2)}$	55	P	1.2 V analog power supply
IOUTD_P	56	O	DAC D output current
IOUTD_N	57	O	complementary DAC D output current
$V_{DDA(1V2)}$	58	P	1.2 V analog power supply
$V_{DDA(1V2)}$	59	P	1.2 V analog power supply
IOUTC_N	60	O	complementary DAC C output current
IOUTC_P	61	O	DAC C output current
$V_{DDA(1V2)}$	62	P	1.2 V analog power supply
$V_{DDA(out)}$	63	P	DACoutput analog power supply
$V_{DDA(out)}$	64	P	DACoutput analog power supply
$V_{DDA(1V2)}$	65	P	1.2 V analog power supply
IOUTB_P	66	O	DAC B output current
IOUTB_N	67	O	complementary DAC B output current

Table 2. Pin description

Symbol	Pin	Type[1]	Description
$V_{DDA(1V2)}$	68	P	1.2 V analog power supply
$V_{DDA(1V2)}$	69	P	1.2 V analog power supply
IOUTA_N	70	O	complementary DAC A output current
IOUTA_P	71	O	DAC A output current
$V_{DDA(1V2)}$	72	P	1.2 V analog power supply

[1] P: power supply; G: ground; I: input; O: output.

[2] JESD204B input lanes can be swapped between P and N using dedicated registers. The order of lanes can be updated logically (see Section 11.9.5.3).

7. LIMITING VALUES

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDA(out)}$	DAC output analog supply voltage		–0.5	+4.6	V
$V_{DDD(1V2)}$	digital supply voltage		–0.5	+1.5	V
$V_{DDDJ1V2)}$	1.2 V JESD204B interface power supply		–0.5	+1.5	V
$V_{DDA(1V2)}$	analog supply voltage		–0.5	+1.5	V
V_{DDD_IO}	I/O digital supply voltage	pins SDO; SDIO; SCLK; SCS_N; RESET_N; ; IO0; IO1; IO2; IO3	–0.5	2.1	V
V_{DDJ_SO}	digital supply voltage for differential sync output buffers	pins SYNCB_E_P; SYNCB_E_N; SYNCB_W_P; SYNCB_W_N	–0.5	2.1	V
V_I	input voltage for JESD204B lanes	pins VIN_CD_Px; VIN_CD_Nx; VIN_AB_Px; VIN_AB_Nx	–0.5	1.5	V
V_I	input voltage	input pins referenced to GND. pins CLKIN_P, CLKIN_N, SYSREF_W_P, SYSREF_W_N, SYSREF_E_P, SYSREF_E_N	–0.5	1.95	V
V_O	output voltage	pins IOUTA_P; IOUTA_N; IOUTB_P; IOUTB_N;IOUTC_P; IOUTC_N; IOUTD_P; IOUTD_N; referenced to GND	–0.5	+4.6	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		–40	+125	°C

8. THERMAL CHARACTERISTICS

Table 4.Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
JEDEC 4L board					
θ_{JA}	thermal resistance from junction to ambient		[3]	22.5	°C/W
θ_{JC}	thermal resistance from junction to case		[3]	9.3	°C/W
θ_{JB}	thermal resistance from junction to bottom case		[3]	0.4	°C/W
ψ_{JT}	Junction to top characterization parameter		[3]	0.07	°C/W
ψ_{JB}	Junction to board characterization parameter		[3]	0.3	°C/W

[3] In compliance with JEDEC test board in free air; 5.9x7.2mm ePAD soldered down, 48 thermal via

Multi layers board, air flow or heat sinking increases heat dissipation with effective reduction of θ_{JA}. It may be required for sustaining operation at 85°C and fulfill the maximum Junction temperature conditions. The DAC165xQ includes a junction temperature sensor that could be very useful in order to check in real system that the specification of the maximum junction temperature T_j is guarantied (see Section 11.7).

The Table 5 shows evolution of θ_{JA} in several PCB / air flow configuration:

Table 5. θ_{ja} in different PCB / air flow configuration.

PCB configuration	air flow			Unit
	0 m/s	1m/s	2m/S	
4 layers board 48 thermal vias	22.5	18.9	17.4	°C/W
6 layers board 48 thermal vias	18.8	15	13.6	°C/W
12 layers board 48 thermal vias	12.7	9.5	8.5	°C/W

9. STATIC CHARACTERISTICS

9.1 Common characteristics

Table 6. Common characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; PLL off; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
Voltages							
$V_{DDA(out)}$	DAC output analog supply voltage	DAC1658Q: high common mode output	C	3.15	3.3	3.45	V
		DAC1653Q: low common mode output	C	2.5	3.3	3.45	V
$V_{DDD(1V2)}$	digital supply voltage	Fs ≤ 1.5 GHz	C	1.14	1.2	1.26	V
		Fs > 1.5 GHz		1.25	1.3	1.35	V
$V_{DDA(1V2)}$	analog supply voltage	Fs ≤ 1.5 GHz	C	1.14	1.2	1.26	V
		Fs > 1.5 GHz	C	1.25	1.3	1.35	V
V_{DDD_IO}	I/O digital supply voltage		C	1.14	1.2	1.9	V
V_{DDJ_SO}	digital supply voltage for differential SYNC output buffers		C	1.14	1.2	1.9	V
Temperature Sensor							
T_α	temperature sensor coefficient		C	-	4.64	-	°C
T_{offset}	temperature sensor offset		C	-	50.3	-	°C
Clock inputs (pins CLKIN_P, CLKIN_N)							
$V_{i(diff)}$	differential Peak-to-Peak voltage		D	400	1000	2000	mV
f_{clkin}	Input frequency compliance range	direct clocking	D			2000	MHz
		harmonic clocking (using clock divider)	D			3000	MHz
f_{ref}	PLL Input frequency compliance range. $f_{ref}=f_{clkin}/prediv$	in PLL mode	C	50	-	123	MHz
f_{dco}	PLL DCO frequency compliance range.	in PLL mode	D	3500	-	4710	MHz
$R_{i(diff)}$	differential input resistor		D	80	100	120	Ω
C_i	input capacitance		D	-	2	-	pF
Digital inputs/outputs (SYSREF_W_P/SYSREF_W_N, SYSREF_E_P/SYSREF_E_N)							
$V_{i(cm)}$	common-mode input voltage	$V_{DDD(IO)}$=1.8V	D	800	1200	1400	mV
		$V_{DDD(IO)}$=1.2V	D	800	950	1100	mV
$V_{i(diff)}$	differential Peak-to-Peak voltage		D	400	800	1000	mV
$R_{i(diff)}$	differential input resistor (could be disconnected see Table 99)		D	-	100	-	Ω

Table 6. Common characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; PLL off; no auxiliary DAC used; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	Min	Typ	Max	Unit
C_i	input capacitance		D	-	1.1	-	pF
Digital inputs (pins , SDIO, SCLK, SCS_N, RESET_N, IO0, IO1, IO2, IO3)							
V_{IL}	LOW-level input voltage		C	GND	-	$0.3V_{DDD\_IO}$	V
V_{IH}	HIGH-level input voltage		C	$0.7V_{DDD\_IO}$	-	V_{DDD_IO}	V
Digital inputs (VIN_Px/VIN_Nx) compliant with the LV-OIF-11G-SR; CML format							
$V_{pp\text{-}diff}$	differential peak-to-peak voltage	below 8 Gbps	C	80	-	-	mV
		above 8 Gbps	C	110	-	-	mV
Z_{diff}	differential impedance	controlled by SPI register	I	71	100	190	Ω
Hi-Z_{diff}	tri-state observed impendance		D	-	64	-	kΩ
DR	data rate		D	2	-	10	Gbps
Digital outputs (pins SYNC_OUT_P and SYNC_OUT_N)							
V_{cm}	common-mode voltage	controlled by SPI register			-		
		V_{DDJ_SO} = 1.8 V	D	1.0	-	1.7	V
		V_{DDJ_SO} = 1.2 V	D	0.4	-	1.1	V
$V_{O(diff)(swing)}$	swing differential output voltage		D	100	-	1200	mV
Digital outputs (pins SDO, SDIO, IO0, IO1, IO2, IO3)							
V_{OL}	LOW-level output voltage		D	-	-	$0.3V_{DDD(IO)}$	V
V_{OH}	HIGH-level output voltage		D	$0.7V_{DDD(IO)}$	-	-	V
Reference voltage output (pin GAPOUT)							
$V_{O(ref)}$	reference output voltage	T_{amb} = 25 °C	C	-	0.70	-	V
DAC output timing							
f_s	sampling rate	DAC165xQ2G0	C	-[2]	-	2000	Msps
		DAC165xQ1G5	C	-[2]	-	1500	Msps
		DAC165xQ1G0	C	-[2]	-	1000	Msps
t_s	settling time	t_o = ±0.5LSB	D	-	20	-	ns

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

[2] Minimum value is linked to the JESD204B link configuration and lane rate

9.2 Specific characteristics

Table 7. Specific characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC165xQ:			Unit
				Min	Typ	Max	
Currents							
$I_{DDA(out)}$	DAC output analog supply current	DAC1658Q , all use cases	C	-	116		mA
		DAC1653Q, all use cases	C	-	227		mA
I_{DDD_IO}	digital supply current for IO pins	depends on SPI and IO0/IO1/IO2/IO3 activity	C	-	< 1		mA
I_{DDD_SO}	digital supply current for SYNC pins	V_{DDD_SO} = 1.2 V	C	-	23		mA
		V_{DDD_SO} = 1.8 V	C	-	38		mA
$I_{DDD(1V2)}$	digital supply current	NCO off; ×4 interpolation; DLQ LMF222;					
		f_s = 983.04 Msps	C	-	361		mA
		f_s = 1228.8 Msps	C	-	429		mA
		f_s = 1474.56 Msps	C	-	497		mA
		NCO on at 150 MHz; ×4 interpolation; DLQ LMF222					
		f_s = 983.04 Msps	C	-	521		mA
		f_s = 1228.8 Msps	C	-	589		mA
		f_s = 1474.56 Msps	C	-	712		mA
$I_{DDA(1V2)}$	analog supply current	$V_{DDA(1V2)}$ = 1.2 V	C	-	371		mA
		$V_{DDA(1V2)}$ = 1.3 V	C	-	380		mA

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

Table 8. Specific characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658Q: High common-mode			DAC1653Q: .Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
Power										
P_{tot}	total power dissipation	f_s = 983.04 Msps; DLQ LMF222, NCO off; ×4 interpolation;	C	-	1371	-	-	1738	-	mW
		f_s = 1228.8 Msps; DLQ LMF222, NCO off; ×4 interpolation;	C	-	1457	-	-	1823	-	mW
		f_s = 1474.56 Msps; DLQ LMF222, NCO off; ×4 interpolation;	C	-	1543	-	-	1909	-	mW
		f_s = 1474.56 Msps; DLQ LMF222, NCO off; ×4 interpolation; $V_{DDA(out)}$ = 2.8 V;	C	-	na	-	-	1793	-	mW
		f_s = 983.04 Msps; DLQ LMF422, NCO off; ×2 interpolation;	C	-	1491	-	-	1857	-	mW
		f_s = 983.04 Msps; DLQ LMF222, NCO on; ×4 interpolation;	C	-	1371	-	-	1738	-	mW
		f_s = 983.04 Msps; DLQ LMF222, NCO off; ×4 interpolation;PLL on	C	-	1506	-	-	1872	-	mW
		full power-down	C	-	12	-	-	12	-	mW
Analog outputs (pins IOUTA_P, IOUTA_N, IOUTB_P, IOUTB_N, OUTC_P, IOUTC_N, IOUTD_P, IOUTD_N,)										
$I_{O(fs)}$	full-scale output current		D	10	20	30	10	20	30	mA
I_{bias}	DAC output biasing current	this additional current has to be used in order to calculate DAC output common mode voltage (Vcm)	D	-	1.6	-	-	1.6	-	mA
$I_{aux(fs)}$	AUX DAC full-scale output current	normal resolution	I	-	2.3	-	-	2.3	-	mA
		high resolution	D	-	0.04	-	-	0.04	-	mA
V_{O_comp}	output voltage compliance range	$V_{DDA(out)}$ =3.3 V	D	$V_{DDA(out)}$ -1.0	-	$V_{DDA(out)}$	$V_{DDA(out)}$ -1.0	-	$V_{DDA(out)}$	V
		$V_{DDA(out)}$ =2.5 V	D	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	V
R_o	internal output resistance		D	-	250	-	-	250	-	kΩ

Table 8. Specific characteristics

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; unless otherwise specified.

Symbol	Parameter	Conditions	Test	DAC1658Q: High common-mode			DAC1653Q: .Low common-mode			Unit
				Min	Typ	Max	Min	Typ	Max	
C_{PN}	differential output capacitance		D	-	0.5	-	-	0.5	-	pF
C_P	positive output capacitance		D	-	8.4	-	-	8.4	-	pF
C_N	negative output capacitance		D	-	8.3	-	-	8.3	-	pF

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

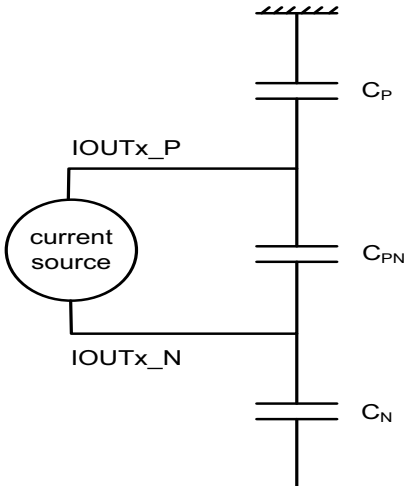


Fig 3. DAC output simplified model

10. Dynamic characteristics

Table 9. Dynamic characteristics DAC165xQ

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC1658Q High common-mode Typical values			DAC1653Q Low common-mode Typical values			Unit
			f_s	1 Gsps	1.5 Gsps	2 Gsps	1 Gsps	1.5 Gsps	2 Gsps	
SFDR	spurious-free dynamic range	interpolation x4								
		BW = f_s / 2								
		$V_{DDA(out)}$ = 3.3 V; f_o = 20 MHz								
		at −1 dBFS	C		85			88		dBc
		at −7 dBFS	C		82			82.5		dBc
		at −14 dBFS	C		76			75		dBc
		$V_{DDA(out)}$ = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	C		81			80		dBc
		at −7 dBFS	C		79			77		dBc
		at −14 dBFS	C		73			73		dBc
		$V_{DDA(out)}$ = 3.3 V; f_o = 280 MHz								
		at −1 dBFS	C		72			74		dBc
		at −7 dBFS	C		72			75		dBc
		at −14 dBFS	C		67			71.5		dBc
$SFDR_{woH2/H3}$	spurious-free dynamic range without H2 or H3	interpolation x4; BW = f_s / 2; $V_{DDA(out)}$ = 3.3 V; f_o = 150 MHz								
		at −1 dBFS	C		83.5			84.5		dBc
		at −7 dBFS	C		81			82		dBc
		at −14 dBFS	C		73			74		dBc
IMD3	third-order intermodulation distortion	$V_{DDA(out)}$ = 3.3 V; f_{o1} = 20 MHz; f_{o2} = 21 MHz; −9 dBFS per tone	C		98			94		dBc
		$V_{DDA(out)}$ = 3.3 V; f_{o1} = 210 MHz; f_{o2} = 211 MHz; −9 dBFS per tone	C		87			83		dBc
ACLR	adjacent channel power ratio	f_o = 50 MHz								
		1 WCDMA carrier; BW = 5 MHz	C		82			81		dBc
		4 WCDMA carriers; BW = 20 MHz	C		78			76		dBc

Table 9. Dynamic characteristics DAC165xQ

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

Symbol	Parameter	Conditions	Test [1]	DAC1658Q High common-mode Typical values			DAC1653Q Low common-mode Typical values			Unit
			f_s	1 Gsps	1.5 Gsps	2 Gsps	1 Gsps	1.5 Gsps	2 Gsps	
		f_o = 350 MHz								
		1 WCDMA carrier; BW = 5 MHz	C		81			80		dBc
		4 WCDMA carriers; BW = 20 MHz	C		77			75		dBc
Channel Isolation	DAC B <-> C direct crosstalk	f_o = 20 MHz	C		tbd			>95		dBc
NSD	noise spectral density	f_o = 70 MHz at −1 dBFS	C		tbd			−163		dBc/Hz

[1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used;PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

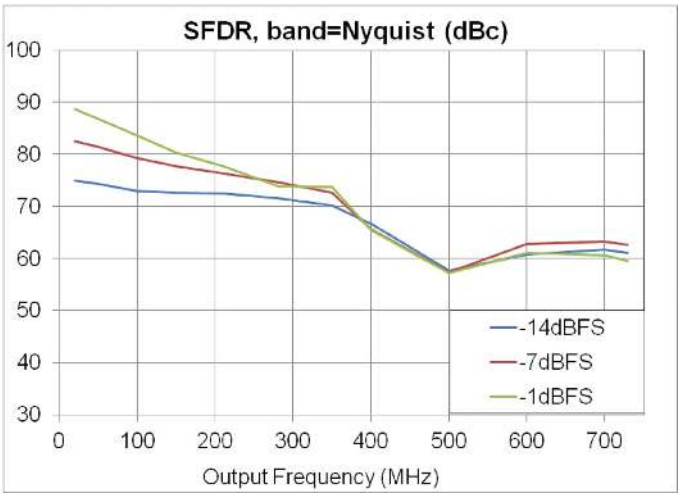


Fig 4. SFDR(dBc) over Nyquist depending on Fout (MHz) and input level (dBFS)

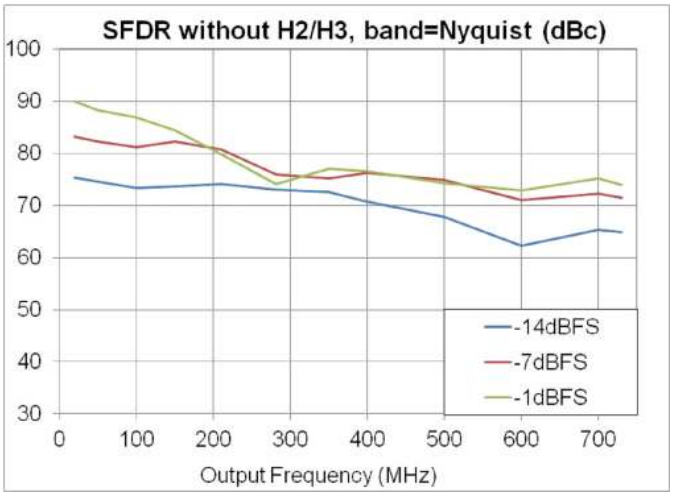


Fig 5. SFDR without H2 and H3 (dBc) over Nyquist depending on Fout (MHz) and input level (dBFS)

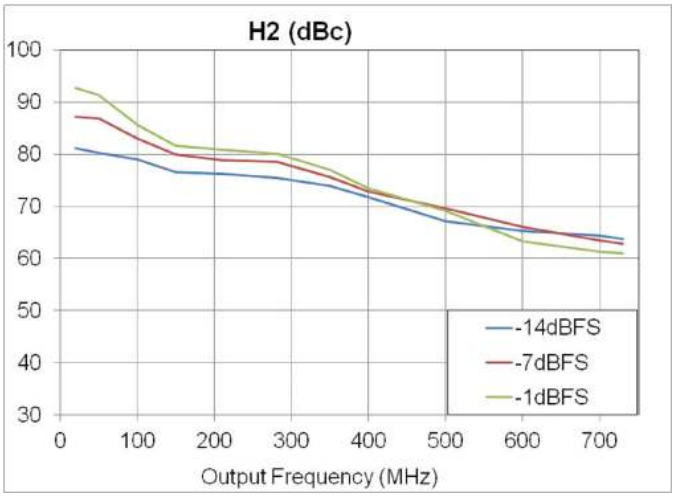


Fig 6. H2 (dBc) over Nyquist depending on Fout (MHz) and input level (dBFS)

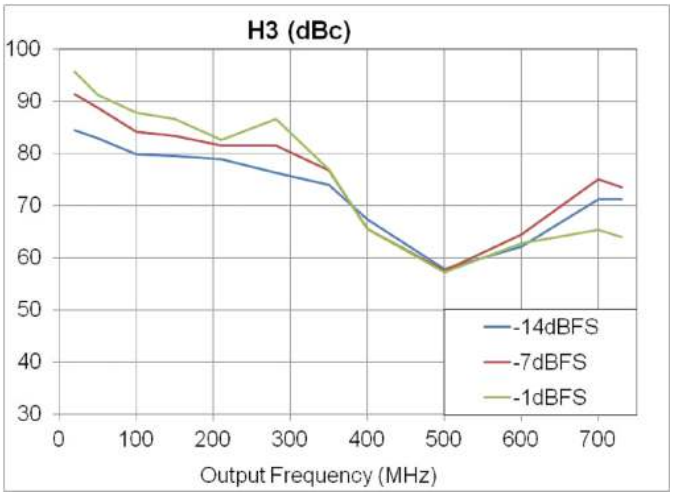


Fig 7. H3 (dBc) over Nyquist depending on Fout (MHz) and input level (dBFS)

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used;PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

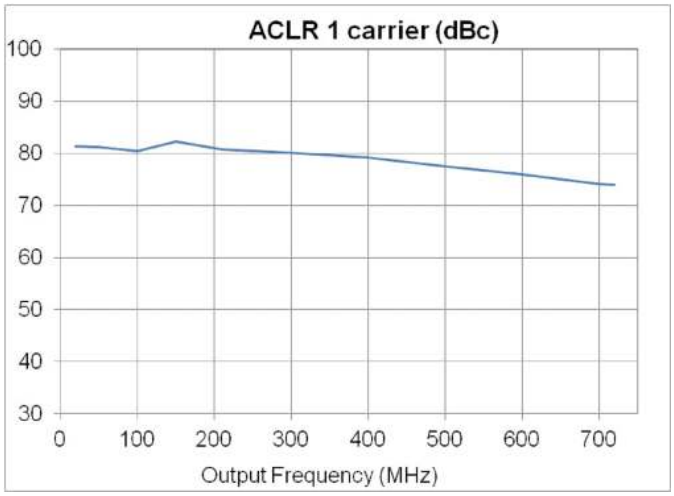


Fig 8. ACLR 1 carrier (dBc) for WCDMA depending on Fout (MHz)

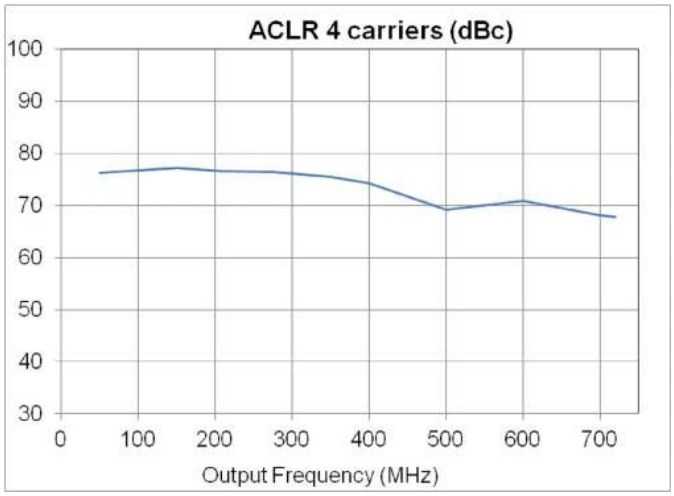


Fig 9. ACLR 4 carriers (dBc) for WCDMA depending on Fout (MHz)

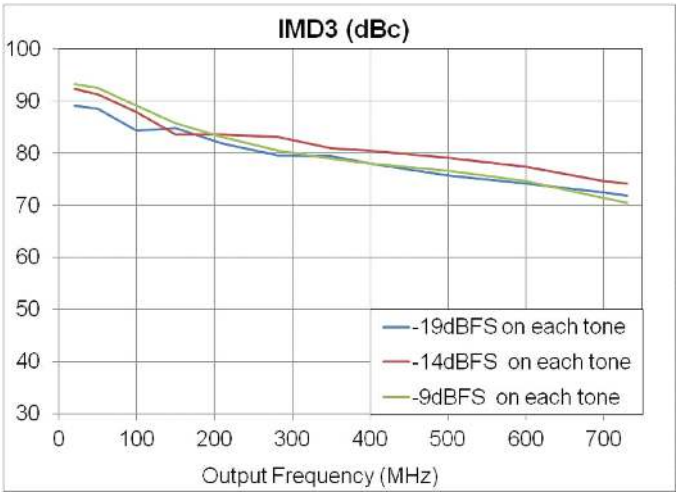


Fig 10. IMD3 (dBc) (1 MHz spacing) depending on Fout (MHz) and input level per tone (dBFS)

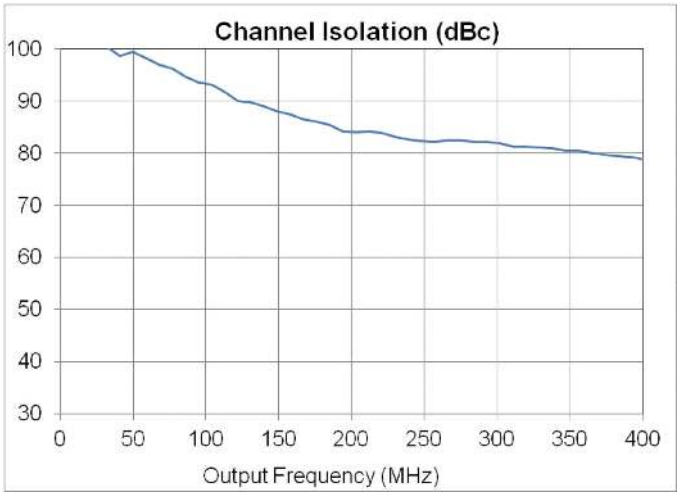


Fig 11. Channel isolation DAC B <--> DAC C direct crosstalk (dBc) depending on Fout (MHz)

VDDA(out) = 3.3 V; VDDA(1V2) = 1.2 V; VDDD(1V2) = 1.2 V; Typical values measured at Tamb = +25 °C; IO(fs) = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used; PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

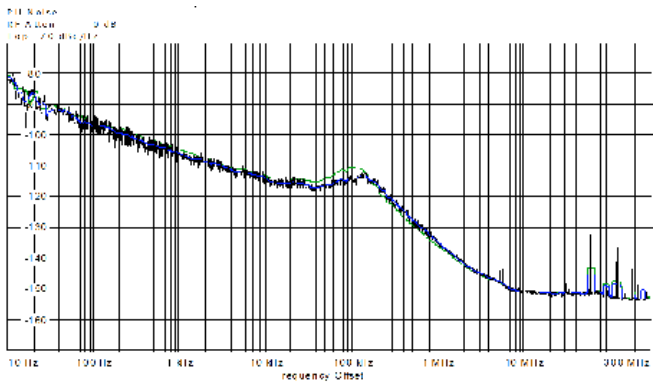


Fig 12. PLL Phase noise (dBc/Hz)

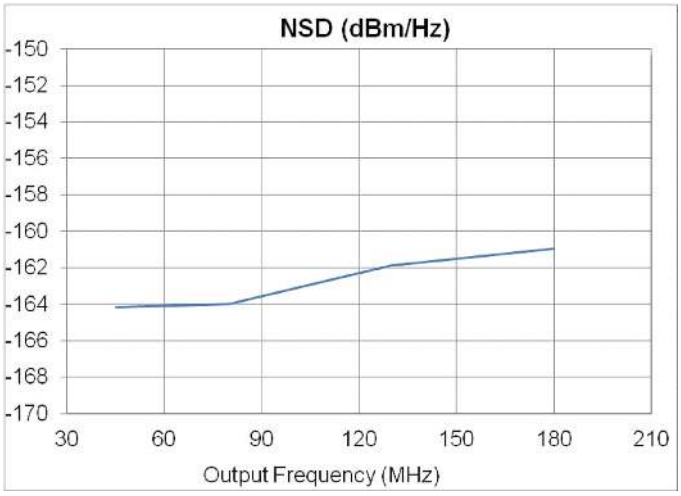


Fig 13. DAC1653Q NSD (dBm/Hz) depending on Fout (MHz) and input level per tone (dBFS)

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used;PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

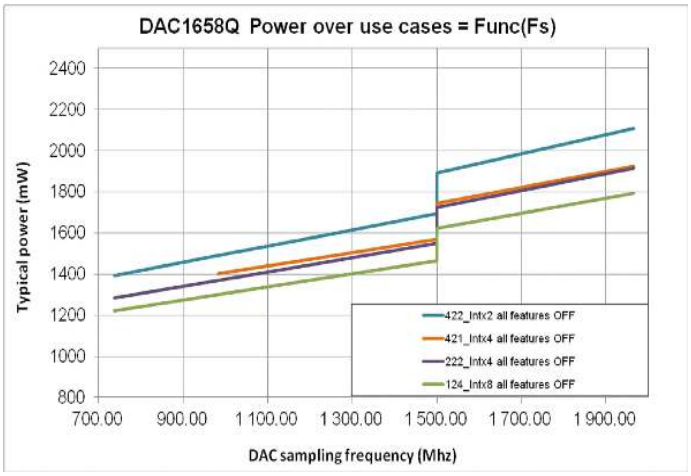


Fig 14. DAC1658Q total power dissipation (mW) depending on sampling frequency Fs (all digital feature off)

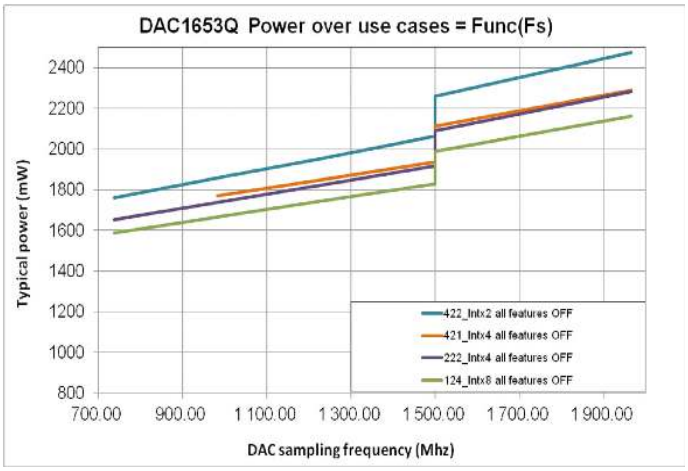


Fig 15. DAC1653Q total power dissipation (mW) depending on sampling frequency Fs (all digital feature off)

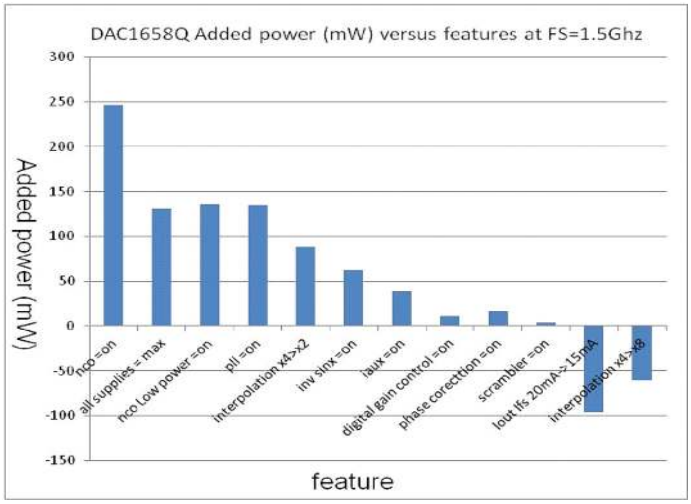


Fig 16. DAC1658Q additional power dissipation (mW) depending on added feature at Fs= 1.5 GHz

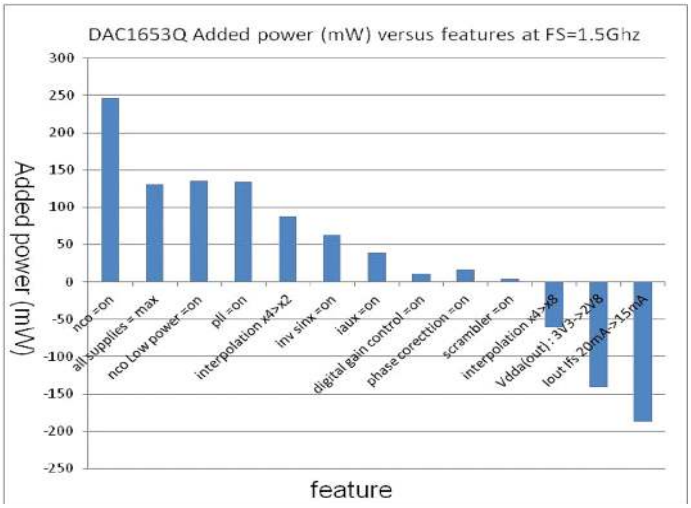


Fig 17. DAC1653Q additional power dissipation (mW) depending on added feature at Fs= 1.5 GHz

$V_{DDA(out)}$ = 3.3 V; $V_{DDA(1V2)}$ = 1.2 V; $V_{DDD(1V2)}$ = 1.2 V; Typical values measured at T_{amb} = +25 °C; $I_{O(fs)}$ = 20 mA; 1.5 Gsps sample rate used; no auxiliary DAC used;PLL off; no inverse sin(x)/x; no output correction; output signal = 1 V_{pp_diff}; output common mode voltage = 3 V (DAC1658Q) or 290 mV (DAC1653Q); unless otherwise specified.

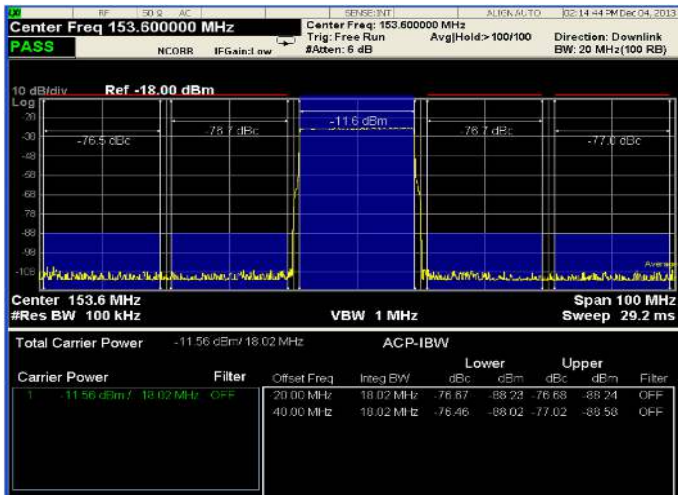


Fig 18. : ACLR of 1 carrier LTE (BW=20 MHz) centered at 153.6 MHz

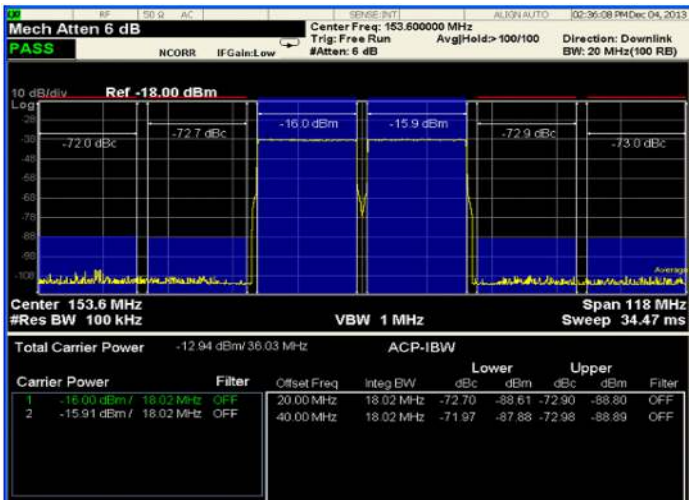


Fig 19. : ACLR of 2 carriers LTE (BW=2 x 20 MHz) centered at 153.6 MHz

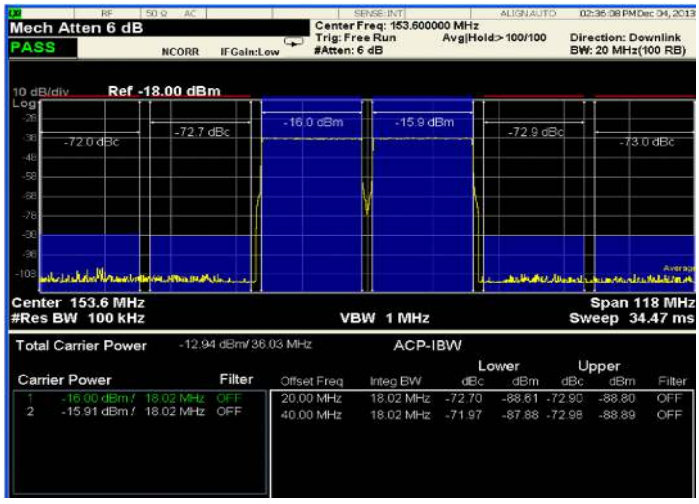


Fig 20. : ACLR of 1 carrier LTE (BW=20 MHz) centered at 350 MHz

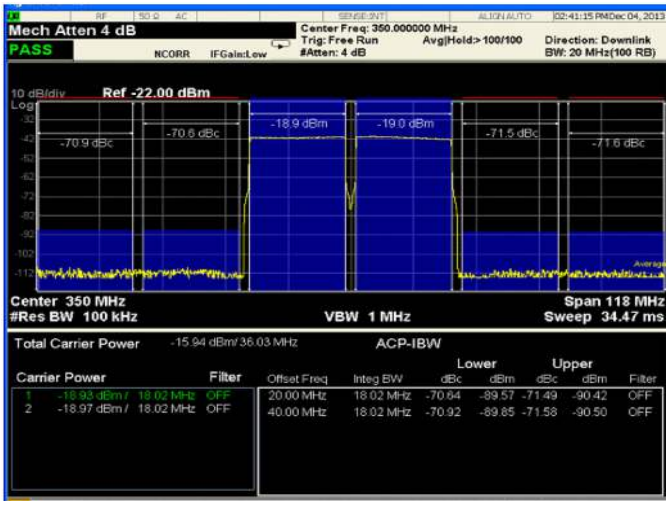


Fig 21. : ACLR of 2 carriers LTE (BW=2 x 20 MHz) centered at 350 MHz

11. Application information

11.1 General description

The DAC165xQ is a quad 16-bit DAC operating up to 2 Gsps. A maximum input data rate up to 1000 Msps is supported to enable more capability for wideband and multicarrier systems. The incorporated quadrature modulator and 40-bit Numerically Controlled Oscillators (NCOs) simplifies the frequency selection of the system. This is also possible because of the ×2, ×4 or ×8 interpolation filters which remove undesired images.

The DAC165xQ embeds four DAC channels (A, B, C and D) that can be configured as a Single Link Quad (SLQ) in which all four DACs are synchronized together or as two Dual Link Quad (DLQ) in which the two dual DACs (A/B and C/D) are synchronized independently. The two NCOs are linked to the A/B and the C/D dual DACs, respectively. Regarding the quad/dual mode used, the eight JESD204B lanes are configured as one single link configuration JESD204 link (one SYNC signal for a specified number of lanes), or dual link configuration JESD204B links (two SYNC signals associated with a specified number of lanes).

The DAC165xQ supports the following JESD204B key features:

- 10-bit/8-bit decoding
- Code group synchronization
- Initial Lane Alignment (ILA)
- $1 + x^{14} + x^{15}$ scrambling polynomial
- Character replacement
- TX/RX synchronization management via SYNC synchronization signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device (subclass 1 compatible)
- Independent Link Synchronization support
- Deterministic latency
- Multiple Device Synchronization (MDS); JESD204B subclass 1 compatible
- Harmonic clocking support
- Number L of serial lanes: 1, 2, 4 or 8 (see LMF-S configuration)
- Number M of data converters: 1,2 or 4 (see LMF-S configuration)
- Number F of octets per frame: 1, 2, 4 (see LMF-S configuration)
- Number S of samples per frame: 1, 2 (see LMF-S configuration)
- Embedded test pattern (PRBS31, PRBS23, PRBS15, PRBS7, JTSPAT, STLTP)

The DAC165xQ can be interfaced with any logic device that features high-speed SERializer/DESerializer (SERDES) functionality. This macro is now widely available in Field-Programmable Gate Array (FPGA) of different vendors. Standalone SERDES ICs can also be used.

The DAC165xQ includes polarity swapping for each of the lanes and additionally offers lane swapping to enhance the intrinsic board layout simplification of the JESD204B standard. Within each group of 4 lanes each physical lane can be configured logically as lane 0, lane 1, lane 2 or lane 3.

This device is MCDA-ML compatible, offering inter lane alignment between several devices. An IDT proprietary mechanism in combination with the JESD204B subclass I clause enables maintenance of sample alignment between devices up to the final analog output stage. Output samples are automatically aligned to the SYSREF signal generated by a dedicated IC or

by the FPGA itself. A system with several DAC165xQs can produce data with a guaranteed alignment of less than +/-1 DAC output clock period. The DAC165xQ incorporates two differential SYSREF ports (located on opposite sides of the IC) to simplify the PCB layout design. The device also enables independent link reinitialization.

The DAC165xQ generates four complementary current outputs on pins IOUTA_P/IOUTA_N and IOUTB_P/IOUTB_N, IOUTC_P/IOUTC_N, and IOUTD_P/IOUTD_N corresponding to channel 'A', 'B', 'C', and 'D', respectively, providing a nominal full-scale output current of 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

The DAC165xQ requires configuration before operating. It features an SPI slave interface to access the internal registers. Some of these registers also provide information about the JESD204B interface status. Optionally, an interrupt capability can be programmed using those registers to ensure ease of use of the device.

Because of the JESD204B standardization, the DAC165xQ does not require any adjustment from the Transmit Logic Device (TLD) to capture the input data streams. Some autolock features can be monitored using the SPI registers.

The DAC165xQ supports the following LMF configuration as described in the JESD204B standard (register XY_LMF_CNTRL (00DEh 02DEh 04DEh)):

Table 10. LMF configuration if DAC165xQ configures in dual JEDS204B links

Link configuration	L-M-F	S[1]	HD[2]
dual link (DLQ)	1-2-4	1	0
dual link (DLQ)	2-2-2	1	0
dual link (DLQ)	4-2-2	2	0
dual link (DLQ)	4-2-1	1	1
single link (SLQ)	2-4-4	2	0
single link (SLQ)	4-4-2	2	0
single link (SLQ)	8-4-2	4	0
single link (SLQ)	8-4-1	2	1

[1] S is the number of samples per frame.

[2] HD is the high-density bit as described in the JESD204B specification.

A new IDT auto-mute feature enables switching off of the RF output signal as a result of various internal events occurring.

A signal level detector allows auto-muting of the DAC outputs if they exceed the detection limit.

The DAC165xQ requires 3.3 V and 1.2 V power supplies. The 1.2 V supply has separate digital and analog power supply pins.

In order to program the device in LMF841 (SLQ) configuration, each DAC AB and DAC CD instance of XY_LMF_CNTRL registers will have to be programmed in LMF421. In parallel, SLQ configuration (common ILA, common sync) must also be selected. Same apply, in order to get SLQ LMF842/LMF442/LMF244 configuration, LMF422/LMF222/LMF124 will have to be programmed for each dual DAC.

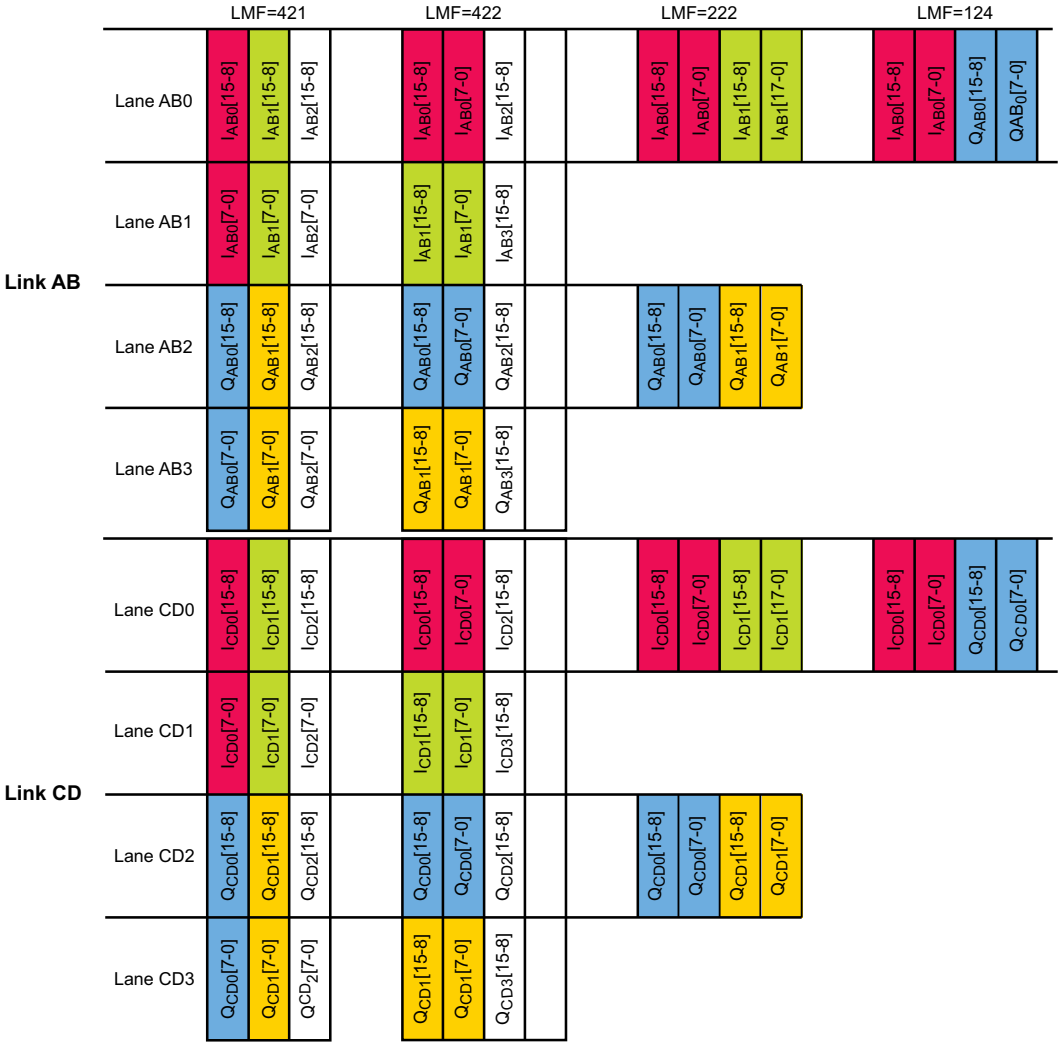


Fig 22. Frame assembly byte representation

11.2 Device operation

The DAC165xQ provides a lot of flexibility in its way of working through its SPI registers. The SPI registers are divided in blocks of registers. Each block is associated with some global functions which are described below. Section 11.13 shows an overview of all register blocks, including the register descriptions.

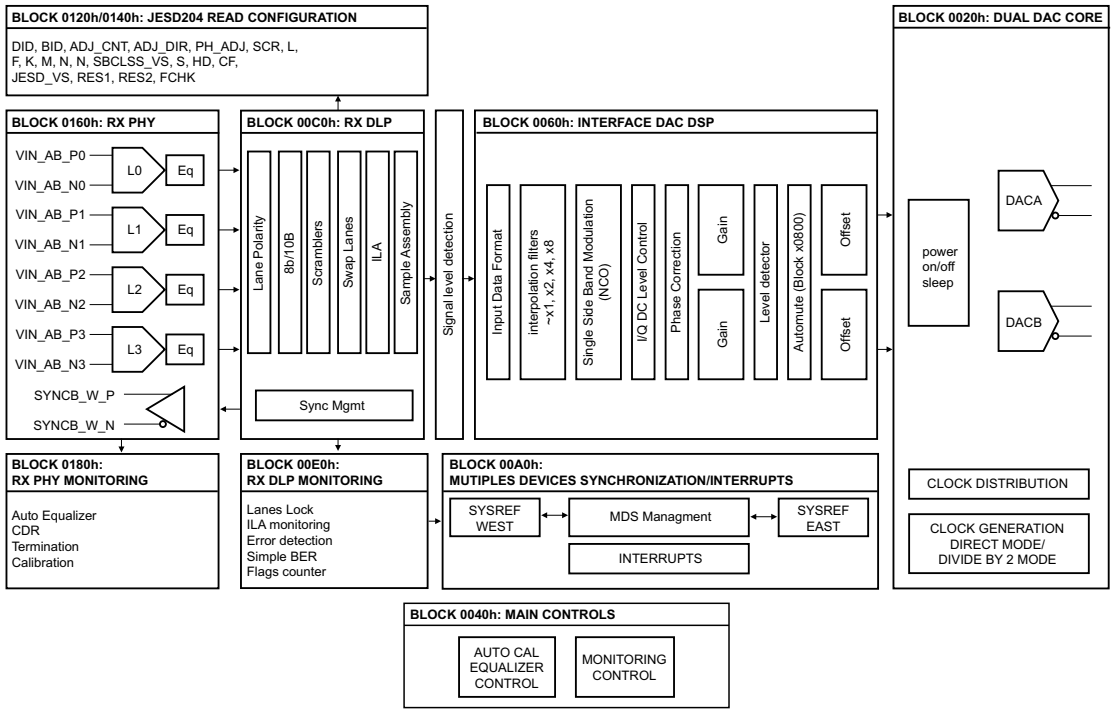


Fig 23. SPI register blocks partition: DAC A/B

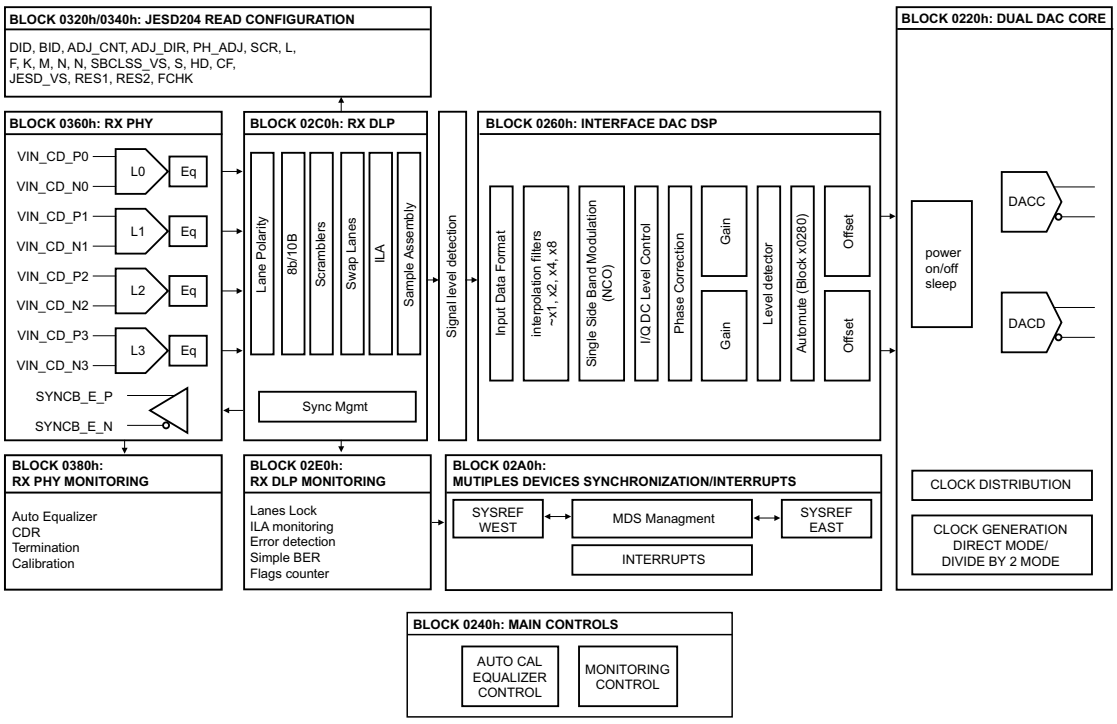


Fig 24. SPI register blocks partition: DAC C/D

11.2.1 SPI configuration block

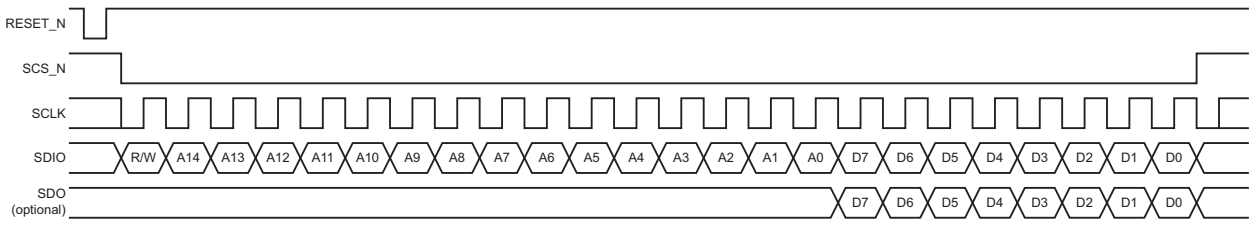
This block of registers specifies how the SPI controller and the identification of the chip work.

11.2.1.1 Protocol description

The DAC165xQ serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both Write mode and Read mode. The reference voltage of the interface is $V_{DDD(IO)}$. Depending on the power supply level of the SPI master device, it can be set from1.2 V to1.8 V.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pins, input and output ports, respectively). In both configurations, SCLK acts as the serial clock and SCS_N acts as the serial chip select.

The DAC165xQ SPI-interface is a slave-device. Multiple slave-device can be attached to the same master interface as long as each device has its own serial chip select signal (SCS_N).



R/W indicates the mode access.

The RESET_N signal is not linked to the SPI interface but enable the reset of the registers to the default values.

Fig 25. SPI protocol

Table 11. Read mode or Write mode access description

R/W	Description
0	Write mode operation
1	Read mode operation

A[14:0] indicates which register is being addressed. If a multiple transfer occurs, this address points to the first register to be accessed.

11.2.1.2 SPI controller configuration

The 3-wire or 4-wire mode is set by bit SPI_4W of register SPI_CONFIG_A (0000h). The default mode is 3-wire mode.

A software SPI reset can be called via bit SPI_RST (0000h). This reset reinitializes all SPI registers, except register SPI_CONFIG_A and SPI_CONFIG_B, to their default settings. Only a hardware reset on pin RESET_N can reset to their default values. Reset the device to its default value at start-up time to avoid any uncontrolled states.

The SPI streaming mode is enabled by default. In this mode, the Read or Write process carries on as long as the SCS_N signal is low. The streaming mode requires a first address 'n' to be set at the beginning of the SPI sequence. The following data are associated from this address in an ascending (auto-increment) or descending (auto-decrement) mode. This ascending/descending mode is specified by bit SPI_ASCEND (0000h). Figures below represent the readback of 2 bytes data in a 3 wires mode for the ascendant and descendant mode.

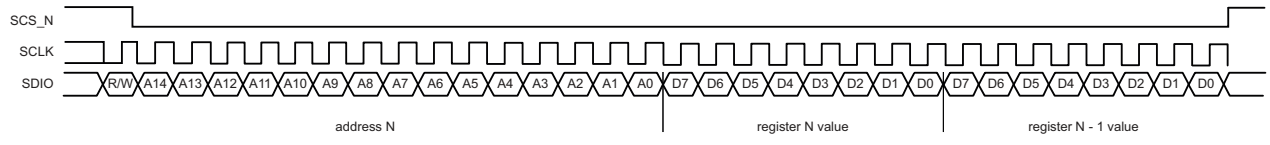


Fig 26. Consecutive 2-byte data readback under descending address

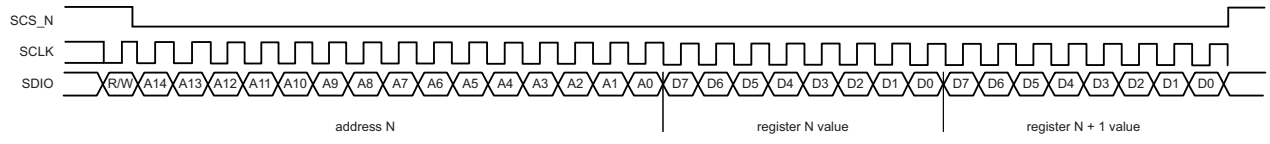


Fig 27. Consecutive 2-byte data readback under ascending address

The streaming mode can be disabled by setting bit SPI_SINGLE (0001h). In this single-byte mode, only 1 byte of data can be written or read, whatever the state of the SCS_N signal.

11.2.1.3 SPI register map

The DAC165xQ includes two dual DAC core. In order to ease access to each dual DAC of the device, the register map implementation enables to either access DAC AB , DAC CD or both using a single write:

- Adress from 040h to 1FFh is reserved for dual DAC AB.
- Adress from 240h to 3FFh is reserved for dual DAC CD.
- Adress from 440h to 5FFh is reserved for dual write access to both DAC AB and DAC CD (only write access possible).
- Adress from 00h to 03F is reserved for common device register.

DAC AB register are ordered in same way than DAC CD register. So if a function for DAC AB is available at address n, the same function is available at address n+ 200h for DAC CD. writing to address n+400h enables to simultaneously set this function for both dual DAC.

11.2.1.4 Double buffering and Transfer mode

Some register functions (like the NCO frequency value) are split over multiple registers. If this is the case, the first address consists of the LSB byte and the highest address in the MSB byte. When programming these registers sequentially, some unexpected behavior can occur at the DAC output. It is preferable to program this set of registers simultaneously. A double buffering feature is available on some registers allowing sequential programming of the first buffers and transferring the values to the final register simultaneously.

The transfer request is done by setting the TRANSFER_BIT bit of register SPI_CONFIG_C register (000Fh). The device clears this bit (autoclear) indicating to the SPI master device that the transfer is complete.

The SPI_READBUF bit (0001h) allows the reading back of the first stage of buffers (in case the register is double buffered).

The following registers are double buffered:

Table 12. Double buffered registers
See *Table 68*

Address	Register
0062h 0262h 0462h	XY_PHINCO_LSB
0063h 0263h 0463h	XY_PHINCO_MSB
0064h 0264h 0464h	XY_FREQNCO_B0
0065h 0265h 0465h	XY_FREQNCO_B1
0066h 0266h 0466h	XY_FREQNCO_B2
0067h 0267h 0467h	XY_FREQNCO_B3
0068h 0268h 0468h	XY_FREQNCO_B4
0069h 0269h 0469h	XY_PHASECORR_CNTRL0
006Ah 026Ah 046Ah	XY_PHASECORR_CNTRL1
006Bh 026Bh 046Bh	XY_DSP_X_GAIN_LSB
006Ch 026Ch 046Ch	XY_DSP_X_GAIN_MSB
006Dh 026Dh 046Dh	XY_DSP_Y_GAIN_LSB
006Eh 026Eh 046Eh	XY_DSP_Y_GAIN_MSB
006Fh 026Fh 046Fh	XY_DSP_OUT_CNTRL
0070h 0270h 0470h	XY_DSP_CLIPLEV
0071h 0271h 0471h	XY_DSP_X_OFFSET_LSB
0072h 0272h 0472h	XY_DSP_X_OFFSET_MSB
0073h 0273h 0473h	XY_DSP_Y_OFFSET_LSB

Table 12. Double buffered registers
See *Table 68*

Address	Register
0074h 0274h 0474h	XY_DSP_Y_OFFSET_MSB
0075h 0275h 0475h	XY_IQ_LEV_CNTRL
0076h 0276h 0476h	XY_I_DC_LEVEL_LSB
0077h 0277h 0477h	XY_I_DC_LEVEL_MSB
0078h 0278h 0478h	XY_Q_DC_LEVEL_LSB
0079h 0279h 0479h	XY_Q_DC_LEVEL_MSB
007Ah 027Ah 047Ah	XY_SPD_CNTRL
007Bh 027Bh 047Bh	XY_SPD_THRESHOLD_LSB
007Ch 027Ch 047Ch	XY_SPD_THRESHOLD_MSB

11.2.1.5 Device description

Registers CHIP_TYPE, CHIP_ID_0, CHIP_ID_1 and CHIP_VERSION (0003h, 0004h, 0005h or 0006h) represent the ID card of the device.

Registers VENDOR_ID_LSB and VENDOR_ID_MSB (000Ch, 000Dh) represent the IDT manufacturer identifier.

11.2.1.6 SPI timing description - 4 wires mode

The SPI interface can operate at a frequency of up to 25 MHz. Figure 28 and Figure 29 show the SPI timing in 4 wires mode.

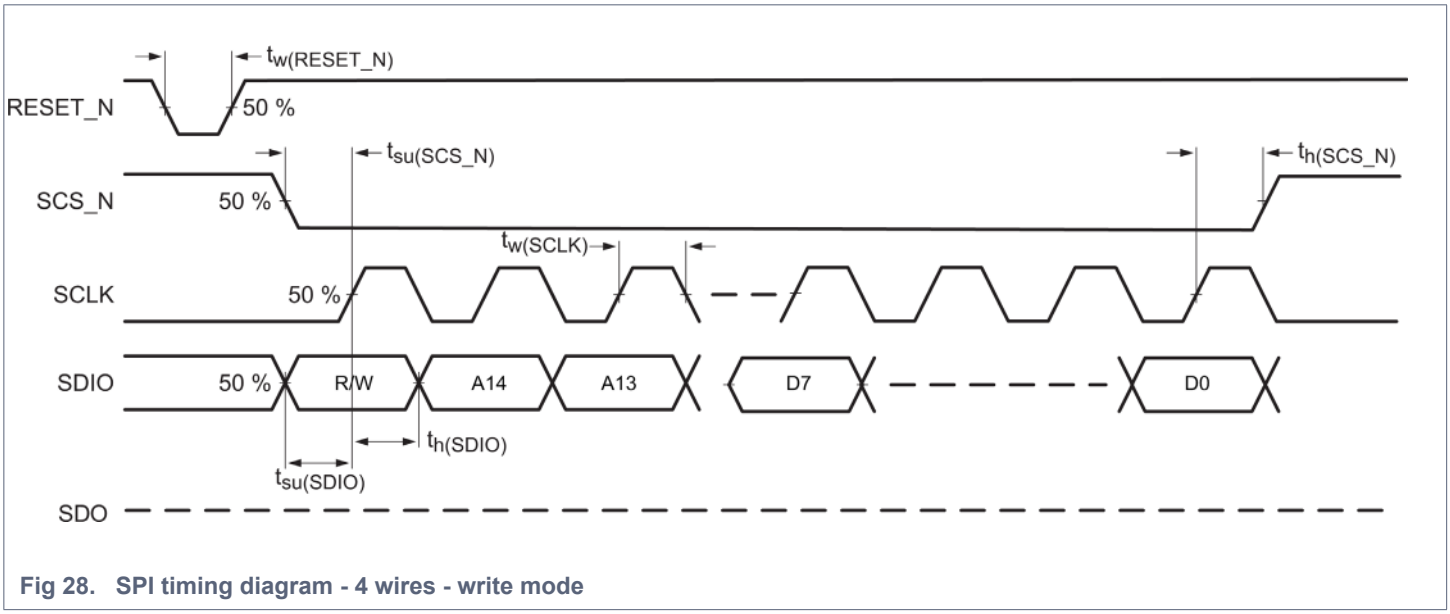


Fig 28. SPI timing diagram - 4 wires - write mode

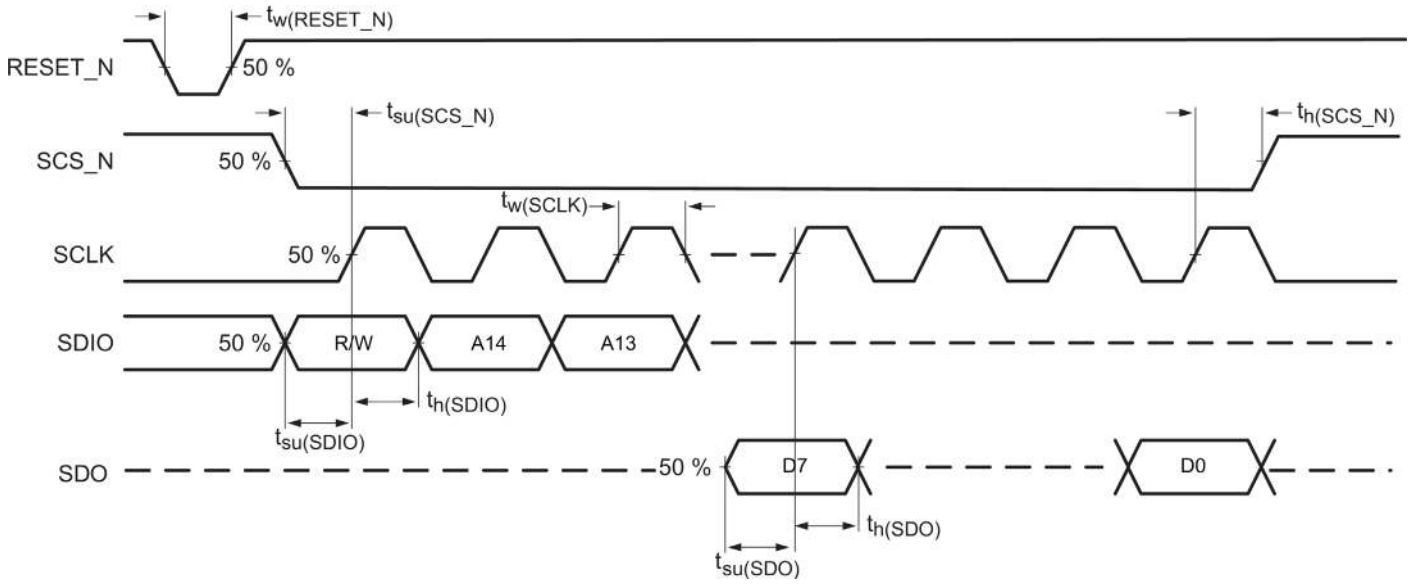


Fig 29. SPI timing diagram - 4 wires - read mode

The SPI timing characteristics are given in Table 13.

Table 13. SPI timing characteristics - 4 wires

Symbol	Parameter		Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency					
	$V_{DDD(IO)}$=1.8V		-	-	25	MHz
	$V_{DDD(IO)}$=1.2V		-	-	20	MHz
$t_{w(SCLK)}$	SCLK pulse width (high)		20	-	-	ns
	SCLK pulse width (low)		depends of propagation time and master timing requirements			
$t_{su(SCS\_N)}$	SCS_N set-up time		5	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time		20	-	-	ns
$t_{su(SDIO)}$	SDIO set-up time		5	-	-	ns
$t_{h(SDIO)}$	SDIO hold time		5	-	-	ns
$t_{su(SDO)}$	SDO set-up time		5	-	-	ns
$t_{h(SDO)}$	SDO hold time		5	-	-	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	[1]	30	-	-	ns

[1] The RESET_N signal is asynchronous to the SPI interface, but enables the reset of the registers to the default values.

11.2.1.7 SPI timing description - 3 wires mode

The SPI interface can operate at a frequency of up to 15 MHz. Figure 30 and Figure 31 show the SPI timing in 3 wires mode.

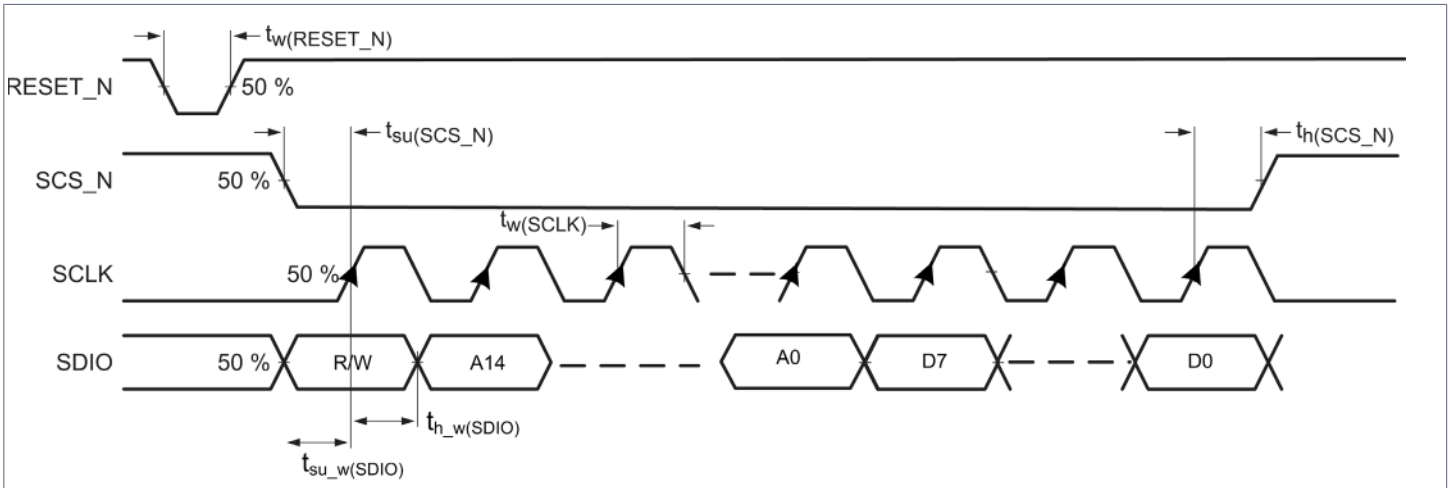


Fig 30. SPI timing diagram - 3 wires - write mode

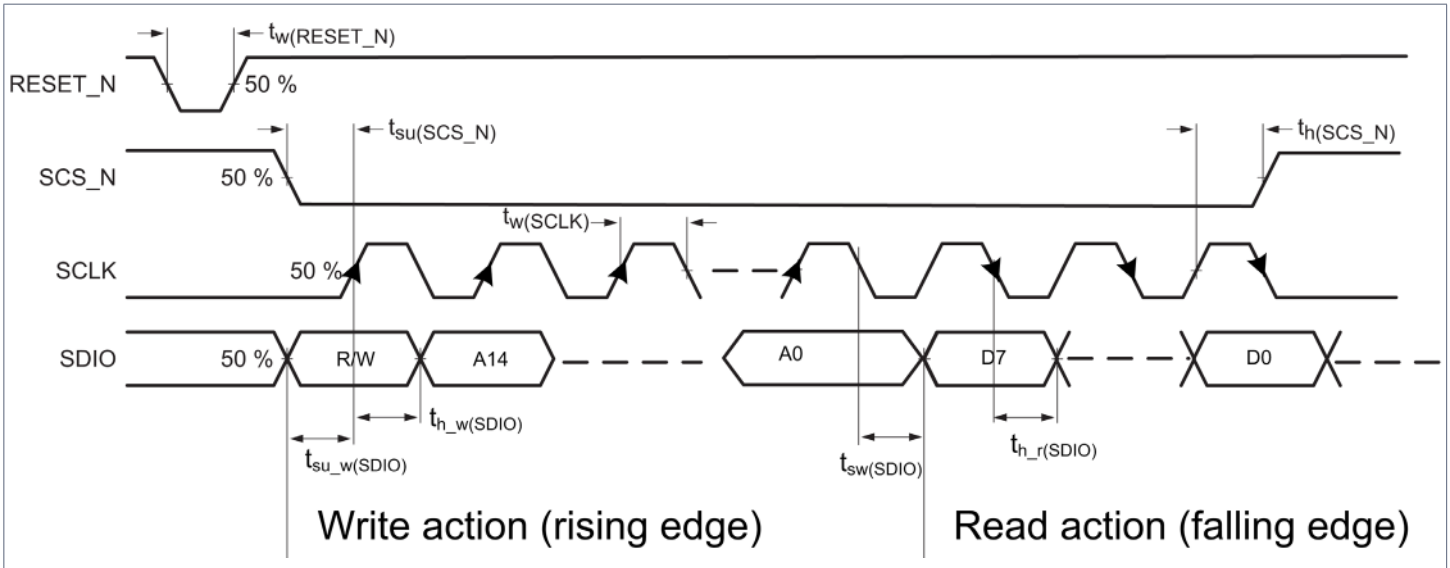


Fig 31. SPI timing diagram - 3 wires - read mode

The SPI timing characteristics are given in Table 14.

Table 14. SPI timing characteristics - 3 wires

Symbol	Parameter	Min	Typ	Max	Unit
f_{SCLK}	SCLK frequency	-	-	15	MHz
$t_{w(SCLK)}$	SCLK pulse width (high)	30	-	-	ns
	SCLK pulse width (low)	depends of propagation time and master timing requirements			
$t_{su(SCS\_N)}$	SCS_N set-up time	5	-	-	ns
$t_{h(SCS\_N)}$	SCS_N hold time	20	-	-	ns

Table 14. SPI timing characteristics - 3 wires

Symbol	Parameter		Min	Typ	Max	Unit
$t_{su\_w(SDIO)}$	SDIO set-up time		5	-	-	ns
$t_{h\_w(SDIO)}$	SDIO hold time		5	-	-	ns
$t_{sw(SDIO)}$	SDIO switch time (write to read mode)					
	$V_{DDD(IO)}$=1.8V		9	-	20	ns
	$V_{DDD(IO)}$=1.2V		9	-	25	ns
$t_{h\_r(SDIO)}$	SDO hold time (read mode)					
	$V_{DDD(IO)}$=1.8V		6	-	20	ns
	$V_{DDD(IO)}$=1.2V		6	-	25	ns
$t_{w(RESET\_N)}$	RESET_N pulse width	[1]	30	-	-	ns

[1] The RESET_N signal is asynchronous to the SPI interface, but enables the reset of the registers to the default values.

11.2.2 Power up sequence

There are four steps for the power-on sequence (see Figure 32):

1. all supplies and clock are switched on. at Ton time (see Figure 32), all DAC165xQ supplies have reached their specification ranges and the device clock CLKIN is up and running.
2. Then a wait duration of 1 µs is needed before releasing the RESET_N pin.
3. Then a wait duration of 40k periods of device clock CLKIN is needed before sending the first SPI device configuration command. So for example a 40µsec wait period is needed when Fclkin= 1 GHz.
4. At start-up, the three clocks WCLK, DCLK and PCLK are forced to reset states to avoid that the DAC outputs any dummy signal through bits FORCE_RESET_WCLK, FORCE_RESET_DCLK and FORCE_RESET_PCLK of the MAINCONTROL register (0020h). The PCLK clock are only used in case of the PLL usage. Refers to the PLL configuration section to know how to program it correctly. The default mode described in following section is when the Device clock is used as sampling clock (DAC PLL OFF). In this case the bit FORCE_RESET_PCLK is kept enabled.

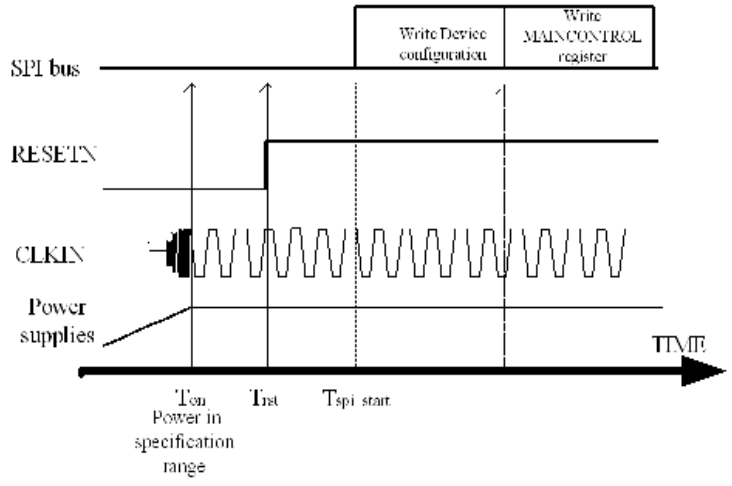


Fig 32. power up sequence

11.2.3 Main device configuration and SPI Start-up Sequence

The registers of block MAIN are used for the main configuration of the DAC165xQ.

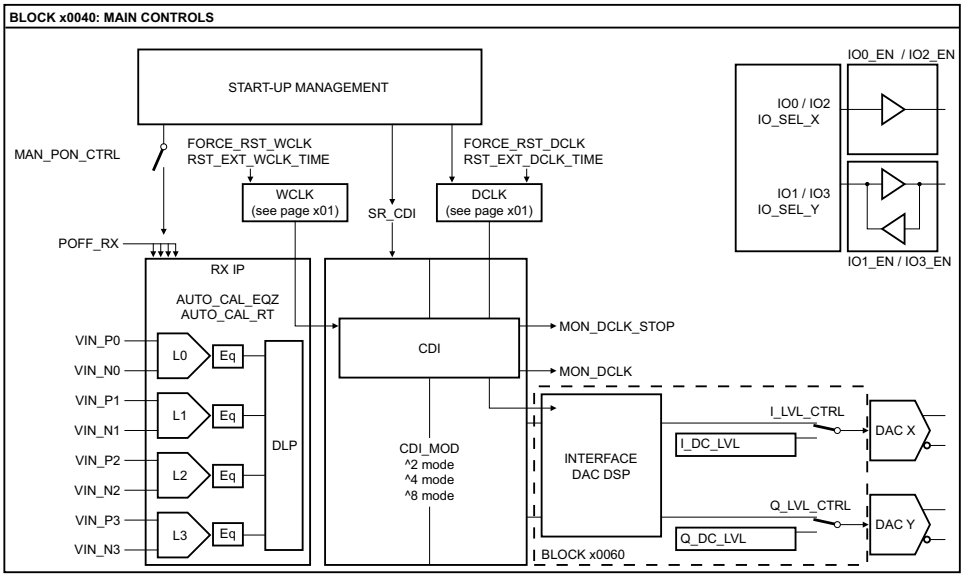


Fig 33. Main Controls

Here are some guidelines to ensure basic correct SPI programming. As DCLK and WCLK are kept to reset, the programming sequence of the registers is not important after the reset:

1. Put PLL in low power mode (needed only if PLL is not used).
2. Proceed to a software reset of all SPI registers (see Section 11.2.1.2)
3. Disable Pin RF_ENABLE Power Down mode (optional)
4. Specify the Clock Domain Interface (CDI) mode (Section 11.2.7.1 and Table 26) and the Interpolation mode (see Table 16) and/or SSBM mode (see Table 18)
5. Set the SYNCB pin control, output common mode level and swing (see Section 11.9.5.5)
6. enable JESD204B HF_REF module.
7. Specify the Clocks configuration (see Section 11.2.7.1):
   a. Divider bypass or Divider mode
   b. WCLK division ratio
8. Specify the JESD204B LMF configuration (see Section 11.9.5.10)
9. Specify the JESD204B logical lanes order (see Section 11.9.5.3) and polarity
10. Specify which JESD204B physical lanes have to be turned off using the POFF_RX bits of register POFF
11. Define JESD204B ILA control and scrambling.
12. Define Mute control option.
13. Release the WCLK and DCLK reset by de-asserting the bits FORCE_RESET_DCLK and FORCE_RESET_WCLK of the MAINCONTROL register (0020h)

Remark: All the Double Buffering registers programmed before the DCLK reset release are transfered automatically after the DCLK reset release. After this reset release, these registers need the TRANSFER_BIT to be active.

11.2.3.1 SPI start-up sequence example

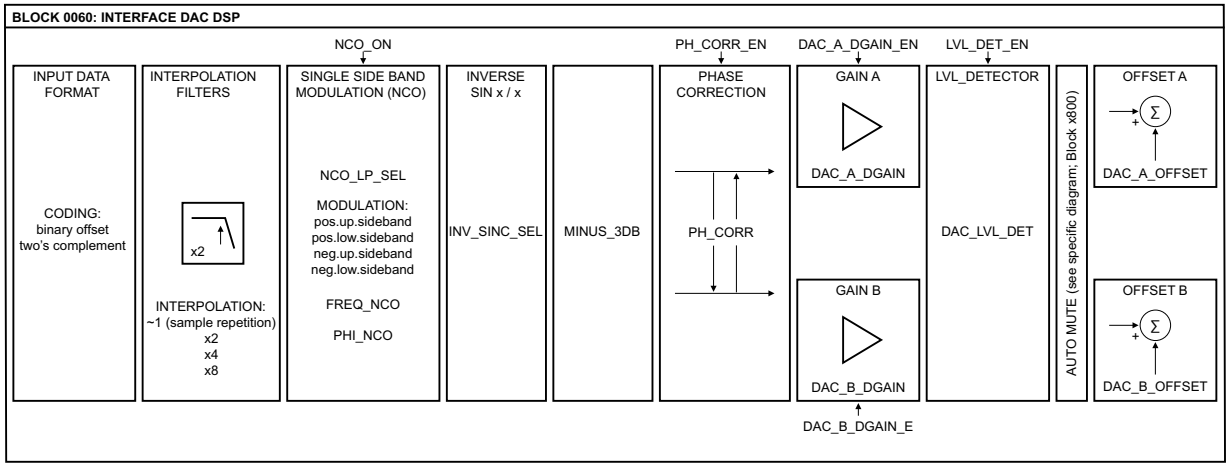
The following SPI sequence shows the list of commands to be used to start the DAC165xQ in DLQ (Dual link Quad) configuration, LMF222 with interpolation ×4 mode with NCO off, PLL bypass mode, and without inverse (sin x) / x. Other start-up sequences can be easily derived from this sequence:

Table 15. SPI start-up sequence

Step	SPI (address, data)	Comment
1	Write(0x0000, 0x99)	Mandatory: sequence needed to put the PLL in real low power mode
	Write(0x0020, 0x01)	
	Write(0x0029, 0x43)	
	Write(0x01C8, 0x0F)	
	Write(0x01CA, 0x9C)	
	Write(0x01C0, 0x02)	
	Write(0x01C4, 0x0F)	
	Write(0x01C6, 0x91)	
	Write(0x01C6, 0x90)	
2	Write(0x0000, 0x99)	Mandatory: configure SPI in 3 or 4 wires and proceed to soft reset
3	Write(0x002A, 0x00)	Optional: disable pin RF_ENABLE power down
4	Write(0x002B, 0x11)	Mandatory: specify CDI mode and interpolation
	Write(0x0460, 0x02)	Mandatory: NCO control , inv sinx/x control , interpolation control
5	Write(0x002C, 0x10)	Mandatory: define the JESD204B SYNCB_E and SYNCB_W signal control
	Write(0x57D, 0xC4)	Optional: define sync level
6	Write(0x0560, 0x03)	Mandatory: enable JESD204B Rx_Phy HS_REF
7	Write(0x01AD, 0x02)	Mandatory: specify DACCLK / WCLK ratio : WCLK div = M/(L*Inter) = 2/4*4 = 1/4)
8	Write(0x04DE, 0x52)	Mandatory: specify the JESD204B LMF configuration (LMF=222)
9	Write(0x00CE, 0xD2)	Optional: specify the JESD204B logical lanes order (reswap lanes ab (3 0 2 1))
	Write(0x02CE, 0x1B)	Optional: specify the JESD204B logical lanes order (reswap lanes cd (0 1 2 3))
	Write(0x04CD, 0x0F)	Optional: specify the JESD204B physical lanes polarity
10	Write(0x0022, 0x59)	Mandatory: Specify which JESD204B physical lanes have to be turned off using the POFF_RX bits
11	Write(0x04C7, 0x62)	Mandatory: define the JESD204B ILA control
12	Write(0x0480, 0x00)	Optional: specify the MUTE options (disable)
13	Write(0x0020, 0x24)	Mandatory: define re-init mode and release the WCLK and DCLK resets

11.2.4 Interface DAC DSP block

This module is the interface between the data processing in the high-speed serial receiver and each of the dual DAC core. The controls of the Digital Signal Processing (DSP) of the DAC are specified to set up the interpolation filter, and enable or disable the various gains and offsets of the data digital path. The data signals have already been processed by the Digital Lane Processing (DLP, see Section 11.9.3). They are provided to this module through the Clock Domain Interface (Section 11.2.7.1). This module is clocked by the digital clock DCLK.



Block 0060h = DAC A/B

Block 0260h = DAC C/D

Block 0460h = All DACs

Fig 34. Interface DAC DSP overview

11.2.4.1 Input data format

After decoding in the high-speed serial receiver, the data representation can be specified as binary offset coding or as two's complement coding using register XY_DATA_FORMAT (0075h 0275h 0475h).

11.2.4.2 Finite Impulse Response (FIR) filters

The DAC165xQ provides three interpolation filters described by their coefficients in Table 17. The three interpolation FIR filters have a stop band attenuation of at least 80 dBc and a pass band ripple of less than 0.0005 dB.

The interpolation ratio can be set through register XY_TXCFG (0060h 0260h 0460h).

Table 16. Interpolation

Symbol	Access	Value	Description
XY_INT_FIR[1:0]	R/W		interpolation
		00	no interpolation/~×1 interpolation
		01	×2 interpolation
		10	×4 interpolation
		11	×8 interpolation

The 'no interpolation' or '~×1' (quasi ×1) mode is in fact a degenerated ×2 interpolation mode where the samples are repeated twice.

Remark: The XY_INT_FIR[1:0] setting must be coupled with the DCLK and WCLK clock configurations and with CDI mode (see Section 11.2.7.1).

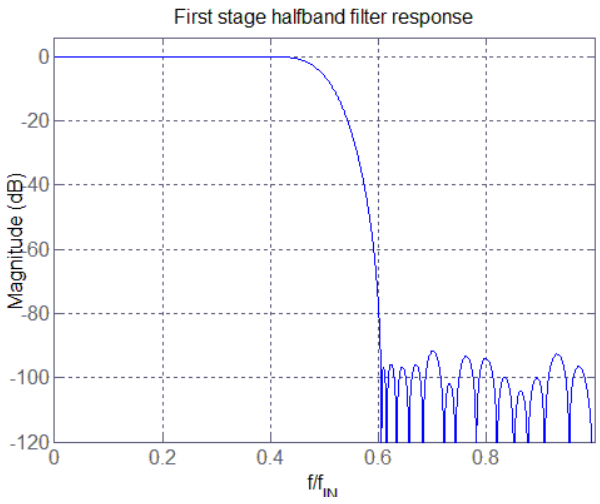


Fig 35. First stage half-band filter response (used in ×2, ×4, and ×8 interpolation)

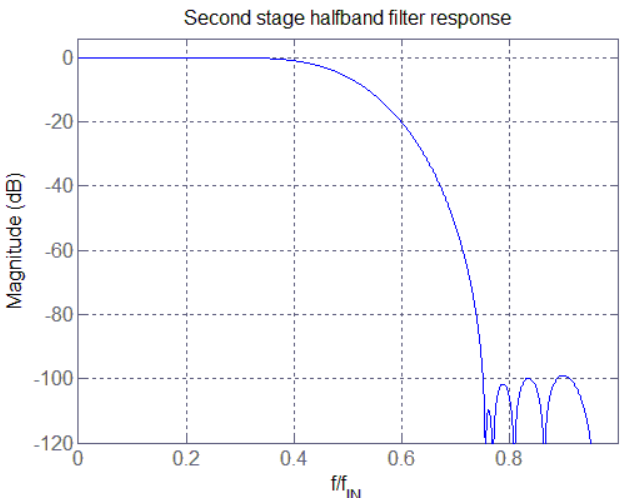


Fig 36. Second stage half-band filter response (used in ×4, and ×8 interpolation)

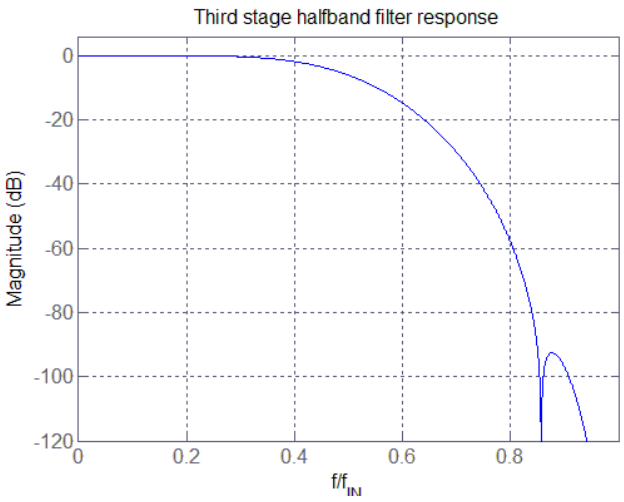


Fig 37. Third stage half-band filter response (used in ×8 interpolation)

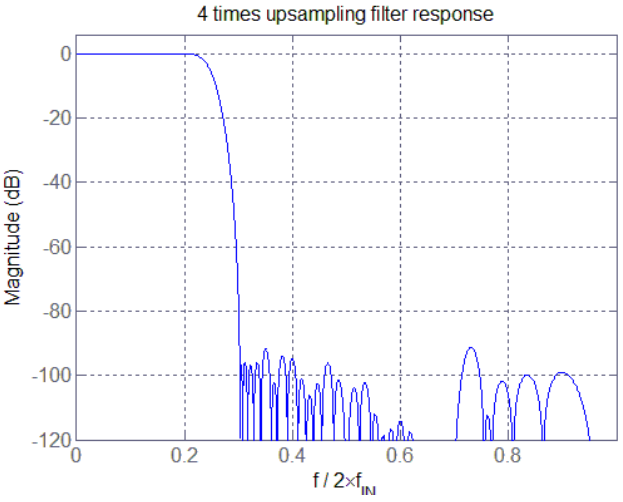


Fig 38. ×4 interpolation cumulated filter response

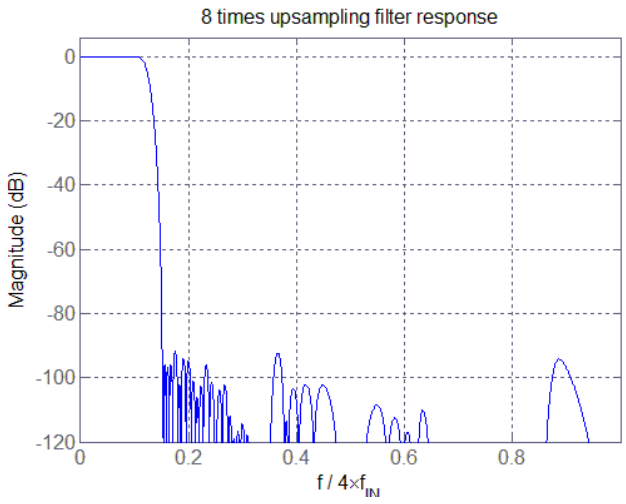


Fig 39. ×8 interpolation cumulated filter response

Table 17: Interpolation filter coefficients

First interpolation filter			Second interpolation filter			Third interpolation filter		
Lower	Upper	Value	Lower	Upper	Value	Lower	Upper	Value
-	H(27)	+65536	H(11)	-	+32768	H(7)	-	+1024
H(26)	H(28)	+41501	H(10)	H(12)	+20272	H(6)	H(8)	+615
H(25)	H(29)	0	H(9)	H(13)	0	H(5)	H(9)	0
H(24)	H(30)	−13258	H(8)	H(14)	−5358	H(4)	H(10)	−127
H(23)	H(31)	0	H(7)	H(15)	0	H(3)	H(11)	0
H(22)	H(32)	+7302	H(6)	H(16)	+1986	H(2)	H(12)	+27
H(21)	H(33)	0	H(5)	H(17)	0	H(1)	H(13)	0
H(20)	H(34)	−4580	H(4)	H(18)	−654	H(0)	H(14)	−3
H(19)	H(35)	0	H(3)	H(19)	0	-	-	-
H(18)	H(36)	+2987	H(2)	H(20)	+159	-	-	-
H(17)	H(37)	0	H(1)	H(21)	0	-	-	-
H(16)	H(38)	−1951	H(0)	H(22)	−21	-	-	-
H(15)	H(39)	0	-	-	-	-	-	-
H(14)	H(40)	+1250	-	-	-	-	-	-
H(13)	H(41)	0	-	-	-	-	-	-
H(12)	H(42)	-773	-	-	-	-	-	-
H(11)	H(43)	0	-	-	-	-	-	-
H(10)	H(44)	+456	-	-	-	-	-	-
H(9)	H(45)	0	-	-	-	-	-	-
H(8)	H(46)	−252	-	-	-	-	-	-
H(7)	H(47)	0	-	-	-	-	-	-
H(6)	H(48)	+128	-	-	-	-	-	-
H(5)	H(49)	0	-	-	-	-	-	-
H(4)	H(50)	−58	-	-	-	-	-	-
H(3)	H(51)	0	-	-	-	-	-	-
H(2)	H(52)	+22	-	-	-	-	-	-
H(1)	H(53)	0	-	-	-	-	-	-
H(0)	H(54)	−6	-	-	-	-	-	-

11.2.4.3 Single Side Band Modulator (SSBM)

The single side band modulator is a quadrature modulator that enables the mixing of the XY_I data and XY_Q data with the sine and cosine signals generated by the NCO to generate path X and Y as described in Figure 40.

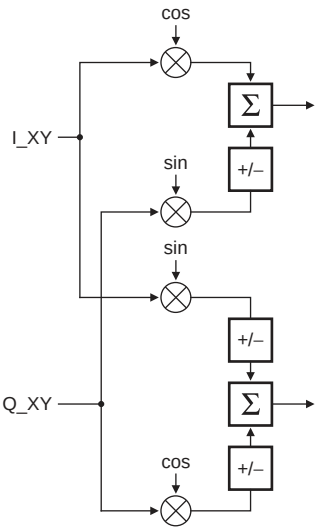


Fig 40. Single sideband modulator principle

Table 18 shows the various possibilities set by register XY_MODE[2:0] (0060h 0260h 0460h).

Table 18. Complex modulator operation mode

XY_MODE[2:0]	Mode	Path A / Path C	Path B / Path D
000	bypass	$I(t)$	$Q(t)$
001	positive upper sideband	$I(t) \times cos(\omega_{NCO} \times t) - Q(t) \times sin(\omega_{NCO} \times t)$	$I(t) \times sin(\omega_{NCO} \times t) + Q(t) \times cos(\omega_{NCO} \times t)$
010	positive lower sideband	$I(t) \times cos(\omega_{NCO} \times t) + Q(t) \times sin(\omega_{NCO} \times t)$	$I(t) \times sin(\omega_{NCO} \times t) - Q(t) \times cos(\omega_{NCO} \times t)$
011	negative upper sideband	$I(t) \times cos(\omega_{NCO} \times t) - Q(t) \times sin(\omega_{NCO} \times t)$	$-I(t) \times sin(\omega_{NCO} \times t) - Q(t) \times cos(\omega_{NCO} \times t)$
100	negative lower sideband	$I(t) \times cos(\omega_{NCO} \times t) + Q(t) \times sin(\omega_{NCO} \times t)$	$-I(t) \times sin(\omega_{NCO} \times t) + Q(t) \times cos(\omega_{NCO} \times t)$
others	not defined	-	-

The effect of the XY_MODE[2:0] parameter is better viewed after mixing the X and Y signal with a LO frequency through an IQ modulator.

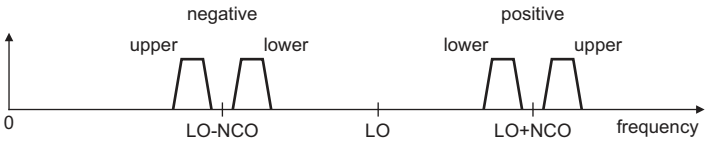


Fig 41. Complex modulation after LO mixing

11.2.4.4 40-bit NCO

The SSBM used the complex signals coming from the NCO (Numerically Controlled Oscillator) to mix the I and Q signals. The 5 registers XY_FREQNCO_B0 to XY_FREQNCO_B4 over 40 bits (0064h 0264h 0464h to 0068h 0268h 0468h) can set the frequency.

The frequency is calculated with Equation 1:

$$f_{NCO} = \frac{XY\_FREQ\_\mathrm{NCO} \times f_s}{2^{40}} \quad (1)$$

Where:

- XY_FREQ_NCO is the value set in the registers XY_FREQ_NCO[39:0].
- f_s is the final DAC output clock sampling frequency

The registers XY_PHINCO_LSB and XY_PHINCO_MSB over 16 bits from 0° to 360° (0062h 0262h 0462h / 0063h 0263h 0463h) can set the phase of the NCO.

11.2.4.5 NCO low power

When using NCO low power (bit XY_NCO_LOWPOWER; 0060h 0260h 0460h), the five most significant bits of register XY_FREQ_NCO[39:0] can set the frequency (bits [31:0] are masked by zero).

The frequency is calculated with Equation 2:

$$f_{NCO} = \frac{XY\_FREQ\_\mathrm{NCO} \times f_s}{2^{40}} \quad (2)$$

Where:

- XY_FREQ_NCO is the value set in the masked bits XY_FREQ_NCO[39:0] of the NCO frequency registers
- f_s is the DAC output clock sampling frequency

11.2.4.6 Minus 3dB

During normal operation, a full-scale pattern is also full-scale at the DAC output. When the I data and the Q data approach full-scale simultaneously, saturation can occur. The Minus 3dB function (bit XY_MINUS_3DB_GAIN of register XY_DSP_OUT_CNTRL; 006Fh 026Fh 046Fh) can be used to reduce the 3 dB gain in the modulator. It retains a full-scale range at the DAC output without added interferers.

11.2.4.7 Phase correction

The IQ modulator which follows the DACs can have a phase imbalance resulting in undesired sidebands. By adjusting the phase between the I and Q channels, the unwanted sidebands can be reduced.

Without compensation the I and Q channels have a phase difference of π / 2 (90°). The registers XY_PHASECORR_CNTRL0 and XY_PHASECORR_CNTRL1(0069h 0269h 0469h and 006Ah 026Ah 046Ah) ensure a phase variation from 75.7° to 104.3° by steps 0.0035°. The two registers define a signed value that ranges from –4096 to +4095. The equation: PH_CORR[12:0] / 16384 gives the resulting phase compensation (in radians). The phase correction can be enabled by register XY_PHASE_CORR_ENABLE.

11.2.4.8 Inverse sin(x) / x

A selectable FIR filter is incorporated to compensate the sin(x) / x effect caused by the roll-off effect of the DAC. The coefficients are represented in Table 19. This feature is controlled by register XY_INV_SINC_EN (0060h 0260h 0460h).

Table 19. Inversion filter coefficients

Inversion filter		
Lower	**Upper**	**Value**
H(1)	H(9)	+1
H(2)	H(8)	–4
H(3)	H(7)	+13
H(4)	H(6)	–51
H(5)	-	+610

Remark: The transfer function of this features adds some gain to the signals and some saturation can occur with a level of distortion in the output spectrum as result. Update the digital gain accordingly to avoid this saturation.

11.2.4.9 Digital gain

The full-scale output current for each DAC is the sum of the two complementary current outputs:

- $I_{OA(fs)} = I_{IOUTA\_P} + I_{IOUTA\_N}$
- $I_{OB(fs)} = I_{IOUTB\_P} + I_{IOUTB\_N}$
- $I_{OB(fs)} = I_{IOUTC\_P} + I_{IOUTC\_N}$
- $I_{OB(fs)} = I_{IOUTD\_P} + I_{IOUTD\_N}$

The IQ-modulator can have an amplitude imbalance which results in undesired sidebands. The unwanted sideband can be reduced by adjusting the amplitude of signals A and B. The two gains are purely digital and could be enabled by registers XY_DSP_X_GAIN_EN and XY_DSP_Y_GAIN_EN (006Fh 026Fh 046Fh).

The output current of DAC A depends on the digital input data and the gain factor defined by registers XY_DSP_X_GAIN_MSB and XY_DSP_X_GAIN_LSB (006Bh 026Bh 046Bh and 006Ch 026Ch 046Ch).

$$I_{IOUTX\_P} = I_{OX(fs)} \times \frac{(DAC\_X\_DGAIN[11{:}0])}{4096} \times \left(\frac{DATA}{65535}\right) \quad (3)$$

$$I_{IOUTX\_N} = I_{OX(fs)} \times \left(1 - \frac{(DAC\_X\_DGAIN[11{:}0])}{4096} \times \left(\frac{DATA}{65535}\right)\right) \quad (4)$$

The output current of DAC Y depends on the digital input data and the gain factor defined by registers XY_DSP_Y_GAIN_MSB and XY_DSP_Y_GAIN_LSB (006Dh 026Dh 046Dh and 006Eh 026Eh 046Eh).

$$I_{IOUYB\_P} = I_{OY(fs)} \times \frac{(DAC\_y\_DGAIN[11{:}0])}{4096} \times \left(\frac{DATA}{65535}\right) \quad (5)$$

$$I_{IOUTY\_N} = I_{OY(fs)} \times \left(1 - \frac{(DAC\_BY\_DGAIN[11:0])}{4096} \times \left(\frac{DATA}{65535}\right)\right) \quad (6)$$

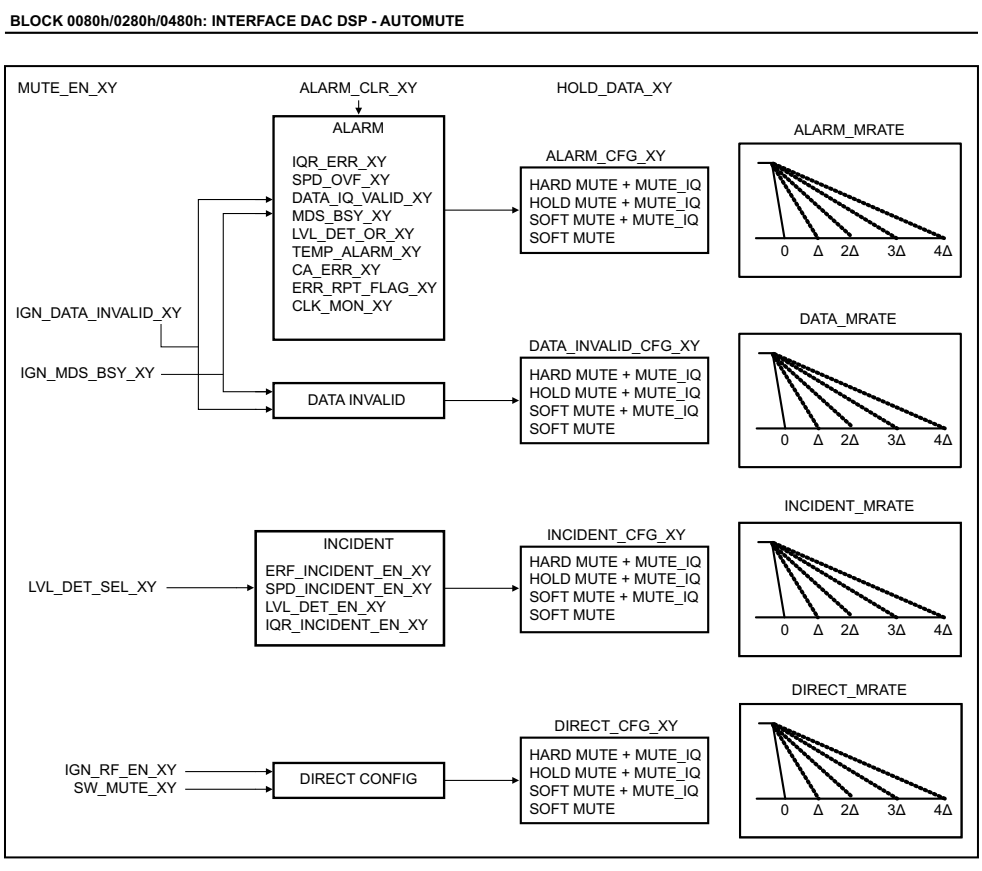
Table 20 shows the output current as a function of the input data, when $I_{OX(fs)} = I_{OY(fs)} = 20$ mA.

Table 20. DAC transfer function

Data	I15 to I0/Q15 to Q0 (binary coding)	I15 to I0/Q15 to Q0 (two's complement coding)	IOUTX_P/ IOUTY_P	IOUTX_N/ IOUTY_N
0	0000 0000 0000 0000	1000 0000 0000 0000	0 mA	20 mA
...	...	...	...	....
32768	1000 0000 0000 0000	0000 0000 0000 0000	10 mA	10 mA
...	...	...	...	...
65535	1111 1111 1111 1111	0111 1111 1111 1111	20 mA	0 mA

11.2.4.10 Auto-mute

The DAC165xQ provides a new Auto-mute feature allowing muting the DAC analog output if a conditional event occurs. The Auto-mute feature is based on a state machine as described in Figure 43 and on the control of the digital gains.



Block 0080h = DAC A/B
Block 0280h = DAC C/D
Block 0480h = All DACs

Fig 42. Auto-mute overview

In normal operating mode, the state machine is in IDLE state. The digital gains are specified by the user.

Various mute events can be detected in the DAC. These trigger the MUTE state. Once the MUTE state is entered, the DAC automatically sets the digital gains to zero using several mute actions. The SOFT mute and HOLD mute drops to zero gradually. The HARD mute drop to zero instantly (see Figure 44).

When the digital gains have been set to zero, the state machine enters the WAIT state. In this state, the gains are kept at zero. The state machine stays in this mode until the end of the wait period and the mute event is not de-asserted.

When the mute event is cleared and the wait period has elapsed, the state machine enters the DEMUTE state. In this state, the digital gains are set again to the initial values. This is done relatively to the mute rate setting. If during this state, a new mute event is triggered, the state machine enters the MUTE state again. The gain decreases from the current gains values, not from the initial ones.

When the digital gains reach the initial values, the state machine enters the IDLE state again.

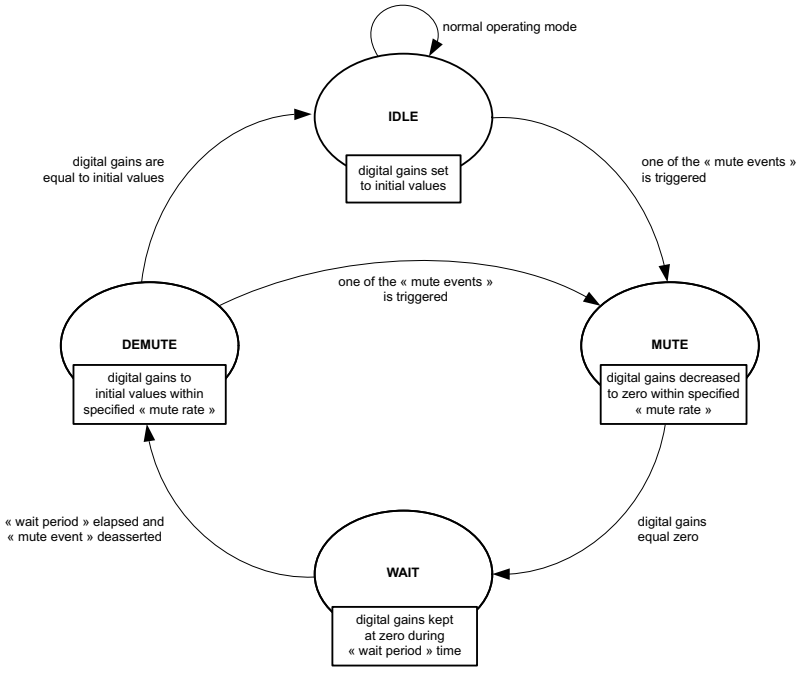


Fig 43. Auto-mute state machine

The mute feature is set by enabling bit XY_MUTE_ENA in register XY_MUTE_CNTRL_0 (see Table 82).

Mute events

The MUTE action is triggered by one of the following mute events. Each of them is linked to either an error detection, a status change or signal power monitoring:

- SW_MUTE:

  Software event that can be requested by the host interface through the SPI bus.
- RF_EN:

  Hardware event that can be requested by the host interface through pin RFTX_ENABLE (= IO1)
- CLK_MON (XY_MC_AL_ENA[0]):

Event linked to the monitoring of the clocks in the receiver physical layer control block.

- MON_DCLK_ERR:

  Event triggered when a clock error occurs in the CDI (see Section 11.2.7.1).
- CA_ERR:

  Event triggered when a clock error occurs in the DLP (see Section 11.9.3).
- TEMP_ALARM:

  Event triggered when the temperature sensor measures a temperature that exceeds the threshold value. TEMP_SEL_MAN must be specified first.
- ERR_RPT_FLAG:

  Event triggered when error report flag is detected by the DLP (see Section 11.9.3).
- CLIP_DET:

  Event triggered when the signal levels exceed the XY_CLIPLEV level on channel X or Y. XY_CLIPDET_ENA, XY_CLIP_LEV_EN and XY_CLIP_SEL LVL_DET_XY must be set first.
- MDS_BSY:

  Event triggered while the MDS process is busy with capturing the SYSREF (see Section 11.8.3).
- DATA_IQ_VALID:

  Event is triggered when DATA_INVALID is detected by the DLP (see Section 11.9.3)
- SPD_OVF:

  Event triggered when the Signal Power Detector (SPD) average value is exceeding the threshold value (Section 11.2.5.2).
- IQR_ERR:

  Event triggered when the IQ signal is out of range (see Section 11.2.5.3).

The monitoring of these events can also be done using the interrupt process available in the DAC165xQ (see Section 11.9). Once the interrupt is detected, the host controller (e.g. an FPGA) can read back the events flags in registers XY_INTR_FLAGS_0 and XY_INTR_FLAGS_1 and determine the actions to be taken.

Ignore events option

Set bits XY_IGNORE_RFTX_ENA, XY_IGNORE_MDS_BSY, and XY_IGNORE_DATA_V_IQ of the mute control register for the mute controller to ignore certain events.

Mute event categories

The MUTE state is entered when one of the mute events is asserted. Four categories of mute events can be distinguished: ALARM, DATA, INCIDENT, and DIRECT. For each categories specific mute action could be selected. The control of these events is summarized in Table 21

Table 21. Mute event categories control

Mute event	ALARM[1]	DATA	INCIDENT	DIRECT
	Enable register bit	Disable register bit	Enable register bit	Enable register bit
SW_MUTE				XY_SW_MUTE_ENA[2]
RF_EN				XY_IGNORE_RFTX_ENA
CLK_MON	XY_CLK_MON_AL_ENA[3]			
MON_DCLK_ERR	XY_MON_DCLK_ERR_AL_ENA[3]			
CA_ERR	XY_CA_ERR_AL_ENA[3]			
TEMP_ALARM	XY_TEMP_ALARM_AL_ENA[3]			
ERR_RPT_FLAG	XY_ERR_RPT_FLAG_AL_ENA[3]		XY_ENA_ERF_INCIDENT	
LVL_DET_OR	XY_LVL_DET_OR_AL_ENA[3]			
MDS_BSY	XY_MDS_BSY_AL_ENA[3]	XY_IGNORE_MDS_BSY		
DATA_IQ_VALID	XY_DATA_IQ_VALID_AL_ENA[3]	XY_IGNORE_DATA_V_IQ		
SPD_OVF	XY_SPD_OVF_AL_ENA[3]		XY_ENA_SPD_INCIDENT	
IQR_ERR	XY_IQR_ERR_AL_ENA[3]		XY_ENA_IQR_INCIDENT	

[1] All ALARM mute events can be disabled using bit XY_IGNORE_ALARM. However, their detection can still be monitored using the INTERRUPT module.

[2] This bit is not auto-clear.

[3] The ALARM mute events must be cleared with bit XY_MC_ALARM_CLR to move from the WAIT state to the DEMUTE state.

Priority between categories

- The priority in which the Auto-mute module evaluates its inputs is:
- Priority 1: DIRECT
- Priority 2: ALARM
- Priority 3: DATA
- Priority 4: INCIDENT

Mute actions

Four mute actions can be selected for each of the four previous mute event categories.

- **Hard_mute + mute IQ**:

  The digital gains of the DACs are set to zero immediately (within 1 DAC clock period). The digital path is filled with the default I and Q levels value (defined with register XY_I_DC_LEVEL[15:0] and XY_Q_DC_LEVEL[15:0]) to avoid disturbances in the FIR filters.

- **Hold_mute + mute IQ:**

  The outputs of the DACs are kept to the latest good value (within 1 DAC clock period). The digital path is filled with the default I and Q levels value (defined with register XY_I_DC_LEVEL[15:0] and XY_Q_DC_LEVEL[15:0]) to avoid disturbances in the FIR filters.

  Remark: Bit XY_HOLD_DATA must be enabled for this action. If this bit is not set, the overall Hold_mute + mute IQ actions are not taken into account.

- **Soft_mute + mute IQ:**

  The digital gains of the DACs are swept down to zero at the mute rate value. The digital path is filled with the default I and Q levels value (defined with register XY_I_DC_LEVEL[15:0] and XY_Q_DC_LEVEL[15:0]) to avoid disturbances in the FIR filters. The DAC165xQ provide the possibility to use different mute rate for incident/data/alarm/direct mute category (using registers XX_ALARM_MRATE / XX_DIRECT_MRATE / XX_INCIDENT_MRATE/ XX_DATA_MRATE). But for proper operation **all** these registers must be set with same value.

- **Soft_mute:**

  The outputs of the DACs are swept down to zero at the mute rate value. The digital path is kept with the received values.

  Remark: As the DC offsets are applied after the digital gain, the outputs are still impacted by their values, even if a mute action event occurs.

Remark: The time period used to decrease or increase the gains during a MUTE or DEMUTE state is called mute rate. Device implementation enables to have for each mute action category, its own mute rate through the registers XX_ALARM_MRATE / XX_DIRECT_MRATE / XX_INCIDENT_MRATE/ XX_DATA_MRATE. But for proper operation **all** these registers must be set with same value. The Table 22 gives the mute time corresponding to possible registers value.

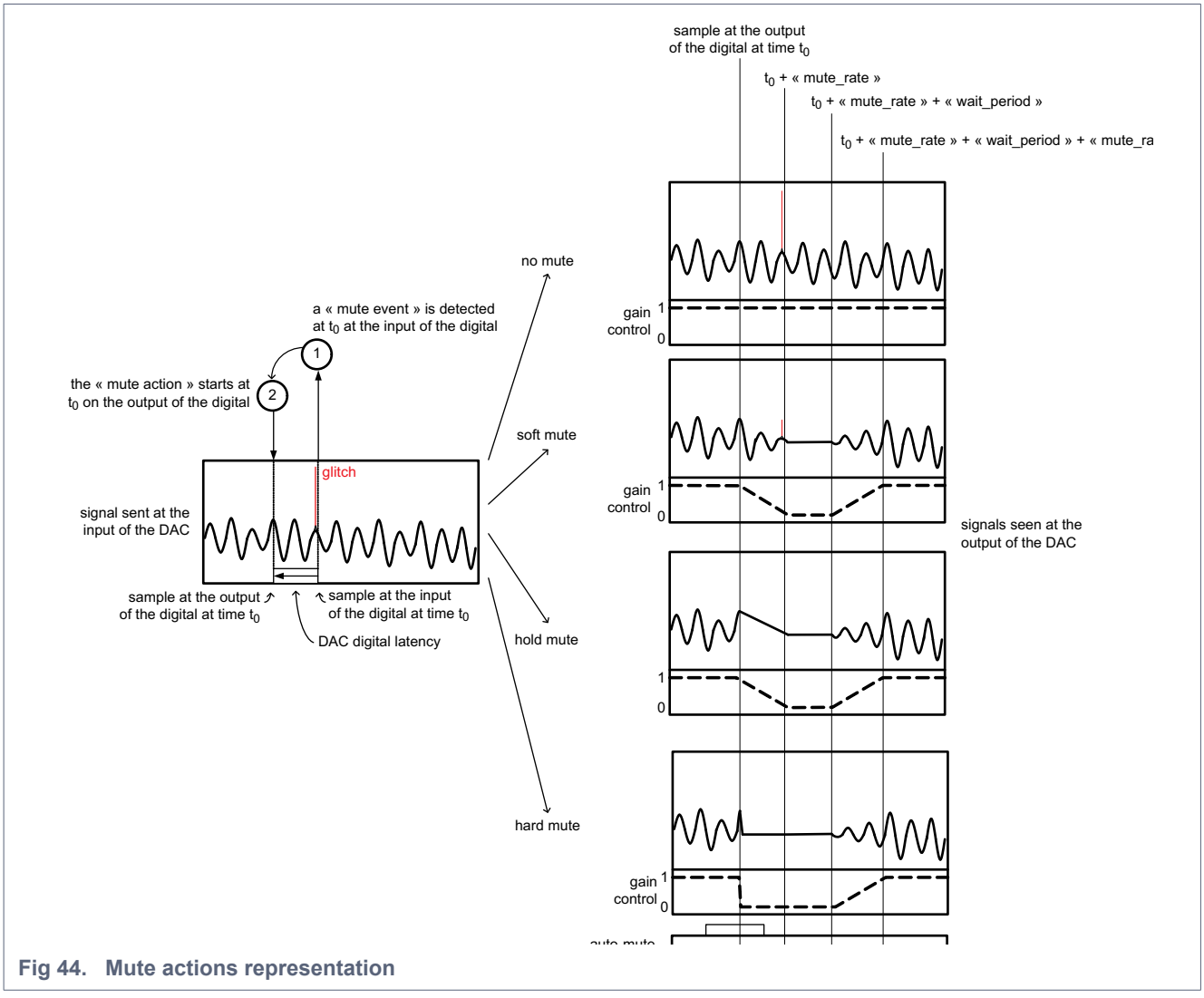


Fig 44. Mute actions representation

Table 22. Mute rate availability
Through XX_ALARM_MRATE / XX_DIRECT_MRATE / XX_INCIDENT_MRATE and XX_DATA_MRATE.

DAC clock	750 MHz	1 GHz	1.5 GHz
Period ×8 (ns)	10.67	8.00	5.33
Value	Mute rate (ns)	Mute rate (ns)	Mute rate (ns)
0000	10.67	8.00	5.33
0001	21.34	16.00	10.66
0010	42.68	32.00	21.32
0011	85.36	64.00	42.64
0100	170.72	128.00	85.28
0101	341.44	256.00	170.56
0110	682.88	512.00	341.12
0111	1,365.76	1,024.00	682.24
1000	2,731.52	2,048.00	1,364.48
1001	3,642.47	2,731.00	1,819.53
1010	5,463.04	4 096.00	2,728.96
1011	7,283.61	5,461.00	3,638.39
1100	10,926.08	8,192.00	5,457.92
1101	14,557.88	10,915.00	7,272.12
1110	21,852.16	16,384.00	10,915.84
1111	43,704.32	32,768.00	21,831.68

Mute wait period

The wait period time can be calculated with Equation 7:

$$wait\ period = (MUTE\_WAIT\_PERIOD + 1) \times 8 \times DAC\_CLK\_PERIOD \quad (7)$$

At 1 Gsps, this gives a wait period between 8 ns and 527 μs.

DEMUTE triggering

When the mute action is either a DIRECT, an INCIDENT or a DATA mute action, the WAIT state is enabled as long as the wait period is not elapsed and the event is not released.

When the mute action is an ALARM mute action, the WAIT state is enabled as long as the alarm controller is not reset using bit XY_MC_ALARM_CLR.

11.2.4.11 Digital offset adjustment

When the DAC165xQ analog output is DC connected to the next stage, the digital offset correction (bits XY_DSP_X_OFFSET[15:0] and XY_DSP_Y_OFFSET[15:0]) can be used to adjust the common-mode level between IOUTxN and IOUTxP pins at the output of each DAC. Table 23 shows the variation range of the digital offset.

Table 23. Digital offset adjustment

XY_DSP_X_OFFSET[15:0] XY_DSP_Y_OFFSET[15:0] (two's complement)	Offset applied
1000 0000 0000 0000	−32768
1000 0000 0000 0001	−32767
...	...
1111 1111 1111 1111	−1
0000 0000 0000 0000	0
0000 0000 0000 0001	+1
...	...
0111 1111 1111 1110	+32766
0111 1111 1111 1111	+32767

Care should be taken when adding DC offset to large signal.The resulting signal might exceeds the 16 bits dynamic of the DAC.

11.2.5 Signal detectors

11.2.5.1 Level detector

A level detector feature is available at the end of the digital path. It can be enabled using bit XY_CLIP_LEV_EN. This feature specifies a signal output range limited (or clipped) to −128 × LVL_DET_XY to +128 × LVL_DET_XY around the half Full-Scale (FS) . If the signal value enters the upper or lower clipping area, it is clipped to +128 × LVL_DET_XY or −128 × LVL_DET_XY, respectively). Figure 45 shows this behavior.

Use this feature in combination with the auto-mute feature to avoid unexpected spectral spurs after the clipping of the signal (see Section 11.2.4.10).

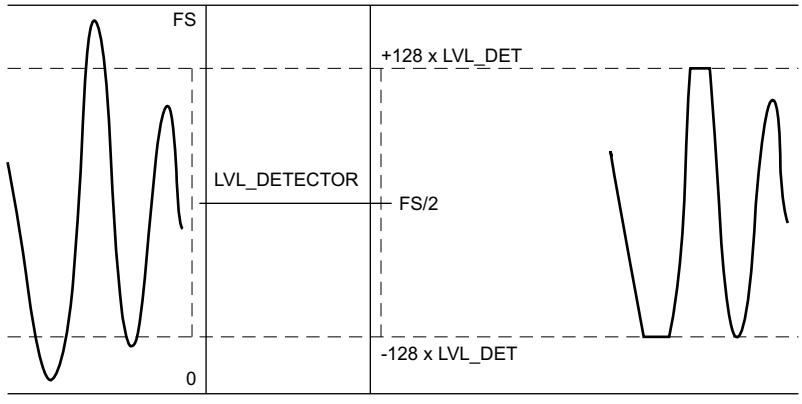


Fig 45. Level detector operation

Table 24. Level detector values

LVL_DET_XY[7:0]	Peak excursion from full-scale / 2	Code output range (binary offset)	dBFS value 10log(peak excursion x 2 / 65536)
00h	0	32768	Na
...		...	...
19h	3200	32568 to 35968	−10.1 dBFS
...		...	...
80h	16384	16384 to 49152	−3 dBFS
...		...	...
CBh	25984	6784 to 58752	-1 dBFS
...		...	...
FFh	32768	0 to 65536	0 dBFS

11.2.5.2 Signal Power Detector (SPD)

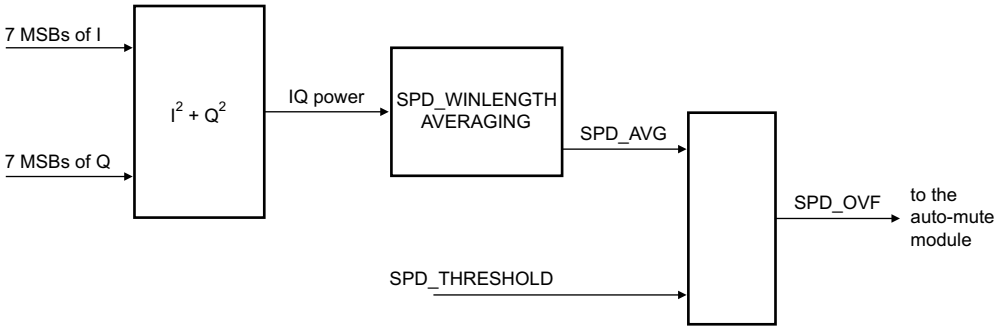


Fig 46. Signal power detector

The Signal Power Detector (SPD) takes the 7 MSBs of the I and Q signal to determine the IQ power of an IQ-pair. Averaging is done over the programmable number (2^6, 2^7 to 2^{21}) of IQ-pairs using the XY_SPD_WINLENGTH register. If the average value (readable in register XY_SPD_AVERAGE) exceeds the 16-bits threshold value (defined in register XY_SPD_THRESHOLD), the SPD overflow (SPD_OVF) flag becomes active and can invoke a mute action depending on the mute control settings.

The SPD can have a large response time because of the samples average based algorithm. This must be taken into account at system level.

11.2.5.3 IQ Range (IQR)

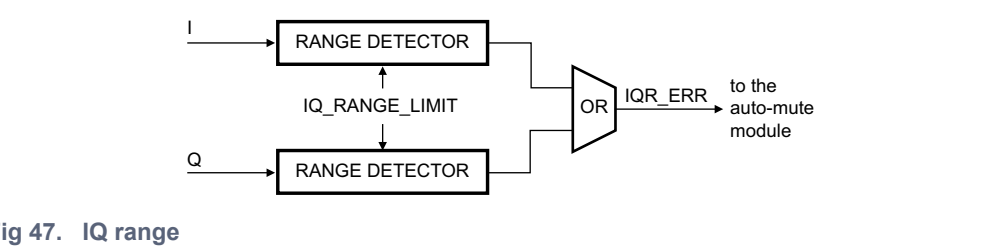


Fig 47. IQ range

The IQ range detector checks if the I and Q signal values are within the range specified by register XY_IQ_RANGE_LIMIT[15:0] compared to the center value (= 0 if the data are in 2 complement's representation or 32768 if the data are in binary offset representation):

–XY_IQ_RANGE_LIMIT < I – center value < +XY_IQ_RANGE_LIMIT

–XY_IQ_RANGE_LIMIT < Q – center value < +XY_IQ_RANGE_LIMIT

11.2.6 Pin RF_ENABLE

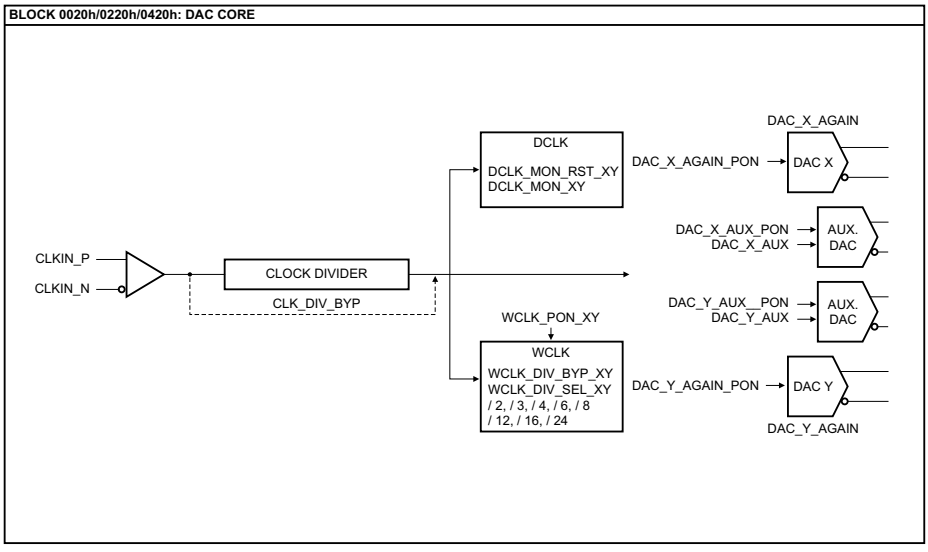
A RF_ENABLE/IO1 pin is available to powerdown the analog output of the DACs. The shutdown consists in a MUTE request on the MUTE controller. This trigger is active low and is part of the direct mute events container (see Section 11.2.4.10). by default this feature is enabled. This means that to enable the DACs output, a signal high needs to be applied on the pin. When applying a signal low, the MUTE controller will mute the DACs output.

The following registers must be set to configure pin IO1 in RF_ENABLE mode (these are the default values at start-up time):

- IO_ENA[1] must be set to '0' to set the pin to input mode.
- XY_IGNORE_RFTX_ENA must be disabled to allow the triggering of the event
- RFTX_ENA_PD_ANA_CD and RFTX_ENA_PD_ANA_AB bits must be enabled

11.2.7 Analog core of the DAC

This section refers to the analog configuration required to set up the dual DAC core. The clock and output stages are described as well as the internal registers (Block x0020; see Figure 48 and Table 49) used to configure the clock tree inside the chip.



Block 0020h = DAC A/B, Block 0220h = DAC C/D, Block 0420h = All DACs

Fig 48. DAC core overview

11.2.7.1 Clocks

The DAC165xQ requires one single differential clock (CLKIN_P, CLKIN_N) for the whole device (including the digital data path, the DAC core and the JESD204B interface).

During the reset phase (RESET_N asserted), the input clock must be stable and running, ensuring a proper reset of the complete device.

On-chip Phase-Locked Loop (PLL)

The DAC165xQ has a single differential clock input to directly feed the digital and analog clock tree of the device. When using the embedded PLL, a reference clock has to be provided at this input. The mixed-signal PLL synthesizes the correct internal clocks with very low jitter. Figure 49 shows a conceptual view of the PLL. Digital control words that control the oscillator frequency determine the output frequency of the PLL:

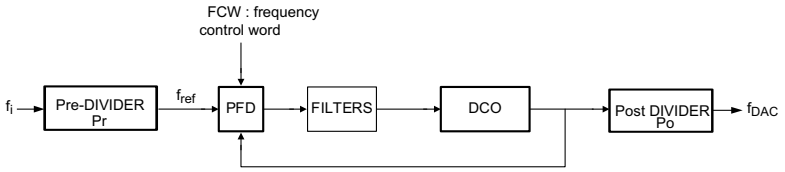


Fig 49. PLL block diagram

The pre-divider (Pr) and post-divider (Po) can be programmed in order to generate targeted DAC sampling frequency. The DAC sampling clock frequency can be calculated with Equation 8:

$$F_{DAC} = \frac{FCW}{Po \times Pr} \times f_i \quad (8)$$

The DCO clock frequency can be calculated with Equation 9:

$$F_{DCO} = \frac{FCW}{(Pr)} \times f_i \quad (9)$$

The DAC165XQ includes a DCO center frequency tuning capability. To get wide DCO frequency compliance range (as described in Table 6), it recommended to program ADPLL_DCO_CTF[7:0] register with the value given by Equation 10 (round result in order to have min value =0 max value=0x0F):

$$ADPLL\_DCO\_CTF = \frac{(F_{DCO} - 3600MHz)}{37.5Mhz} \quad (10)$$

In order to get a valid combination of FCW, Pr and Po, the compliance range for both Fref (=Fclkin/N) and Fdco as defined in Table 6 must be considered. Table 25 give some examples of valid combinations:

Table 25. PLL setting examples

f_i (MHz)	Pr	f_{ref} (MHz)	FCW	DCO (MHz)	Po	F_{DAC} (MHz)	PLL_DCO_CTF
491.52	8	61.44	0x40	3932.16	4	983.04	0x8
122.88	2	61.44	0x40	3932.16	4	983.04	0x8
122.88	2	61.44	0x48	4423.68	3	1474.56	0xF
122.88	2	61.44	0x3C	3686.4	3	1228.8	0x2

Clock input external configuration

The DAC165xQ incorporates one differential clock input, CLKIN_N/CLKIN_P, with embedded 100 Ω differential termination resistor. The clock input can be LVDS but it can also be interfaced with CML.

The clock input buffer is self biased. An AC coupling circuit is recommended as shown in Figure 50. The minimum requested differential voltage is given in Table 6 but a higher voltage swing of 1000mVpp,diff will give better results.

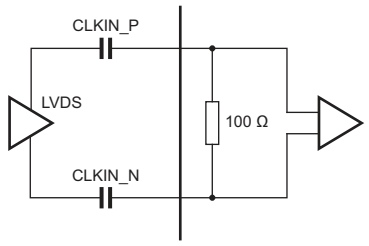


Fig 50. DAC clock interface

Clock frequency input range

The DAC165xQ can only operate in two modes:

- Direct clocking mode:

  The input clock frequency is limited to 2000 MHz
- Divided clocking mode:

  The input clock is internally divided by 2, 4, 6, or 8. The maximum input frequency is 3 GHz. This mode allows the programming of the group delay feature.

Clocks internal configuration

The following registers must be specified to configure the DAC165xQ clocking mode:

- CLKGENCFG1 to specify the WCLK configuration.
- CLKDIV_CFG to specify the DCLK configuration and the divider / group delay feature.
- PON_DCKDIV_CFG to power on the clock divider (required only for divided clock) (see Table 55)

The final clock is referred to as the "DAC clock". This is the clock that is going directly to the DAC core and is running at maximum speed. From this DAC clock two digital clocks are derived: DCLK and WCLK.

DCLK is the digital clock used for all logic related to the Digital Signal Processing (DSP) of the DAC.

WCLK is the digital clock used for all logic related to the Digital Lane Processing (DLP) of the input interface. The divider ratio WCLK_DIV_SEL (see Table 54) must be specified using the following equation:

$$\frac{WCLK}{DAC\_Clock} = \frac{M}{(L \times INTERPOLATION)} \quad (11)$$

Where:

- M stands for the number of DACs used inside the dual core DAC (=2).
- L stands for the number of serial input lanes used (L = 1, L = 2, or L = 4)
- INTERPOLATION stands for the interpolation factor specified in registers XY_TXCFG and CDI_CNTRL.

Table 26 shows the results for nominal use cases

Table 26. WCLK_DIV selection

LMF configuration	Interpolation ratio	WCLK/DAC clock	WCLK_DIV_BYPASS	WCLK_DIV_SEL
421 / 422	2	1/4	0	010
	4	1/8	0	100
	8	1/16	0	110
222	2	1/2	0	000
	4	1/4	0	010
	8	1/8	0	100
124	2	1	1	xxx
	4	1/2	0	000
	8	1/4	0	010
211	2	1/2	0	000
	4	1/4	0	010
	8	1/8	0	100

Clock divider and Group Delay configuration

To enable the Clock division, the dividers biasing should be powered on using PON_CGFG_NC. Then the division ratio CLK_DIV_SEL needs to be configured and the default bypass mode must be disabled (CLK_DIV_BYPASS register). In this mode, the CLKDIV_SEL_PHASE bits are used to specify the group delay phase. The CLKDIV_SEL_DIV must be set during the DAC initialization phase only (see Table 57).

When changing the DAC clock phase during nominal usage, the DAC output will be kept at the previous value while the new phase is set. For instance, setting the DAC clock phase from setting 0 to setting 1 will imply a 1.5 DAC clock constant value. No glitches are expected during this phase.

Table 27. XY_CLKDIV_SEL_PHASE selection

CLKDIV_SEL_PHASE	
000	DAC clock phase = 0
001	DAC clock phase = 1 x (CLK IN period) /2
010	DAC clock phase = 2 x (CLK IN period) /2
011	DAC clock phase = 3 x (CLK IN period) /2
100	DAC clock phase = 4 x (CLK IN period) /2
101	DAC clock phase = 5 x (CLK IN period) /2
110	DAC clock phase = 6 x (CLK IN period) /2
111	DAC clock phase = 7 x (CLK IN period) / 2

Clock Domain Interface (CDI)

A CDI logic handles the error-free data transition from the WCLK clock domain to the DCLK domain. It consists of 12 buffers that absorb the phase variation between the two clocks. The reliability of the data transmission depends on the clock-frequency ratios and therefore on the interpolation mode. The CDI must be set in the same mode as the interpolation ratio to be properly configured. This mode is configured with register CDI_CNTRL.

Table 28. Interpolation and CDI modes

Interpolation	CDI_mode_AB CDI_mode_CD	Maximum input data rate (Msps)
		DAC165xQ1G5 / DAC165xQ1G0
~1	Mode 0 (^2)	1000
×2	Mode 0 (^2)	1000
×4	Mode 1 (^4)	500
×8	Mode 2 (^8)	250

Ideally, buffer number 11 is selected as the reference. If jitter of +/- 1 clock cycle is injected between the clocks occurs, the pointer can oscillate between buffers 10 and 0. If more jitter is injected, the range increases to buffers 9 and 1, etc.

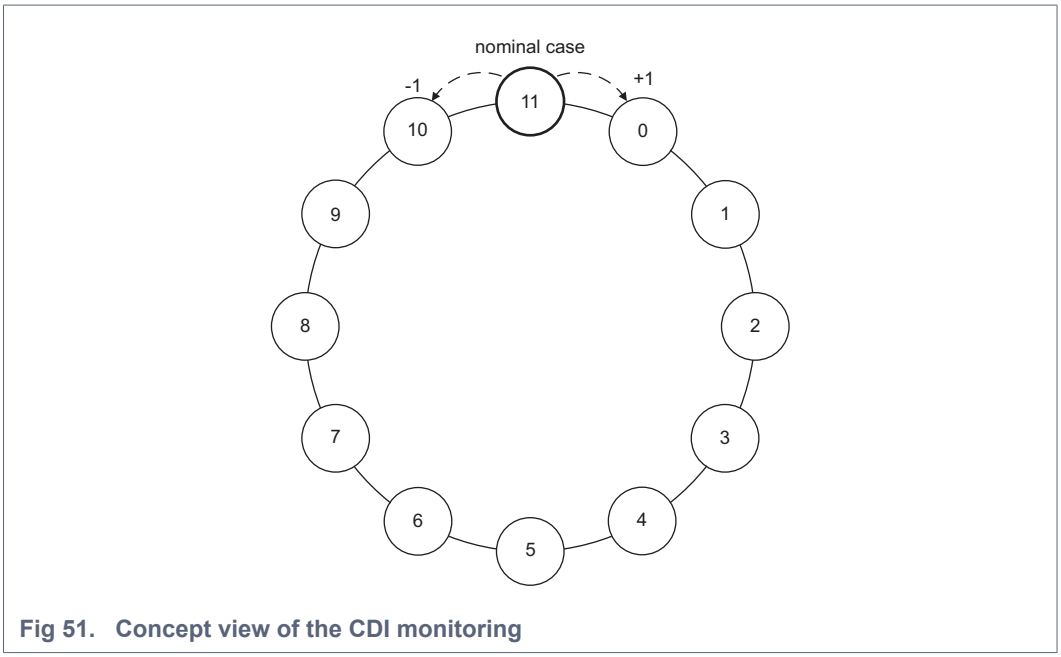


Fig 51. Concept view of the CDI monitoring

This buffer position can be monitored using register MON_DCLK_AB and MON_DCLK_CD flags.

The variation of the buffer location could also raise an interrupt (see Section 11.9).

11.3 Overall Latency

The implementation of the different features of the DAC165xQ imply a different latency regarding the mode used. This latency is dependent of the following features:

1. the LMF-S configuration
2. the Interpolation mode
3. the Phase Correction usage
4. the SSBM/NCO usage
5. the InvSin(x)/x usage

The total latency is expressed in DAC clock cycles and could therefore be scaled regarding the DAC clock frequency used. Moreover, the values of the table are showing the uncertainties due to the internal design implementation. There are two buffers/fifo that are used to compensate the skew between the lanes (see registers XY_ILA_MON_L_LN xx) and to delay

the data path (XY_MDS_MAN_ADJUSTDLY). The values of the Table 29 are provided for the case when all the lanes are aligned (XY_ILA_MON_L_LN xx= 8 by default) and the XY_MDS_MAN_ADJUSTDLY is set to 0 (minimal delay). See Table 30 for additional delays.

Remark: The overall latency values are given when the MDS feature is not used.

Table 29. Latency for LMF-S= without : MDS , Phase correction, SSBM, and InvSin x/x

LMF-S	Interpolation	Total latency DAC clk		
		min	avg	max
421-1 or 422-2	x2	250	254	266
	x4	420	424	444
	x8	740	744	780
222-1	x2	216	220	228
	x4	352	356	368
	x8	588	592	612
124-1	x2	195	199	205
	x4	310	314	322
	x8	504	508	520

Table 30. Additional latency

Digital feature	Additional latency
Lanes skew compensation	+/- 7 wclk (see Table 26 for the DAC clock ratio)
XY_MDS_MAN_ADJUSTDLY	0 to 256 DAC clk
Phase Correction	+16 DAC clk
SSBM/NCO	+16 DAC clk
InvSin(x)/x	+4 DAC clk

11.4 Analog quad DAC core

The DAC165xQ core consists of four DACs. Each of them can be independently set to Power-down mode dedicated register XY_PON_DDCCFG_0.Please note that as DAC A is used as CGU/BIAS master of other DACs, so it recommended when DAC A is not used (but other DACs are still used), to only power down DAC A core and DAC A commutator using bit XY_PON_DAC_X and XY_PON_COMM_X of register XY_PON_DDCCFG_0.

11.4.1 Regulation

The DAC165xQ reference circuitry integrates an internal band gap reference voltage which delivers a 0.7 V reference on the GAPOUT pin. Decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of 562 Ω (1 %) connected to VIRES pin.

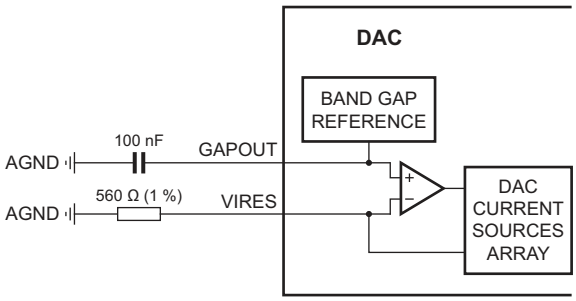


Fig 52. Internal reference configuration

Figure 52 shows the optimal configuration for temperature drift compensation because the band gap reference voltage can be matched to the voltage across the feedback resistor.

The DAC current can also be adjusted by applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal band gap reference voltage (bit PON_GAP of register PON_CFG_NC).

11.4.2 Full-scale current adjustment

The default full-scale current ($I_{O(fs)}$) is 20 mA. However, further adjustments, ranging from 10 mA to 30 mA, can be made to each DACs independently using the SPI interface. The registers values allowed to reach lower and higher current values but those values are out the range that maintains the typical dynamics performances.

The settings applied to XY_CSA_BIAS_X[9:0] and XY_CSA_MULT2_X define the full-scale current of DAC X:

$$I_{O(fs)}\ \mu A = 2^{XY\_CSA\_MULT2\_X} \times XY\_CSA\_BIAS\_X[9{:}0] \times 25 \quad (12)$$

The XY_CSA_BIAS_Y[9:0] and XY_CSA_MULT2_Y define the full-scale current of DAC Y:

$$I_{O(fs)}\ \mu A = 2^{XY\_CSA\_MULT2\_Y} \times XY\_CSA\_BIAS\_Y[9{:}0] \times 25 \quad (13)$$

11.5 Analog output

11.5.1 DAC1658Q: High common-mode output voltage

The device has four output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IOUTA_P/IOUTA_N, IOUTB_P/IOUTB_N, IOUTC_P/IOUTC_N and IOUTD_P/IOUTD_N. Connect these pins using a load resistor R_L to the 3.3 V analog power supply ($V_{DDA(out)}$).

Figure 53 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of NMOS current sources and associated switches for each segment.

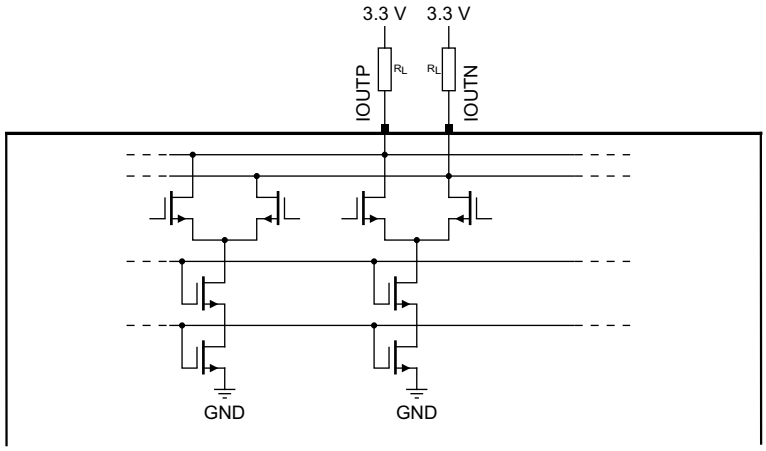


Fig 53. Equivalent analog output circuit

The cascode source configuration increases the output impedance of the source, which improves the dynamic performance of the DAC because there is less distortion.

11.5.2 DAC1653Q: Low common-mode output voltage

The device has four output channels, each producing two complementary current outputs, which enable the reduction of even-order harmonics and noise. The pins are IIOUTA_P/IOUTA_N, IOUTB_P/IOUTB_N, IOUTC_P/IOUTC_N and IOUTD_P/IOUTD_N. Connect these pins using a load resistor R_L to the analog ground (GND).

Figure 54 shows the equivalent analog output circuit of one DAC. This circuit includes a parallel combination of PMOS current sources and associated switches for each segment.

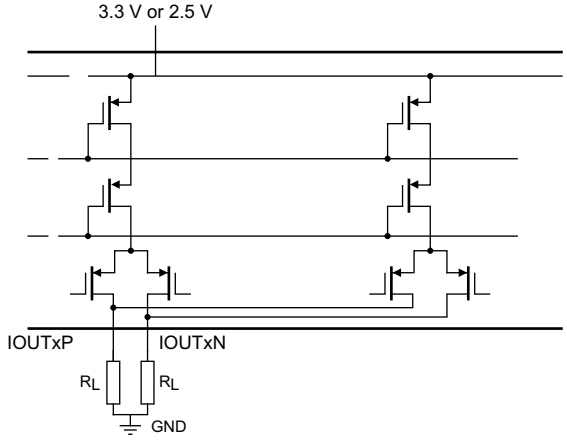


Fig 54. Equivalent analog output circuit

11.6 Auxiliary DACs

Each DAC output of the DAC165xQ is internally connected to auxiliary DACs, which are used to compensate any offset at DACs output (useful for example in order to compensate IQ modulator LO leakage). DAC1658Q auxiliary DACs sink current (referenced to $V_{DDA(out)}$). DAC1653Q source current (referenced to ground). Auxiliary DACs have a 10-bit resolution.these auxiliary DACs can be disabled using bits XY_PON_AUX_DAC_X and XY_PON_AUX_DAC_Y of the XY_AUX_CFG_X_0 and XY_AUX_CFG_Y_1 Auxiliary DACs registers.

The full-scale output current for each DAC is the sum of the two complementary current outputs:

$$I_{OAUX(fs)} = I_{AUX\_P} + I_{AUX\_N}$$

The output current depends on the SPI registers XY_AUX_DAC_X[9:0] and XY_AUX_DAC_Y[9:0]:

$$I_{AUX\_P} = I_{OAUX(fs)} \times \left(\frac{XY\_AUX\_DAC[9:0]}{1023}\right) \quad (14)$$

$$I_{AUX\_N} = I_{OAUX(fs)} \times \left(\frac{1023 - XY\_AUX\_DAC[9:0]}{1023}\right) \quad (15)$$

Table 31 shows the output current as a function of the auxiliary DACs setting :

Table 31. Auxiliary DAC transfer function

DATA	XY_AUX_DAC_X[9:0]/ XY_AUX_DAC_Y[9:0] (binary coding)	I_{AUX_P} (mA)	I_{AUX_N} (mA)
0	00 0000 0000	0	2.3
...	...	...	...
512	10 0000 0000	1.15	1.15
...	...	...	...
1023	11 1111 1111	2.3	0

11.7 Temperature sensor

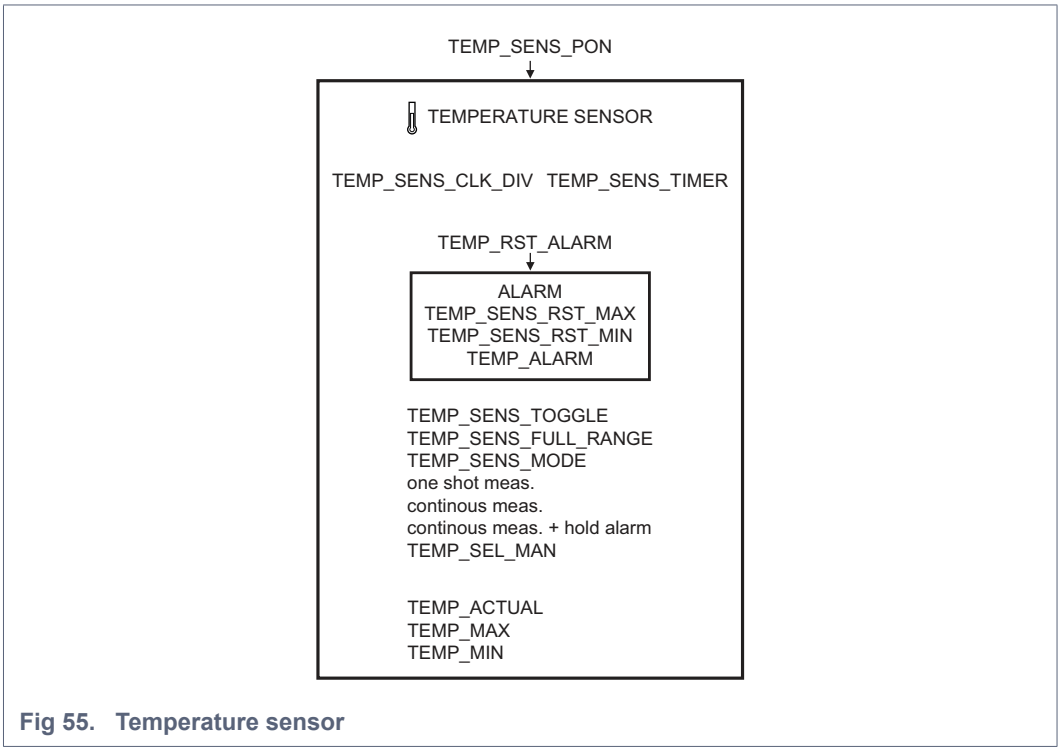


Fig 55. Temperature sensor

The DAC165xQ embeds a temperature sensor to monitor the temperature inside the chip. This module is based on a 6-bit resolution ADC clocked at DAC_CLK / (8 × TS_CLKDIV). The mode of measurements is configurable as a one shot measurement, continuous measurements or continuous measurements with alarm flag held in case of temperature

exceeding a preset threshold. In continuous mode, the measurement is done every TS_TIMER cycles. The TEMPS_LEVEL specifies the threshold level that is compared with the measured value. If the measured value exceeds the threshold, the TEMP_ALARM flag is set and triggers a mute action (see Section 11.2.4.10). The maximum and minimum temperatures measured are stored in registers TEMP_MAX and TEMP_MIN respectively. The current temperature is stored in register TEMP_ACTUAL. Once the TEMP_ALARM flag is set, it must be reset using the TS_RST_ALARM bit of the temperature sensor control register. The maximum and minimum temperature can also be reset using bits TS_RST_MAX and TS_RST_MIN of the temperature sensor TEMPS_CNTRL register.

The value stored in the TEMP_MAX, TEMP_MIN and TEMP_ACTUAL registers represents the output value of the ADC. This value could be converted in real die temperature using Equation 16.

$$T\,(°C) = T\alpha \times ADC\_value - Toffset \qquad \text{(refer to Table 6 for } T_{\alpha} \text{ and } T_{offset} \text{ definition)} \qquad (16)$$

For life time , it is recommended to have die junction temperature T_j < 125 °C, which could be easily checked by: TEMP_MAX < 0x26.

11.8 Multiple Device Synchronization (MDS); JESD204B subclass I

The MDS feature enables multiple DAC channels to be sampled synchronously and phase coherently to within one DAC clock period. This feature is part of the JESD204B standard but the implementation adds some unique features that simplify the PCB design.

11.8.1 Non-deterministic latency of a system

In a system using multiple DAC devices, there are numerous sources of timing uncertainties. Figure 56 gives an overview of these uncertainties.

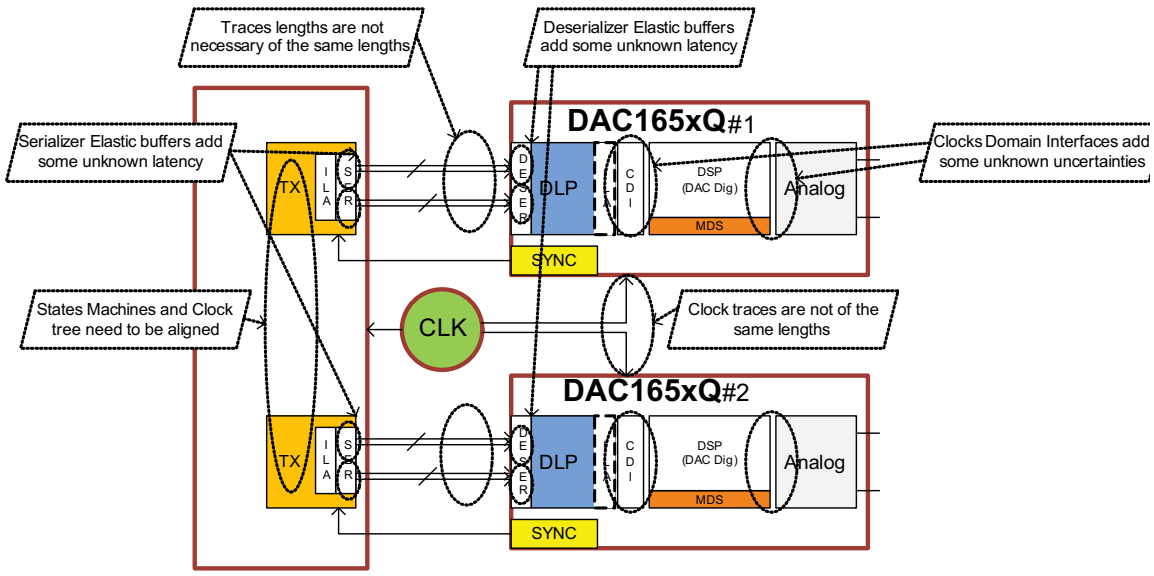


Fig 56. Timing uncertainties when using multiple DAC devices

The sources of uncertainties are shared between the Transmitter devices (TX), the Receiver devices (RX), the PCB layout and the architectures of the JESD204B system clocks. A single device can detect timing drift and uncertainties, but not at system level. Therefore a synchronization process is required to enable the system to output the analog signals of all the RX devices in a coherent way. Moreover, the system becomes predictable if from one start-up to another one, the overall latency is deterministic.

The MDS feature of the DAC165xQ has been implemented in accordance with the JESD204B subclass 1 specification to fulfill these requirements.

11.8.2 JESD204B system clocks and SYSREF clock

There are various system 'clocks' that are used in the JESD204B specification. However, only one of them is seen at system level, the device clock, which is provided to the device. The other clocks are related to the JESD204B standard and are used to assemble/de-assemble the data in octets and then in 10 bits words (see JESD204B standard). Figure 57 and Table 32 show the relationship between them.

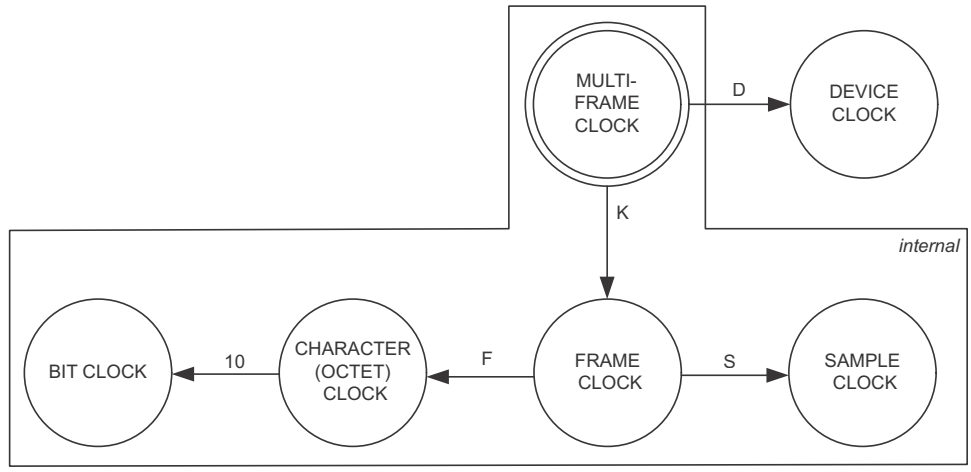


Fig 57. JESD204B system clocks

Table 32. Relationship between various clocks

Clock name	Ratio with respect to multi-frame clock	Comments regarding JESD204B specification
multi-frame clock	1	-
frame clock	× K	Ceil(17 / F) ≤ K ≤ min(32, floor(1024 / F))
character clock	× F × K	F = 1 to 256
bit clock	× 10 × F × K	8b/10b encoding
sample clock	× S × K	S = 1 to 32
device clock	× D	D is integer
sysref clock	/ R	R is integer

As all clocks can be derived from the Multi-Frame Clock (MFC), this clock becomes the reference for a JESD204B system. Each device used in the system has its own local version of the MFC. These local version are called Local Multi-Frame Clock (LMFC). Due to the timing uncertainties the phase relationships between all the device LMFCs are unknown. The goal of MDS is to be able to realign all LMFCs in a deterministic and accurate way.

To align all the LMFCs within the system, a new clock named SYSREF (SYStem REFerence) is used. This clock is linked to the multi-frame clock by a divided ratio R, therefore it is a low frequency signal.

The SYSREF signals must be propagated to all the devices of the system. They are used as a timing reference to align the internal LMFC of each devices. To ensure that all phases of the signals are aligned at the source, the SYSREF signals and the device clocks must be generated from the same clock IC (see Figure 58). The appropriate clock device could be found within the IDT Timing Division unit portfolio.

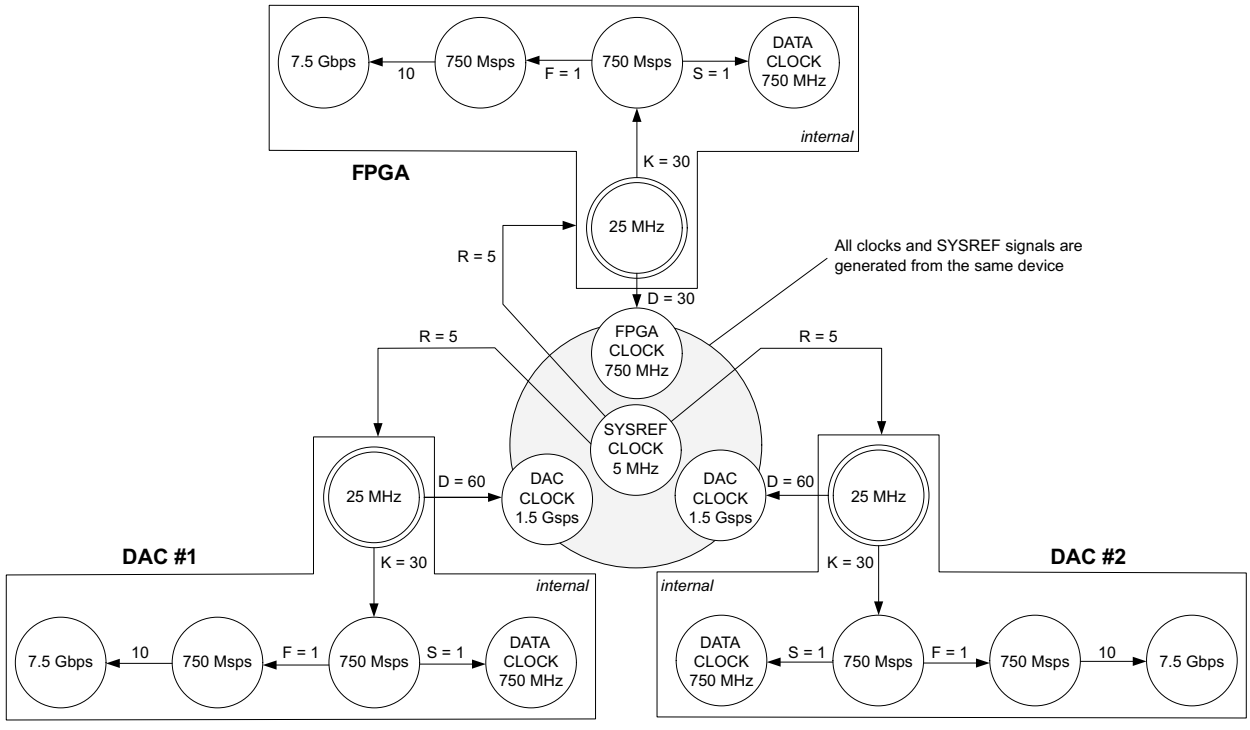


Fig 58. System overview

All the JESD204B devices will capture their SYSREF signal and use it to align their datastream/LMFC. The edge detection of the SYSREF signal is used as a system timing reference and the device align their LMFCs phase to the closest edge of the SYSREF. To ensure an accurate alignment within all devices, the SYSREF signal must show the same phase at the input port of all the devices to synchronize. Therefore, the trace lengths of the SYSREF signals must be equal for all the DAC devices.

The DAC165xQ embeds updated SYSREF buffers. Both West and East side can use the incoming SYSREF signal asynchronously to remove the uncertainties due to the sampling moment inside each devices. There is no more setup and hold constraint on the SYSREF signal in asynchronous mode.

The following figure shows the virtual LMFCs before and after alignment to the SYSREF clock.

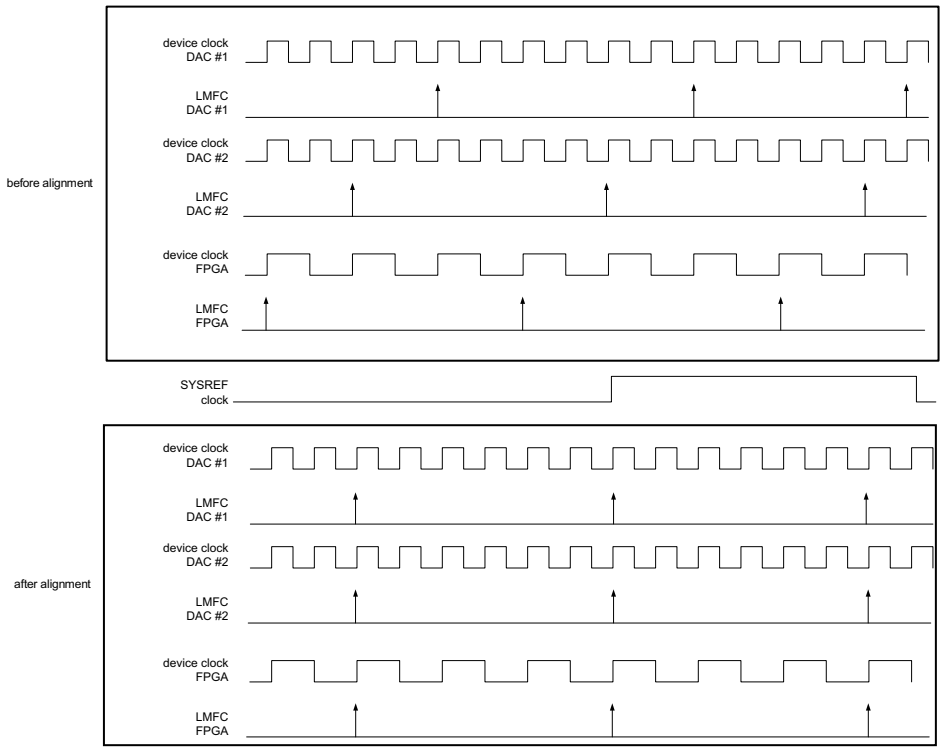


Fig 59. LMFCs before and after alignment to the SYSREF clock

11.8.3 MDS implementation

The DAC165xQ MDS implementation is based on two modules as described in Figure 60:

- **M1**:

  This module contains the SYSREF detector and the control loop used to create a $LMFC_{MDS}$ signal. The control loop is clocked with the digital clock. The digital clock equals DAC clock / 8.

- **M2**:

  This module compares the phase of the $LMFC_{RCV}$ received from the JESD204B digital lane processing to the phase of the $LMFC_{MDS}$ and shifts the position of the buffer to align the data path to the $LMFC_{MDS}$.

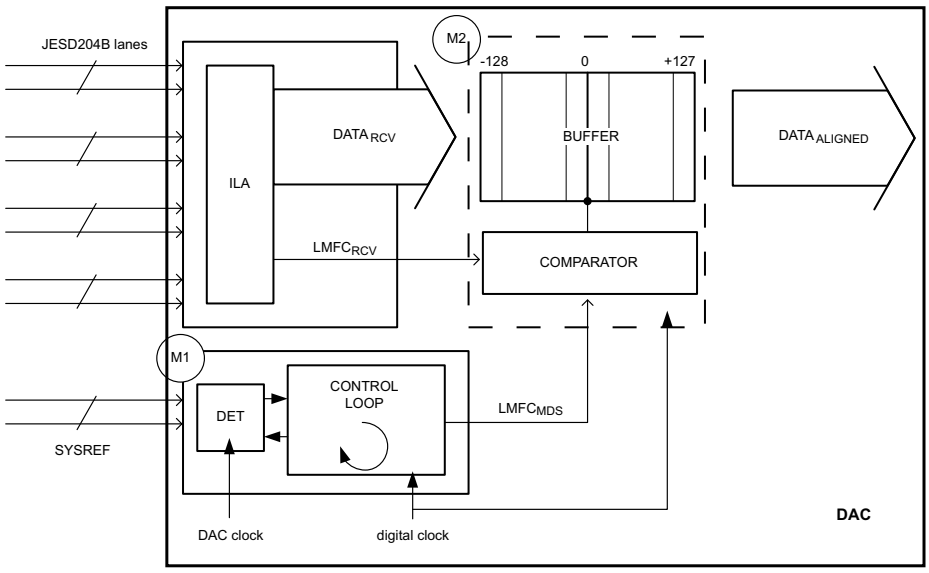
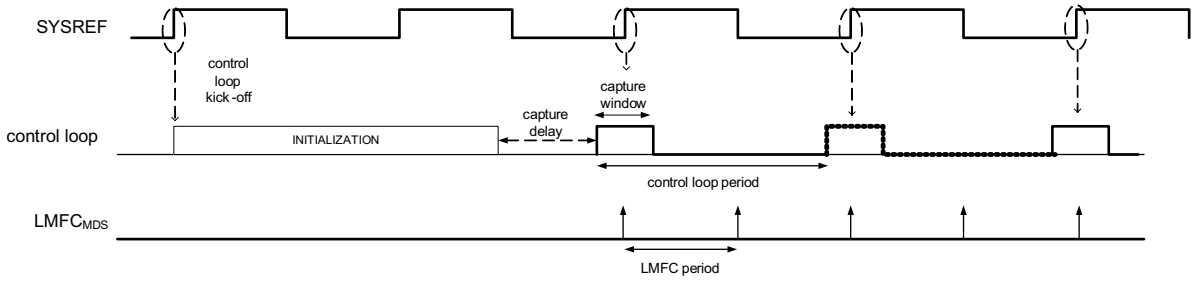


Fig 60. Modules of MDS implementation

11.8.3.1 Capturing the SYSREF signal

Module M1 ensures the capture of the SYSREF signal at DAC clock accuracy. This is done by an early-late detector and a control-loop. The control-loop must capture several SYSREF edges to deliver an accurate $LMFC_{MDS}$ signal to the M2 module. The Initialization of the control-loop is triggered by the edge detection of the SYSREF signal (see Figure 61). The capture is done during the capture window and is repeated at the end of every control loop period until the signal is locked. The SYSREF edge must occur within the capture window.



In this example the SYSREF period is twice the LMFC period (R=2)

Fig 61. Capturing the SYSREF signal

Figure 62 shows an example on how to set up the M1 module.

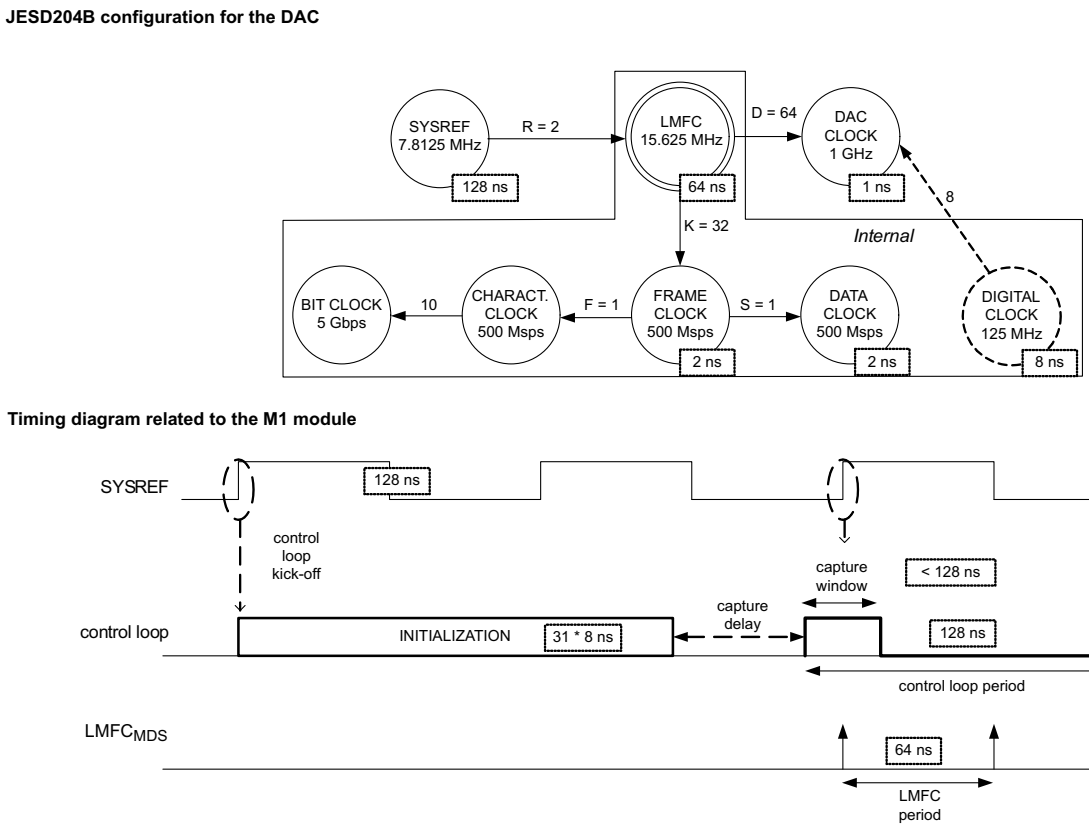


Fig 62. Example of how to set up the M1 module

The DAC165xQ requires the following parameters:

- **LMFC_PERIOD register**:

  Period of the LMFC in digital clock cycles (e.g. 8 × 8 ns)

- **Capture window and control loop period**:

  These are specified using XY_MDS_WIN_HIGH and XY_MDS_WIN_LOW registers (respectively at address 0x0A9/0x2A9/0x4A9 and 0x0A8/0x2A8/0x4A8). They are expressed in digital clock cycles and must be set using the following equations:

$$capture\ window = 2 \times (MDS\_WIN\_HIGH + 1)$$

$$control\ loop\ period = capture\ window + MDS\_WIN\_LOW + 1$$

  Remark: The capture window must be smaller than the SYSREF period.

At the end of the capture process, the $LMFC_{MDS}$ signal is provided to the M2 module and the XY_MDS_LOCK bit of the XY_MDS_STATUS2 status register is set to 1. If the M1 module cannot lock, the MDS_I_BUSY flag of register XY_MDS_STATUS1 is kept high and a mute action can be held (see Section 11.2.4.10).

11.8.3.2 Aligning the LMFCs and the data

Module M2 ensures the phase alignment of the $LMFC_{RCV}$ to the closest $LMFC_{MDS}$ edge. The $LMFC_{RCV}$ is issued from the digital lane processing by analyzing the ILA sequence using the multi-frames /A/ symbols present. The transmitter (TX) is expected to have its self-synchronization process to the global MFC_{SYSTEM}. It generates the ILA sequence based on the

aligned $LMFC_{TX}$. The total latency of the link is compounded of a fixed value (due to PCB traces, devices internal fixed delays, etc.) and a random value (due to elastic buffers, clocks domains interface, etc.). By buffering the data and the $LMFC_{RCV}$ after the initial-lane alignment process, the M2 module is capable to adjust the position of the buffer delay to match the recovered $LMFC_{MDS}$.

Figure 63 shows the alignment process for two links. The two links have two different total latencies but due to the $LMFC_{TX}$ and $LMFC_{MDS}$ phase synchronization to the MFC_{SYSTEM}, the various devices are capable to align to the same MFC_{SYSTEM} edge in a fixed and deterministic way.

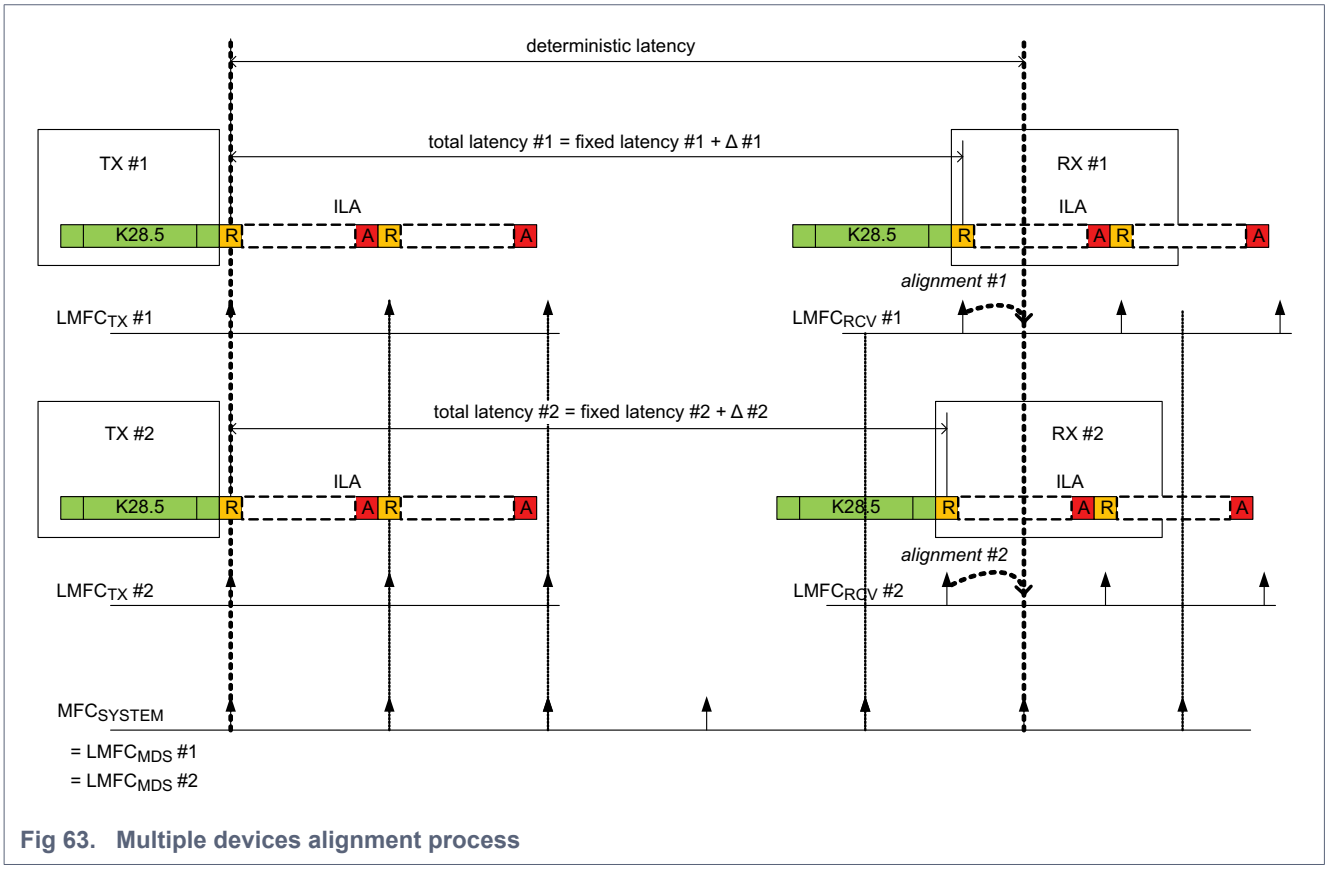


Fig 63. Multiple devices alignment process

Take special care when selecting the MFC_{SYSTEM} period. A longer period is better than a short one. In general, the MFC_{SYSTEM} period must be at least two times the maximum latency between devices to avoid a wrong edge selection as shown in Figure 64.

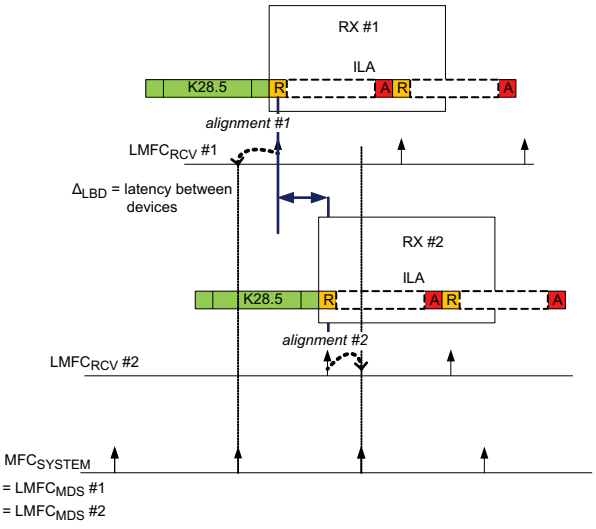


Fig 64. Wrong edge selection

11.8.3.3 Monitoring the MDS process

The buffer adjustment performed using the M1 and M2 modules can be read back using the XY_MDS_ADJDELAY register. Bits 7 to 3 of this register represent the coarse delay expressed in digital clock cycles whereas bits 2 to 0 represent the fine adjustment in DAC clock cycles. The buffer adjustment has a default value of 80h.

MDS_LOCK bit of register XY_MDS_STATUS2 is set to 1 when the MDS process is completed. You can use this bit to check if the device is aligned to the SYSREF.

11.8.3.4 Adding adjustment offset

The DAC165xQ allows adding an offset on top of the automatic adjustment. This is available via register XY_MDS_OFFSET_DLY. The offset range is from −16 to 15 digital clock cycles. This offset value can be set at the start-up time as well as in at later period. This enables compensating a layout error or adding a specific phase to one DAC device.

Another adjustment delay can be set but only after a first automatic alignment using the manual adjustment delay register XY_MDS_MAN_ADJUSTDLY with a resolution of DAC clk.

11.8.3.5 Selecting the SYSREF input port

The DAC165xQ incorporates two SYSREF differential ports: SYSREF_E_P/N (East side of the device) and SYSREF_W_P/N (West side of the device). One of these ports can be selected as the input for the SYSREF signal and will be capture in an asynchronous way.

Remark: *SYSREF signal is only needed during SYNC_Request periods. The signal should/could be switched off later to avoid analog disturbances.*

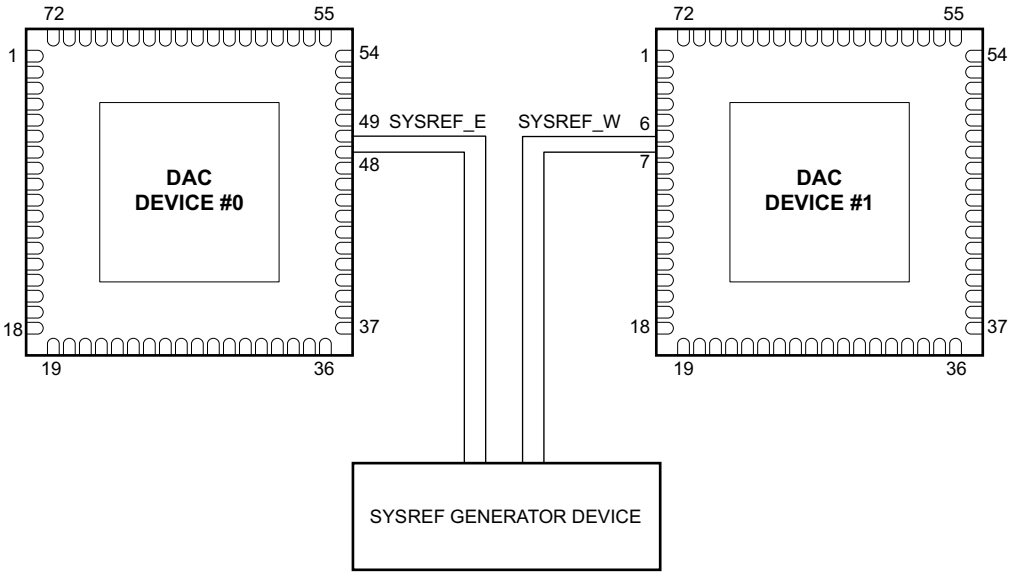


Fig 65. SYSREF differential ports

Register bit XY_MDS_EAST_WEST is used to select between the East port or the West port. Each SYSREF input buffer has an optional internal differential resistor termination of about 100 Ω. This resistor can be enabled with registers MDS_SEL_RT_E and MDS_SEL_RT_W. Polarity could also been switched using MDS_SYSREF_POL_W and MDS_SYSREF_POL_E bits. Please note that only SYSREF_W input support resynchronization mode to clkin using register MDS_IO_CNTRL1 bit MDS-RESYNC_SYSREF.

11.8.3.6 MDS script example

Here are some guidelines to ensure basic correct MDS SPI programming (based on default register settings). This sequence must be applied before DCLK and WCLK resets are released (step 14 in Section 11.2.3.1):

1. Specify the asynchronous mode and the polarity expected for East and West input by asserting the bits of register MDS_IO_CNTRL1.
2. Specify the input to use (XY_MDS_EAST_WEST bit) by asserting MDS_MAIN.
3. Power on the expected SYSREF buffer by setting XY_MDS_IO_PON_E or XY_MDS_IO_PON_W.
4. Specify optional offset delay by programming register XY_MDS_OFFSET_DLY.
5. Specify the MDS_WIN_LOW and MDS_WIN_HIGH registers.
6. Specify the XY_LMFC_PERIOD.

Other advanced settings could be added, refer to the IDT application note about MDS.
Once the device started (after WCLK and DCLK clocks release), the XY_MDS_LOCK bit could be checked to verify that MDS process has worked.

SPI MDS init sequence example:

The following SPI sequence shows the list of commands to be used to start the MDS in LMF421 DLQ configuration, interpolation x2 mode, with PLL on (Fclkin=491.52 MHz Fs=1474.56 MHz). Step 1 to 21 corresponds to standard initialization of the DAC in above configuration. Step 22 ..31 are useful to start the MDS feature. if MDS test is needed in other configurationonly step 1..21 need to be rewrite.

Table 33. SPI MDS start-up sequence

Step	SPI (address, data)	Comment
1	Write(0x0000, 0x99)	Mandatory: configure the SPI mode and apply a reset
ADPLL setting:		
2	Write(0x0029, 0x43)	Mandatory: disable the auto-adpll-su reset
3	Write(0x01C9, 0x01)	Mandatory: postdiv_sel[3:0] (/3) (clkin/(reg.value + 2))
4	Write(0x01C8, 0x06)	Mandatory: prediv_sel[3:0] (491.52 MHz / 8 = 61.44 MHz) (clkin/(reg.value + 2))
5	Write(0x01CC, 0x0F)	Mandatory: program adpll_dco_ctf[7:0]
6	Write(0x01DA, 0x48)	Mandatory: FCW_int[7:0] (DCOfreq = 61.44 x 72 = 4423.68 MHz)
7	Write(0x01AC, 0x3F)	Mandatory: power on I_source, bias and bandgap
8	Write(0x01CA, 0x1C)	Mandatory: reset ADPLL
9	Write(0x01CA, 0xDC)	Mandatory: release ADPLL reset , select temperature drift compensation
10	Write(0x0021, 0x6F)	Mandatory: DCSMU wil start ADPLL in BB mode , auto lock detection
JESD204B setting:		
11	Write(0x002B, 0x00)	Mandatory: cdi_cd as master, cdi_mode_cd = x2, cdi_ab as master, cdi_mode_ab = x2
12	Write(0x002C, 0x10)	Mandatory: mds_select_E,syncb_sel_E[1:0],'-',mds_select_W,syncb_sel_w[1:0]
13	Write(0x01AD, 0x02)	Mandatory: WCLK div = 1/4 (M/(L*Inter) = 2/(4*2))
14	Write(0x0460, 0x01)	Mandatory: interpolation x2
15	Write(0x04C7, 0x62)	Mandatory: independant ILA,sel_ila[1:0],sel_lock[2:0],lane_syn,en_scr
16	Write(0x00CE, 0xD2)	Optional: reswap lanes (0 1 2 3)
17	Write(0x02CE, 0x1B)	Optional: reswap lanes (3 0 2 1)
18	Write(0x04CD, 0x0F)	Optional: inverse polatity lane 2/3
19	Write(0x04DE, 0x91)	Mandatory: LMF=421
20	Write(0x0480, 0x90)	Optional: enable auto mute
21	Write(0x0560, 0x03)	Mandatory: Enable JESD204B Rx_Phy HS_REF
MDS setting:		
22	Write(0x01B7, 0x90)	Mandatory: power on MDS_EAST buffer and enabled internal termination
23	Write(0x01B8, 0x05)	Mandatory: SYSREF_E polarity not inverted, SYSREF_W polarity not inverted
24	Write(0x04A0, 0xCD)	Mandatory: equation check '11', MDS east input selected, mode JESD204B-subclass1
25	Write(0x00A1, 0x05)	Mandatory: AB path as master
26	Write(0x02A1, 0x04)	Mandatory: CD path will use reference from AB
27	Write(0x04A8, 0x19)	Mandatory: MDS_WIN_PERIOD_A, SYSREF sub-sampled by 4
28	Write(0x04A9, 0x02)	Mandatory: MDS_WIN_PERIOD_B
29	Write(0x04AA, 0x08)	Mandatory: LMFC_PERIOD
30	Write(0x04AB, 0x06)	Mandatory: LMFC_PRESET, optional to align 0xBC to 0x04 (= LMFC_PERIOD / 2)
31	Write(0x0020, 0x20)	Mandatory: reinit_mode[2:0],'-'force_rst_(pclk,dclk,wclk)

11.9 Interrupts

In some cases it may be useful if the host-controller is notified that a certain internal event has taken place by means of an interrupt. The DAC165xQ includes a simple interrupt (INTR) controller for this purpose.

The INTR-signal can be made available on one of the I/O pins. The polarity is programmable (see section Section 11.9.7).

11.9.1 Events monitored

The DAC165xQ monitors various internal events and indicates their occurrence in the XY_INTR_FLAGS_0 and XY_INTR_FLAGS_1 registers. The following event can be observed:

- XY_INTR_DLP:

  Digital Lane Processing (DLP) has its own interrupt controller. The result of this slave controller is provided to the main interrupt controller through the XY_INTR_DLP bit.
- XY_MDS_BUSY and $\overline{\text{XY\_MDS\_BUSY}}$:

  Refer to the activity of the MDS controller. During the synchronization phase, the XY_MDS_BUSY signal is high, and becomes low once finished.
  - XY_MDS_BUSY reflects the start of the activity of the MDS controller
  - $\overline{\text{XY\_MDS\_BUSY}}$ reflects the end of the activity of the MDS controller
- XY_TEMP_ALARM:

  Indicates that the temperature measured by the on-chip temperature sensor exceeds the threshold temperature (see Section 11.7).
- XY_CLIP_DET_OR:

  Indicates that one of the level detectors is enabled.
- XY_CA_ERR:

  Indicates a DLP clock error.
- XY_CLK_MON:

  Indicates a CDI clock error.
- XY_MON_DCLK_ERR:

  Indicates a drift on the DCLK as specified by register XY_INTR_MON_DCLK_RANGE.
- XY_ERR_RPT_FLAG:

  Indicates the transmission of error reporting via the SYNCB interface.
- XY_MC_ALARM:

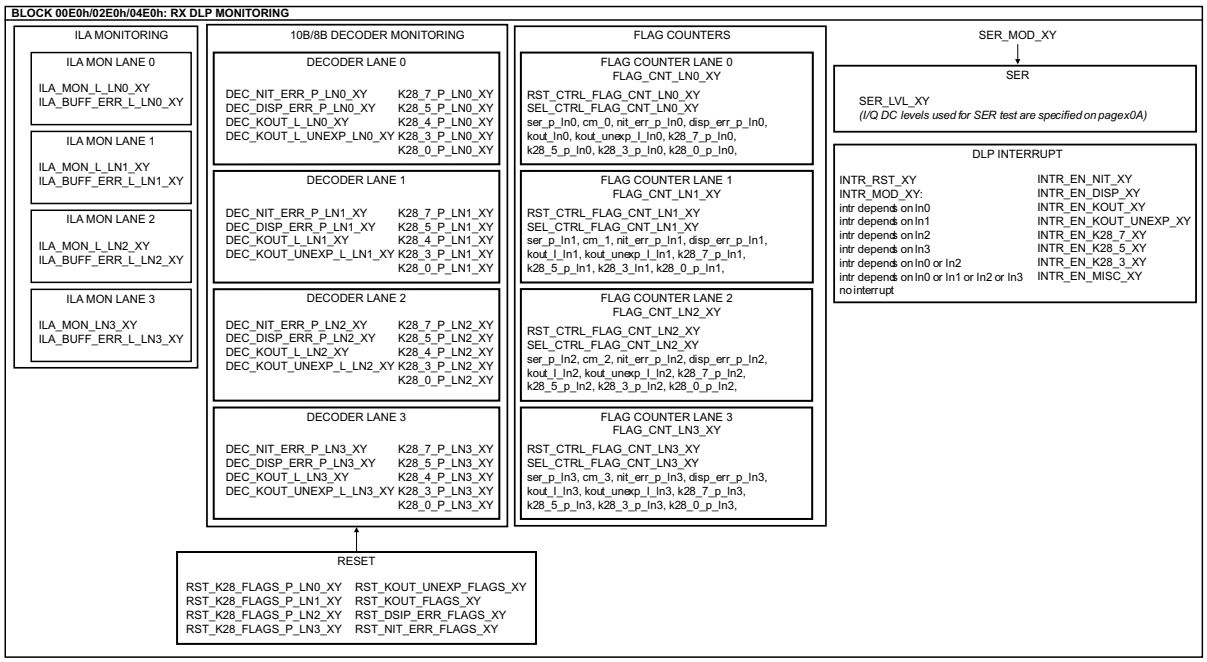
  Indicates when an auto-mute event occurs (see Section 11.2.4.10).

11.9.2 Enabling interrupts

An indication of an 0→1 transition of the corresponding monitor- or error indicator activates the INTR-signal can be given using the XY_INTR_ENA_0 and XY_INTR_ENA_1 registers. The XY_INTR_FLAGS_0 and XY_INTR_FLAGS_1 registers indicate which of the selected events has invoked the interrupt. When bit XY_INTR_CLEAR is set to 1 the flags and the INTR-signal are reinitialized.

11.9.3 Digital Lane Processing (DLP) interrupt controller

The DLP has its own interrupt controller that reports to the main interrupt controller. This DLP interrupt controller is managed from the SPI registers of block x00E0/x02E/0x04E0 (see Figure 66).



Block 00E0h = DAC A/B

Block 02E0h = DAC C/D

Block 04E0h = All DACs

Fig 66. Digital lane processing monitoring

As this interrupt controller is dedicated to the JESD204B serial interface the XY_INTR_MODE bits must be specified according to the LMF configuration used in the system.

Table 34. INTR_MODE settings

XY_INTR_MODE	Interrupt setting[1]	Nominal LMF use[2]
000	DLP interrupt depends on lane 0	124
001	DLP interrupt depends on lane 1	124
010	DLP interrupt depends on lane 2	124
011	DLP interrupt depends on lane 3	124
100	DLP interrupt depends on lane 0 or lane 2	222
101	DLP interrupt depends on lane 0 or lane 1 or lane 2 or lane 3	421 / 422
110	Hold_flagcnt[3]	-
111	no interrupt	-

[1]The lane numbering refers to the logical lanes (see Section 11.9.4).

[2]Any mode can also be used for debug purposes.

[3]The "FLAG_CNT" feature is explained in Section 11.9.6.1.

Register XY_INTR_DLP is reinitialized when the bit XY_DBG_INTR_CLEAR control is set to logic 1.

The DLP events that can be monitored with the interrupt controller are programmable via register XY_INTR_ENA0. Those events are related to the lanes specified by the XY_INTR_MOD bits register. Interrupt can be enabled by the following bits:

- XY_INTR_ENA_NIT: enables Not-In-Table (NIT) error on one of the lanes

- XY_INTR_ENA_DISP: enables disparity error on one of the lanes
- XY_INTR_ENA_KOUT: K enables detection of control characters on one of the lanes
- XY_INTR_ENA_KOUT_UNEXP: enables detection of unexpected K control character on one of the lanes
- XY_INTR_ENA_K28_7: enables detection of K28.7 symbol on one of the lanes
- XY_INTR_ENA_K28_5: enables detection of K28.5 symbol on one of the lanes
- XY_INTR_ENA_K28_3: enables detection of K28.3 symbol on one of the lanes
- XY_INTR_ENA_MISC: enables detection of event related to the XY_INTR_MISC_ENA register.

  Register XY_INTR_MISC_ENA refers to two kinds of events, mainly for debug purposes:
  - Lane x has reached the CS_INIT state
  - An error has occurred in the ILA alignment process on lane x

When register XY_INTR_DLP is invoked, the “FLAGS” registers must be read to determine which event has occurred:

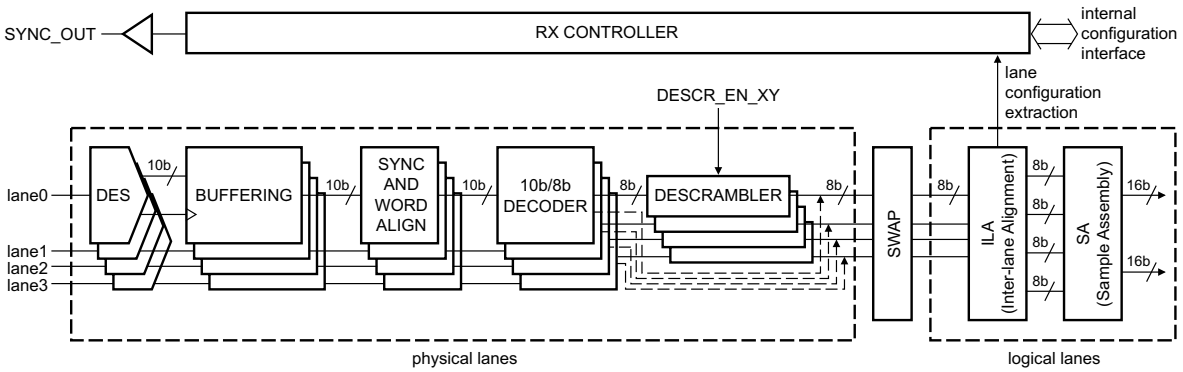
- An XY_INTR_ENA_NIT event is related to the XY_DEC_NIT_ERR_P_LN x bits of register XY_DEC_FLAGS.
- An XY_INTR_ENA_DISP event is related to the XY_DEC_DISP_ERR_P_LN x bits of register XY_DEC_FLAGS.
- An XY_INTR_ENA_KOUT event is related to the XY_DEC_KOUT_P_LN x bits of register XY_KOUT_FLAG.
- An XY_INTR_ENA_KOUT_UNEXP event is related to the XY_DEC_KOUT_UNEXP_LN x bits of register XY_KOUT_UNEXPTED_FLAG.
- An XY_INTR_ENA_K28_7 event is related to the XY_K28_7_P_LN x bits of register XY_K28_LNx_FLAG.
- An XY_INTR_ENA_K28_5 event is related to the XY_K28_5_P_LN x bits of register XY_K28_LNx_FLAG.
- An XY_INTR_ENA_K28_3 event is related to the XY_K28_3_P_LN x bits of register XY_K28_LNx_FLAG.
- An XY_INTR_ENA_MISC event is related to the XY_CS_STATE_P_LN x bits of register XY_CS_STATE_P_LNX and the XY_ILA_BUF_ERR_L_LN x bits of register XY_ILA_BUF_ERR register.

All flag bits can be reset using register XY_MON_FLAGS_RESET.

Remark: Checking the XY_CS_STATE_P_LNX = CS_INIT = 00 interrupts allows to indirectly test the SYNC_REQUEST of the DAC. This feature can help if one does not want to use the differential SYNCB pins.

11.9.4 JESD204B physical and logical lanes

The DAC165xQ integrates a JESD204B serial interface with a high flexibility of configuration.



The descrambler can be enabled or disabled.

Fig 67. JESD204B receiver

Because of various implementations for JESD204B transmitter devices, a flexible configuration of the physical lanes is required. This configuration allows the lane polarity to invert individually and to arbitrary swap the lane order. Identifying the lane numbers can be confusing because of the lane swapping. Two terms, physical and logical, are used in this document to explicitly identify the lanes.

Physical lanes:

The DAC165xQ integrates two times four JESD204B serial receivers that are referenced via the pinning information (see Figure 2).

- DAC A/B physical lane 0 refers to the signal coming from pins VIN_AB_P0 and VIN_AB_N0
- DAC A/B physical lane 1 refers to the signal coming from pins VIN_AB_P1 and VIN_AB_N1
- DAC A/B physical lane 2 refers to the signal coming from pins VIN_AB_P2 and VIN_AB_N2
- DAC A/B physical lane 3 refers to the signal coming from pins VIN_AB_P3 and VIN_AB_N3
- DAC C/D physical lane 0 refers to the signal coming from pins VIN_CD_P0 and VIN_CD_N0
- DAC C/D physical lane 1 refers to the signal coming from pins VIN_CD_P1 and VIN_CD_N1
- DAC C/D physical lane 2 refers to the signal coming from pins VIN_CD_P2 and VIN_CD_N2
- DAC C/D physical lane 3 refers to the signal coming from pins VIN_CD_P3 and VIN_CD_N3

Logical lanes:

The DAC165xQ incorporates a Swap lanes module (see Figure 67) that allows a remapping of the lane numbers to be compatible with the system implementation.

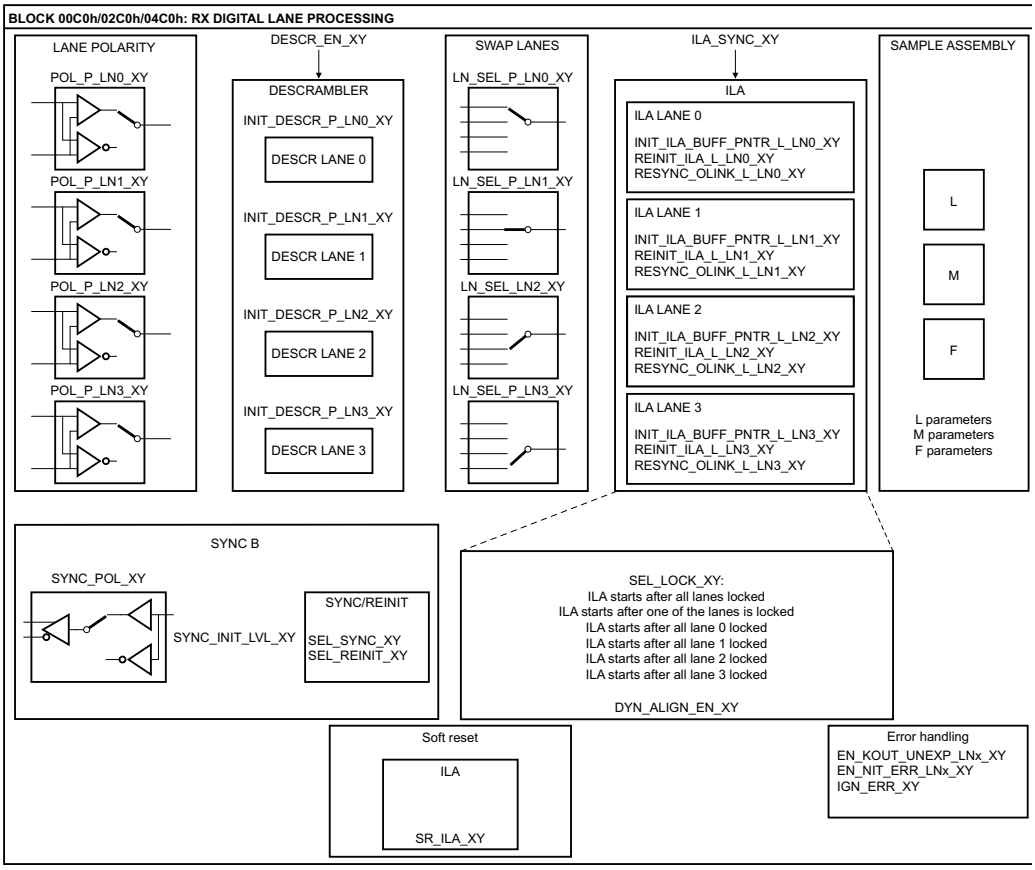
- DAC A/B logical lane 0 refers to the lane specified with the XY_LANE_SEL_L_LN#0 bits in register XY_LANE_SELECT (adress = 0x0CE).
- DAC A/B logical lane 1 refers to the lane specified with the XY_LANE_SEL_L_LN#1 bits in register XY_LANE_SELECT (adress = 0x0CE).
- DAC A/B logical lane 2 refers to the lane specified with the XY_LANE_SEL_L_LN#2 bits in register XY_LANE_SELECT (adress = 0x0CE).
- DAC A/B logical lane 3 refers to the lane specified with the XY_LANE_SEL_L_LN#3 bits in register XY_LANE_SELECT (adress = 0x0CE).
- DAC C/D logical lane 0 refers to the lane specified with the XY_LANE_SEL_L_LN#0 bits in register XY_LANE_SELECT (adress = 0x2CE).
- DAC C/D logical lane 1 refers to the lane specified with the XY_LANE_SEL_L_LN#1 bits in register XY_LANE_SELECT (adress = 0x2CE).
- DAC C/D logical lane 2 refers to the lane specified with the XY_LANE_SEL_L_LN#2 bits in register XY_LANE_SELECT (adress = 0x2CE).
- DAC C/D logical lane 3 refers to the lane specified with the XY_LANE_SEL_L_LN#3 bits in register XY_LANE_SELECT (adress = 0x2CE).

The following naming convention is used to distinguish between the physical lanes and the logical lanes in the SPI registers: “P_LNx” is used to identify the physical lanes. “L_LNx” is used to identify the logical lanes. “x” stands for the lane number in both cases.

11.9.5 RX Digital Lane Processing (DLP)

Digital lane processing is the module containing all JESD204B interface controls except the PHY deserializer.

Figure 68 shows the registers for the configuration of the digital lane processing.



Block 00C0h = DAC A/B
Block 02C0h = DAC C/D
Block 04C0h = All DACs

Fig 68. RX digital lane processing

11.9.5.1 Lane polarity

Each physical lane polarity can be individually inverted with the XY_POL_P_LN x bits of register XY_LANE_POLARITY. Using this feature transforms the 10 bits from ABCDEFGHIJ to $\overline{\text{ABCDEFGHIJ}}$.

11.9.5.2 Scrambling

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial $1 + x^{14} + x^{15}$. From the JESD204B specification, the scrambling/descrambling process only occurs on the user data, not on the code group synchronization or the ILA sequence. After two received bytes, the descrambler is correctly set up to decode the data in the proper way. However, if the initial state of the descrambler bits is set incorrectly, the two first decoded bytes are decoded incorrectly. The JESD204B specification proposes an initial state for both scrambler and descrambler to avoid this.

Using registers XY_INIT_DESCR_P_LN0 x any kind of intitial state can be set in the DAC165xQ. The descrambling process starts when the ILA sequence has finished. This process can be turned off by deasserting bit XY_EN_SCR in register XY_ILA_CNTRL.

The first samples cannot be sent to the DSP using the XY_FORCE_1ST_SMPL_LOW bits of register XY_ALIGN_CNTRL. This avoids the use of the two incorrectly decoded samples.

11.9.5.3 Lane swapping and selection

If the physical lanes do not match with the ordering of the transmitter lanes, they can be reordered using the lane swapping module. As the DAC165xQ allows various LMF configurations, it is important that the lane swapping respects the following reordering constraints linked to the L value (see Table 35).

Table 35. Logical lanes versus L values

L value		Logical lanes used for the Sample assembly module
Binary	Decimal	
DAC A/B		
100	4	logical lane 0
		logical lane 1
		logical lane 2
		logical lane 3
010	2	logical lane 0
		logical lane 2
001	1	logical lane 0
DAC C/D		
100	4	logical lane 0
		logical lane 1
		logical lane 2
		logical lane 3
010	2	logical lane 0
		logical lane 2
001	1	logical lane 0

The selection of the logical lanes can be is specified by the XY_LANE_SEL_L_LN x bits of register XY_LANE_SELECT.

Table 36 shows the possible choices regarding the value of the L parameter.

Table 36. Lane mapping between Logical and Physical lanes regarding the L value

L	4	2	1
DAC A/B or DAC C/D			
logical lane 0	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3
logical lane 1	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used	not used
logical lane 2	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used
logical lane 3	physical lane 0 or physical lane 1 or physical lane 2 or physical lane 3	not used	not used

11.9.5.4 Word locking and Code Group Synchronization (CGS)

When the bits are received from the RX physical layer, DLP has to identify the MSB and LSB boundaries of the 10-bit codes from the bitstream. This can be monitored using the XY_LOCK_CNT_MON_P_LN01 and XY_LOCK_CNT_MON_P_LN23 registers.

When all lanes are locked, the values of the registers are stable and the code group synchronization process can start. This process is described by the JESD204B specification and is represented by the state machine shown in Figure 69.

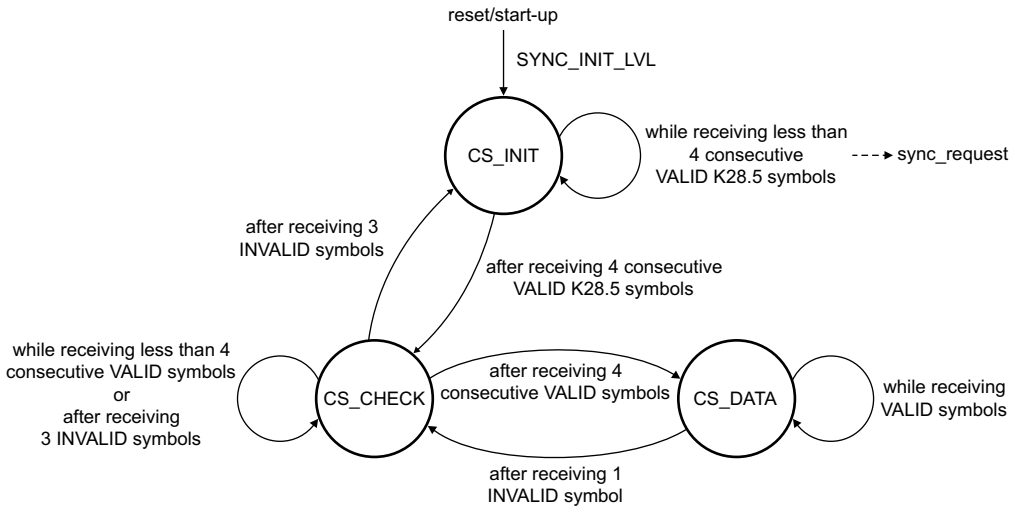


Fig 69. Code group synchronization

The CGS states of each lane can be monitored using the XY_CS_STATE_P_LN x bits of register XY_CS_STATE_P_LNX. The definition of each state can be found in Table 37.

Table 37. Code group synchronization state machine

CSYNC_STATE_P_LNx_XY[1:0]	Name	Definition
00	CS_INIT	looking for K28_5 (/K/) symbol
01	CS_CHECK	four consecutive K28_5 (/K/) symbols have been received
10	CS_DATA	code group synchronization achieved

11.9.5.5 SYNC configuration

The SYNC signal is the feedback signal that is sent to the transmitter device to ensure the JESD204B link synchronization. When one lane are in CS_INIT state a sync_request is sent to the SYNC buffer.

- in DLQ (Dual Link Quad) configuration the two internal dual DAC run independently. So two SYNC signals have to be output by the DAC165xQ device. SYNCB_SELECT_E[1:0] bit of register SRC_SELECT_CNTRL register enables to select which SYNC signal (from data path AB or from data path CD) will be output on pins SYNCB_E_P/N. SYNCB_SELECT_W[1:0] bit of register SRC_SELECT_CNTRL register enables to select which SYNC signal (from data path AB or from data path CD) will be output on pins SYNCB_W_P/N.
- in SLQ (Single Link Quad) configuration the two internal dual DAC are synchronized together. So only one SYNC signal need to be output by the DAC165xQ device. as previously this SYNC signal could be output on either pins SYNCB_E_P/N or pins SYNCB_W_P/N using SRC_SELECT_CNTRL register.

The polarity of SYNC signal is controlled by bit XY_SYNC_POL of register XY_LANE_POLARITY. By default the synchronization request is active low. The synchronization request signal can be specified by bits XY_SEL_SYNC[2:0] of register XY_SYNCOUT_MODE. Bit XY_SYNC_INIT_LEVEL of register XY_SYNCOUT_MODE only specifies the state of the sync_request signal after resetting the CGS state machine (at start-up time or after device reset only). Detail XY_SEL_SYNC[2:0] configuration is presented in Table 38 .

Table 38. Sync_request control

XY_SEL_SYNC[2:0]	Description
000	sync_request active when state machine of one of the lanes is in CS_INIT mode (default)
001	sync_request active when state machine of all lanes is in CS_INIT mode
010	sync_request active when state machine of lane 0 is in CS_INIT mode
011	sync_request active when state machine of lane 1 is in CS_INIT mode
100	sync_request active when state machine of lane 2 is in CS_INIT mode
101	sync_request active when state machine of lane 3 is in CS_INIT mode
110	sync_request fixed to 1
111	sync_request fixed to 0

11.9.5.6 SYNC common mode voltage configuration

The SYNC output common mode is programmable by setting the register XY_SYNC_SET_VCM[2:0]. The final value depends on the voltage provided on VDDJ_SO. The recommended value depends of the VDDJ_SO voltage.

Table 39. SYNC output common mode voltage

XY_SYNC_SET_VCM[2:0]	VCM general formula	VCM when VDDJ_so=1.8V	VCM when VDDJ_so=1.2V	Remark
000	VDDJ_SO-0.8	1.0V	0.4V	
001	VDDJ_SO-0.7	1.1V	0.5V	
010	VDDJ_SO-0.6	**1.2V**	0.6V	**recommended when VDDJ_so=1.8v**
011	VDDJ_SO-0.5	1.3V	0.7V	
100	VDDJ_SO-0.4	1.4V	**0.8V**	**recommended when VDDJ_so=1.2V**
101	VDDJ_SO-0.3	1.5V	0.9V	
110	VDDJ_SO-0.2	1.6V	1.0V	
111	VDDJ_SO-0.1	1.7V	1.1V	

11.9.5.7 SYNC output swing configuration

The SYNC output swing is programmable by setting the register XY_SYNC_SET_LEVEL[2:0]. The recommended value is b100.

Table 40. SYNC output swing voltage

XY_SYNC_SET_LEVEL[2:0]	Single ended value	Differential value
000	0.05V	0.10V
000	0.10V	0.20V
010	0.15V	0.30V
011	0.20V	0.40V
100	**0.30V**	**0.60V**
101	0.40V	0.80V
110	0.50V	1.00V
111	0.60V	1.20V

11.9.5.8 Initial-lane alignment

This module handles the alignment of the logical lanes based on the ILA sequence described in the JESD204B specification. Inter-lane alignment starts when all lanes are locked and at reception of the first non-K28.5 (or /K/) symbol.

During the ILA sequence, the K28.3 (/A/ symbol) is used to align the data streams. During this sequence, the length (K) of the multi-frame is measured. This value is used by the lane monitoring and correction process. The value is also used for the MDS circuitry, where the SYSREF signal is expected to be a multiplication of the multi-frame length (K) in the JESD204B specification.

During the second multi-frame, the JESD204B configuration data of physical lane 0 is stored in register XY_P_LN0_CFG_0 to XY_P_LN0_CFG_13 (similarly register XY_LNx_CFG_0 to XY_LNx_CFG_13 for lane x) (see Figure 70). The DAC165xQ does not do anything with these configuration data. They are only made available for the host controller.

BLOCK nnn0h: JESD204 READ CONFIGURATION (DAC X/Y)

JESD204 CONFIGURATION

CONFIG 0	P_LN_DID	
CONFIG 1	P_LN_ADJ_CNT	P_LN_BID
CONFIG 2	P_LN_ADJ_DIR P_LN_ADJ_PH	P_LN_LID
CONFIG 3	P_LN_SCR	P_LN_L
CONFIG 4	P_LN_F	
CONFIG 5		P_LN_K
CONFIG 6	P_LN_M	
CONFIG 7	P_LN_CS	P_LN_N
CONFIG 8	P_LN_SBCLSS_VS	P_LN_N'
CONFIG 9	P_LN_JESD_VS	P_LN_S
CONFIG 10	P_LN_HD	P_LN_CF
CONFIG 11	P_LN_RES1	
CONFIG 12	P_LN_RES2	
CONFIG 13	P_LN_FCHK	

Fig 70. JESD204 read configuration for physical lanes overview

Table 41. Overview of generic parts of register map addresses

	DAC A/B	DAC C/D
lane 0	0x120 to 0x12D	0x320 to 0x32D
lane 1	0x130 to 0x13D	0x330 to 0x33D
lane 2	0x140 to 0x14D	0x340 to 0x34D
lane 3	0x150 to 0x15D	0x350 to 0x35D

The ILA module uses a 16-bit buffer for each lane. The first /A/ symbol received over the lanes is used as reference. The /A/ symbols of the other lanes, which are received later, are compared to the first one to be all aligned. The initial location of the symbols is predefined by the XY_INIT_ILA_BUFPTR_L_LN x registers. The alignment can be monitored with the XY_ILA_MON_L_LN x registers. If the lane difference is too great, a buffer out-of-range error occurs, which can be monitored with bits XY_ILA_BUF_ERR_L_LN x registers. In this specific case, a reinitialization of the full link can be requested by setting the XY_REINIT_ILA_L_LN x bits of register XY_REINIT_CNTRL.

The JESD204B specification also mentions a dynamic realignment mode where a monitoring process is checking the /A/-symbol location. This can realign the data stream if two successive /A/ symbols are found at the same new position. By default this monitoring and correction process is disabled to avoid any moving latency over the link, but one can enable the feature by setting the XY_DYN_ALIGN_ENA bit of register XY_ALIGN_CNTRL.

11.9.5.9 Character replacement

Character replacement, as specified by the JESD204B specification, can occur at the end of the frame (K28.7 or /F/ symbol) or at the end of the multi-frame (K28.3 or /A/ symbol). By default this feature is enabled, but it can be disabled using bit XY_FRAME_ALIGN_ENA of the XY_ALIGN_CNTRL register.

Remark: The DAC165xQ can handle multi-frame length values (K) between ceil(17 / F) and 32 but with the restriction that the number of octets in a multi-frame must always be even. This implies that if F = 1, a value of K = 17 is not allowed. When F = 1 only even values > 17 are allowed. Working with F = 1 and K = 17 often implies that the character replacement process is not reliable.

11.9.5.10 Sample assembly

Sample assembly handles the assembly of the data based on the LMF parameters described by register XY_LMF_CNTRL. each dual DAC of DAC165xQ need to be programmed independently. this means that if LMF841 is targeted ,in fact each dual DAC instance need to be programmed in LMF421 and in parallel SLQ (Single Link Quad) mode need to be selected.The following configurations are supported:

- LMF-S = 421-1
- LMF-S = 422-2
- LMF-S = 222-1
- LMF-S = 124-1

Sample assembly is based on the logical lanes definition when updating the L value.

11.9.5.11 Resynchronization over links

The DAC165xQ recognizes a K28.5 (/K/) symbols sequence coming over its lanes. This identification allows resynchronization of the device if the XY_RESYNC_OLINK_P_LN x bits of register XY_REINIT_CNTRL are set correctly.

11.9.5.12 Symbols detection monitoring and error handling

The DLP decodes the 10-bit words to 8-bit words. The decoding table is specified in the IEEE 802.3-2005 specification. During decoding, the disparity is calculated according to the disparity rules mentioned in the same specification. The JESD204B specification also defines the following definitions:

- VALID:

  The code group is found in the column of the 10b/8b decoding tables according to the current running disparity.
- DISPARITY ERROR:

  The received code group exists in the 10b/8b decoding table, but is not found in the correct column according to the current running disparity.
- NOT-IN-TABLE (NIT) ERROR:

  The received code group is not found in the 10b/8b decoding table of either disparity.
- INVALID:

  A code group that either shows a disparity error or that does not exist in the 10b/8b decoding table.

Remark: The 8b/10b decoder only provides reliable information in the CSYNC_CHCK and CSYNC_DATA states. During CSYNC_INIT state, the DLP is "hunting" for the correct position of the K28.5 (/K/) symbols in the received bitstream. Therefore the DISPARITY ERROR/NOT-IN-TABLE/ INVALID flags are not yet consistent and are not be used in the internal monitoring.

The Not-In-Table error (NIT) and Disparity error (DISP) can be monitored using the DEC_NIT_ERR_P_LNx_XY and XY_DEC_DISP_ERR_P_LN x bits of register XY_DEC_FLAGS. Both are considered invalid, but the DAC165xQ has some flexibility in this definition. The specified invalid errors can also be totally ignored by setting the bit XY_ IGNORE_ERR of register XY_ERR_HANDLING_1. This specific mode is designed for debug purposes only, especially when sample error measurement needs to be executed.

The VALID/INVALID status of the decoded word can trigger the MUTE feature using the XY_IGNORE_DATA_V_IQ bits of register XY_MUTE_CNTRL_2 (see Section 11.2.4.10).

The following comma symbols are detected during data transmission irrespective of the running disparity:

/K/ = K28.5

/F/ = K28.7

/A/ = K28.3

/R/ = K28.0

/Q/ = K28.4

Their single detection is monitored in registers XY_KOUT_FLAG and XY_K28_LN x _FLAG.

During the data transmission phase, only K28.3 (/A/) and K28.7 (/F/) symbols are expected. Sometimes (e.g. wrong bit transmission), a code group is interpreted as a K character that is not K28.3 or K28.7. If this occurs a KOUT_UNEXP flag is asserted that can be read using the XY_DEC_KOUT_UNEXP_LN x bits of register XY_KOUT_UNEXPECTED_FLAG.

All the previous flags can be reset using the XY_MON_FLAGS_RESET register. Detection of them can also assert the DLP interrupt (see Section 11.9.3).

11.9.6 Monitoring and test modes

The DAC165xQ embeds various monitoring and test modes that are useful during the prototyping phase of a system.

Remark: The test capability linked to observing specific characters, errors or state machine statuses is not reviewed in this section. It is up to the reader to define specific modes based on the DAC165xQ capability.

11.9.6.1 Flag counters

Due to the high data rate of the JESD204B serial interface, it is hard to monitor events that occur on the lanes in real time. Four multi-purpose counters have been added to the design to help this monitoring. Each counter is 16 bits wide and is linked to one lane. It increments its value each time a specific event occurs. These flags counters can be read using the XY_FLAG_CNT_LSB_LN x and XY_FLAG_CNT_MSB_LN x registers and reset using the XY_CNTRL_FLAGCNT_LN x registers. The flag counters can also be reset automatically when DLP is reset by setting the XY_AUTO_RST_FLAGCNTS bit of register XY_MISC_FLAG_CNTRL to logic 1.

The specification of the event that increments the counter is done by setting the XY_SEL_CFC_LN x bits of the XY_CNTRL_FLAGCNT_LN x registers to one of the sources described in Table 42.

Table 42. Counter source
Default settings are shown highlighted.

XY_SEL_CFC_LN x[2:0]	Source
000	not-in-table error
001	disparity error
010	K symbol not found
011	unexpected K symbol found
100	K28_7 (/F/) symbol found

Table 42. Counter source
Default settings are shown highlighted.

XY_SEL_CFC_LN x[2:0]	Source
101	**K28_5 (/K/) symbol found**
110	K28_3 (/A/) symbol found
111	K28_0 (/R/) symbol found

When the counter is reaching its maximum value (0xFFFF), this value is held until the next counter reset. Bit XY_FLAGCNT_HOLD_MODE of XY_MISC_FLAG_CNTRL register gives two options for when a counter reaches the maximum value.

Table 43. XY_FLAGCNT_HOLD_MODE options
Default settings are shown highlighted.

XY_FLAGCNT_HOLD_MODE	Option
0	**All counters are independent. Each counter continues its own counting.**
1	All counters are linked. When one counter reached the maximum value and stops, all other counters stop as well.

When the counters are stopped, an interrupt can be activated (see Section 11.9.3).

This feature makes it possible to, for instance, analyze the occurrence of character replacement or NIT errors.

11.9.6.2 Sample Error Rate (SER)

A sample error rate feature is implemented in the DAC165xQ to analyze the quality of the transmission. Due to the 8b10b encoding, the analysis is done at sample level only and not at bit level. The transmitter sends a constant data over the link and the DAC165xQ compared this received value to the value specified in the XY_BER_LEVEL_P_LN x[15:0] registers. Enable the scrambling on both transmitter and receiver side to add more random effect on the data. The XY_BER_LEVEL_P_LN x[15:0] are specifying a 16-bit value at the lane level, it means the device can be considered as operating in one of two modes:

- F = 2 mode:

  The lane is receiving 16-bit data specified by this register.
- F = 1 mode:

  The lane is receiving alternately 8-bit data specified by MSB and LSB of this register.

The SER mode requires that the DAC is already synchronized (using CGS and ILA sequence). The kick-off of the measurement is done by setting the XY_BER_MOD bit of register XY_DBG_CNTRL. In this mode, the flags counters are used to count the number of 16-bit samples that do not match the XY_BER_LEVEL_P_LN x value. This mode enables the establishing of the sample error rate of each lane.

11.9.6.3 PRBS test

The DAC165xQ embeds PRBS7,PRBS15, PRBS23, and PRBS31 PRBS checkers that are shared for the 4 lanes of each dual DAC.

To test a specific lane, the setting XY_SEL_XBERT_LN[1:0] needs to be set first. Then it is required to disable the restart of the RX PHY due to the error monitoring this is done by setting the register XY_IGNORE_ERR[1:0] to value 3 and XY_REINIT_CNTRL to value x00. After the release of the DCLK and WCLK clocks, the XY_XBERT_CNTRL[2:0] bits must specified to the expected test (PRBS31, 23 , 15, 7) and the XY_CHECK_PRBS bit must be set to the “sync to prbs sequence” mode. Once synchronized, the internal PRBS counter is aligned with the received PRBS sequence. The test starts when the XY_CHECK_PRBS is set to 1 (ie= “check PRBS sequence” mode). The XY_XBERT_CNT[15:0] counter

indicates the number of bits in error. Example of SPI settings (step 1..14 corresponds to standard initialization of the DAC in LMF421 SLQ intx2 , step 20 ..31 are useful to start the device in watchdog disable mode and then define and start PRBS test). if PRBS test is needed in other LMF configuration or in PLL mode only step 1..19 need to be rewrite:

Table 44. SPI PRB7 start-up sequence

Step	SPI (address, data)	Comment
1	Write(0x0000, 0x99)	Mandatory: sequence needed to put the PLL in real low power mode
	Write(0x0020, 0x01)	
	Write(0x0029, 0x43)	
	Write(0x01C8, 0x0F)	
	Write(0x01CA, 0x9C)	
	Write(0x01C0, 0x02)	
	Write(0x01C4, 0x0F)	
	Write(0x01C6, 0x91)	
	Write(0x01C6, 0x90)	
2	Write(0x0000, 0x99)	Mandatory: Configure the SPI mode and apply a reset
3	Write(0x0028, 0x01)	Mandatory: Combine_rx_phy_lock
4	Write(0x002B, 0x04)	Mandatory: sr_cdi,sel_ms,mode_sel[1:0])_cd,(sr_cdi,sel_ms,mode_sel[1:0])_ab
5	Write(0x002C, 0x00)	Mandatory: mds_select_E,syncb_sel_E[1:0],'-',mds_select_W,syncb_sel_w[1:0]
6	Write(0x04C7, 0x82)	Mandatory: comb_ln_ila,sel_ila[1:0],sel_lock[2:0],lane_syn,en_scr
7	Write(0x04CD, 0x00)	Optional: sync_pol,pol_ln[3:0]
8	Write(0x00CE, 0xD2)	Optional: reswap lanes ab (3 0 2 1)
9	Write(0x02CE, 0x1B)	Optional: reswap lanes cd (0 1 2 3)
10	Write(0x04CC, 0x10)	Mandatory: sel_re_init[2:0],combine_ln_sync,sync_ini_lev,sel_sync[2:0]
11	Write(0x04CD, 0x0F)	Optional: inverse polatity lane
12	Write(0x04DE, 0x91)	Mandatory: specify LMF=421
13	Write(0x0560, 0x03)	Mandatory: Enable JESD204B Rx_Phy HS_REF
14	Write(0x0030, 0xFC)	Optional: io_select_0: use to output result on IO pins
15	Write(0x0031, 0xFC)	Optional: io_select_1: use to output result on IO pins
16	Write(0x0032, 0xFD)	Optional: io_select_2: use to output result on IO pins
17	Write(0x0033, 0xFD)	Optional: io_select_3: use to output result on IO pins
18	Write(0x0034, 0xAA)	Optional: io_select_4: use to output result on IO pins
19	Write(0x0035, 0x0A)	Optional: io_ena
20	Write(0x029, 0x03)	Mandatory: watchdog disabled
21	Write(0x002A, 0x00)	Optional: disable pin RF_ENABLE power down
22	Write(0x04DB,0xFF)	Mandatory: disable the error handle
23	Write(0x04DC, 0x00)	Mandatory: prevent restart due to k28.5
24	Write(0x0020, 0x04)	Mandatory: reinit_mode[2:0],'-'force_rst_(pclk,dclk,wclk)
25	Write(0xFFFF, 0xFF)	Wait=255 units time
26	Write(0x0500, 0x01)	Mandatory: reset_xbert_cnt
27	Write(0x0500, 0x0A)	Mandatory: ln0, sync to PRBS, in prbs7
28	Write(0xFFFF, 0xFF)	Wait=255 units time
29	Write(0x0500, 0x2A)	Mandatory: ln0, check PRBS, in prbs7
30	Write(0xFFFF, 0xFF)	Wait BER test time (depending BER test time):

Table 44. SPI PRB7 start-up sequence

Step	SPI (address, data)	Comment
31	Read(0x0104, 0x2A)	read result of PRBS test (LSB bit DAC AB)
32	Read(0x0105, 0x2A)	read result of PRBS test (MSB bit DAC AB)
33	Read(0x0304, 0x2A)	read result of PRBS test (LSB bit DAC CD)
34	Read(0x0305, 0x2A)	read result of PRBS test (MSB bit DAC CD)

11.9.6.4 JTSPAT test

The Jitter Tolerance Scrambled PATtern (JTSPAT) is an 1180-bit pattern intended for receiving jitter tolerance testing for scrambled systems. The JTSPAT test pattern consists of two copies of JSPAT and an additional 18 characters intended to cause extreme late and early phases in the CDR PLL followed by a sequence, which can cause an error (i.e. an isolated bit following a long run). This pattern was developed to stress the receiver within the boundary conditions established by scrambling.

Table 45. Jitter tolerance scrambled pattern symbols sequence [1]

D1.4	D16.2	D24.7	D30.4	D9.6	D10.5
0111010010	0110110101	0011001110	1000011101	1001010110	0101011010
D16.2	D7.7	D24.0	D13.3	D23.4	D13.2
1001000101	1110001110	0011001011	1011000011	0001011101	1011000101
D13.7	D1.4	D7.6	D0.2	D21.5	D22.1
1011001000	0111010010	1110000110	1001110101	1010101010	0110101001
D23.4	D20.0	D27.1	D30.7	D17.7	D4.3
0001011101	0010110100	1101101001	1000011110	1000110001	1101010011
D6.6	D23.5	D7.3	D19.3	D27.5	D19.3
0110010110	0001011010	1110001100	1100101100	110101010	1100100011
D5.3	D22.1	D5.0	D15.5	D24.7	D16.3
1010010011	0110101001	1010010100	0101111010	0011001110	1001001100
D1.2	D23.5	D29.2	D31.1	D10.4	D4.2
0111010101	0001011010	1011100101	0101001001	0101011101	0010100101
D5.5	D10.2	D21.5	D10.2	D21.5	D20.7
1010011010	0101010101	1010101010	0101010101	1010101010	0010110111
D11.7	D20.7	D18.7	D29.0	D16.6	D25.3
1101001000	0010110111	0100110001	1011100100	0110110110	1001100011
D1.0	D18.1	D30.5	D5.2	D21.6	D1.4
1000101011	0100111001	1000011010	1010010101	1010100110	0111010010
D16.2	D24.7	D30.4	D9.6	D10.5	D16.2
0110110101	0011001110	1000011101	1001010110	0101011010	1001000101
D7.7	D24.0	D13.3	D23.4	D13.2	D13.7
1110001110	0011001011	1011000011	001011101	1011000101	1011001000
D1.4	D7.6	D0.2	D21.5	D22.1	D23.4
0111010010	1110000110	1001110101	1010101010	0110101001	0001011101
D20.0	D27.1	D30.7	D17.7	D4.3	D6.6
0010110100	1101101001	1000011110	1000110001	1101010011	0110010110
D23.5	D7.3	D19.3	D27.5	D19.3	D5.3
0001011010	1110001100	1100101100	1101101010	1100100011	1010010011

Table 45. Jitter tolerance scrambled pattern symbols sequence [1]

D22.1 0110101001	D5.0 1010010100	D15.5 0101111010	D24.7 0011001110	D16.3 1001001100	D1.2 0111010101
D23.5 0001011010	D27.3 1101100011	D3.0 1100010100	D3.7 1100011110	D14.7 0111001000	D28.3 0011101100
D30.3 0111100011	D30.3 1000011100	D7.7 1110001110	D7.7 0001110001	D20.7 0010110111	D11.7 1101001000
D20.7 0010110111	D8.7 0100110001	D29.0 1011100100	D16.6 0110110110	D25.3 1001100011	D1.0 1000101011
D18.1 0100111001	D30.5 1000011010	D5.2 1010010101	D21.6 1010100110		

[1] This table must be read, starting from the top, left-to-right first and then line-by-line to follow the sequence.

The DAC165xQ embeds a JTSPAT checker. JTSPAT checker is start in same way than PRBS test using XY_XBERT_CNTRL[2:0]=001.

11.9.6.5 DLP strobe

The data coming out of the ILA module can be sampled by setting the XY_DLPSTROBE bit of register XY_MISC_CNTRL. On each lane two octets are stored, which can be read out through bit XY_LN10_SAMPLE[15:0] (in register XY_LN10_SAMPLE_LSB and XY_LN10_SAMPLE_MSB) and XY_LN32_SAMPLE[15:0] (in register XY_LN32_SAMPLE_LSB and XY_LN32_SAMPLE_MSB). The selection of the lane to read out the data is done by registers XY_LN10_SEL and XY_LN32_SEL.

11.9.7 IO-mux

The DAC165xQ uses four general purpose pins, IO0 IO1, IO2 and IO3. IOs can be configured as an input (x01) or as an output (x00) by setting the IO_ENA bit of register IO_CNTRL.

When acting as an input, the IO1 pin is referred as the RF enable feature (see Section 11.2.6).

When acting as an output, the two IO pins are multiplexed to internal signals that can be useful for debug purposes. Table 46 shows the main configuration when using registers bit IO_SELECT_ x in register IO_MUX_CNTRL x. The definitions of the three registers depend on the "Indicator" and the "Range" values used to specify the signal that is sent through the IOs pins (see Table 46 and Table 47).

Table 46. Definition of IO_SEL registers

Register name	b7	b6	b5	b4	b3	b2	b1	b0
IO_SEL_4	IO3 indicator[1:0]		IO2 indicator[1:0]		IO1 indicator[1:0]		IO0 indicator[1:0]	
IO_SEL_3	IO3 range[7:0]							
IO_SEL_2	IO2 range[7:0]							
IO_SEL_1	IO1 range[7:0]							
IO_SEL_0	IO0 range[7:0]							

Table 47. Output signals for combination of indicators and ranges

Indicator[1:0]	Range[7:0]	Output signal
00	xxxx xxx0	IO0: WCLK
		IO1: DCLK
00	xxxx 0011	synchronization request
10	1111 0010	end of ILA
11	1100 0000	$\overline{\text{interrupt}}$
11	1100 0001	interrupt
11	1111 even	IO0: fixed to logic 1
		IO1: fixed to logic 0
11	1111 odd	IO0: fixed to logic 0
		IO1: fixed to logic 1

11.10 JESD204B PHY receiver

Each JESD204B lane owns its own physical de-serializer (RX PHY) that provides the 10-bit data stream to the DLP module. The DAC165xQ provide various control features of the RX PHY, like the equalizer, the common-mode voltage and the resistor termination.

Remark: Most of the main controls (power on/off, PLL clock dividers, etc.) are automatically set while specifying the LMF mode (see Section 11.9.5.10) and/or by the POFF_RX[7:0] and MAINCONTROL registers.

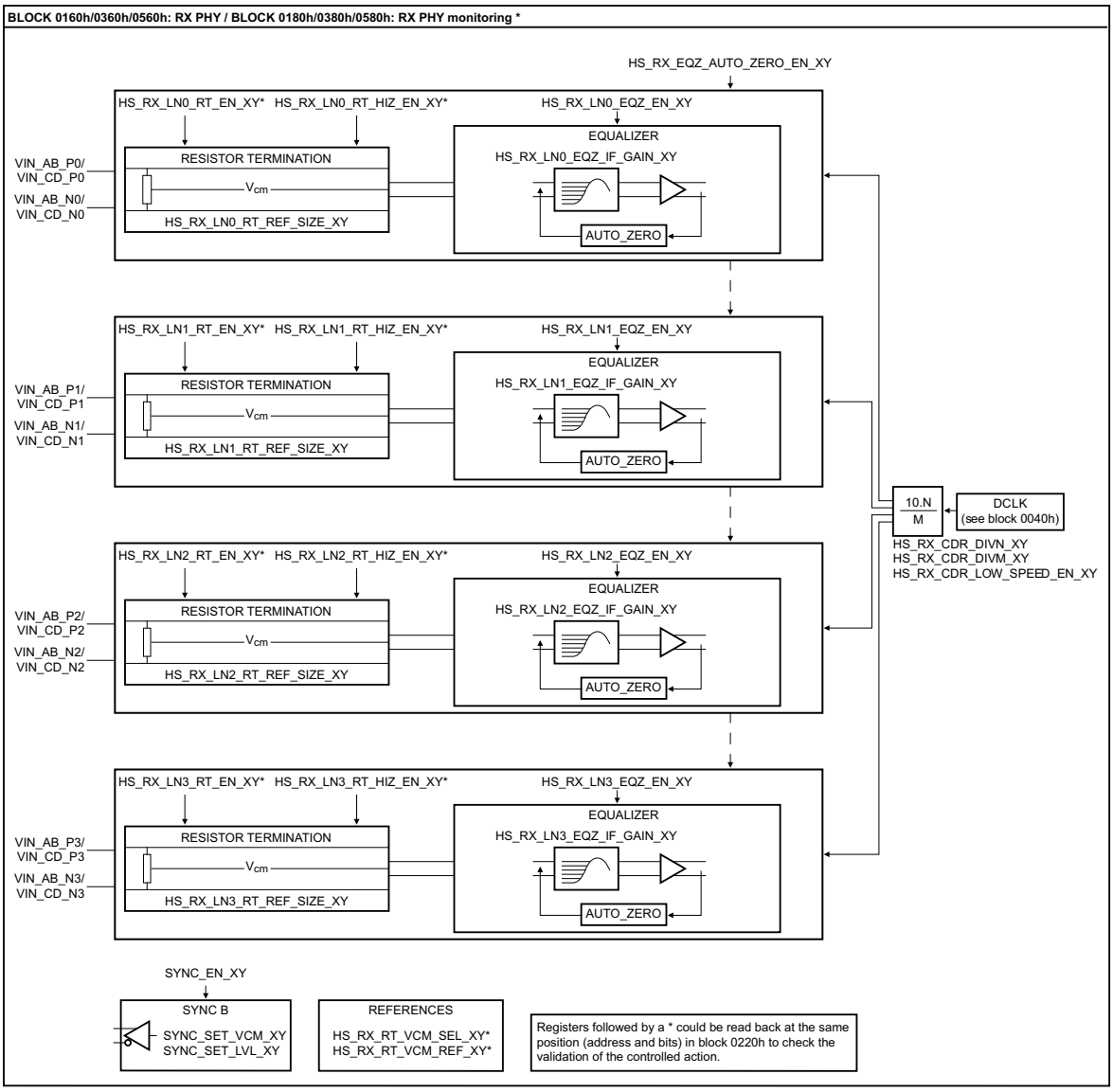


Fig 71. RX PHY control overview

11.10.1 Lane input

Each lane is Current Mode Logic (CML) compliant.

Rx lanes need to be connected to FPGA Tx using AC-coupling. The DAC165xQ do not need on PCB external termination: lane's terminations are already included.

11.10.2 Equalizer

The lane 0 of DAC165xQ embeds an internal equalizer controlled by bits XY_HS_RX_0_EQ_IF_GAIN[2:0] (similarly, bits XY_HS_RX_n_EQ_IF_GAIN[2:0] controls lane n). This improves the interference robustness between signals by amplifying the high-frequency jumps in the data conserving the energy of the low-frequencies ones. The equalizer can be programmed depending on the quality of the channel used (PCB traces/layout, connectors, etc.). The total Equalizer gain is defined in Table 48 and Figure 72.

Table 48. XY_HS_RX_ n _EQ_IF_GAIN Equalizer gain

IF_GAIN	Equalizer Gain (dB)
000	0.0
001	0.0
010	0.5
011	2.0
100	3.5
101	5.0
110	6.5
111	8.0

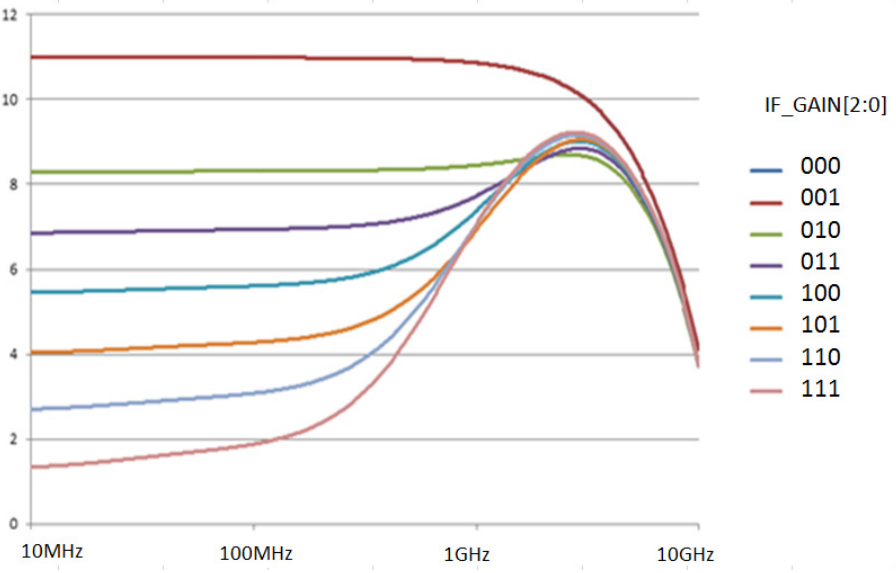


Fig 72. Equalizer gain (dB)

The auto-zero feature (bit XY_HS_RX_EQ_AUTO_ZERO_ENABLE in register XY_HS_RX_EQ_CNTRL) is enabled by default for the deserializer to adapt itself to the common-mode of the received signal.

11.10.3 Deserializer

The deserializer performs the incoming data clock recovery and also the serial-to-parallel conversion. One global PLL provides the same reference clock to the four lanes. The PLL configuration is automatically done when specifying the LMF parameters (see Table 10).

11.10.4 Low Serial Input Data Rate

When using the DAC165xQ with a low serial input data rate (lower than 3 Gbps), it is recommended to enable the low speed mode of the Clock Data Recovery (CDR) unit by writing the value x84 in register XY_HS_RX_CDR_DIV.

11.10.5 PHY test mode

A special test mode is available for measurement purposes only. The recovered clock of each CDR unit can be transmitted to the SYNC buffer after a frequency division by 20. This is done by setting the XY_SYNC_TEST_DATA_TX_ENABLE bit of register XY_SYNC_SEL_CNTRL_XY to logic 1. Bit XY_SYNC_TEST_DATA_SEL[1:0] is used to specify which CDR clock is used.

11.11 Output interfacing configuration

11.11.1 DAC1658Q: High common-mode output voltage

The DAC1658Q can easily be interfaced with high common mode modulator. Figure 73 is showing a typical connection in a 1Vpp configuration.

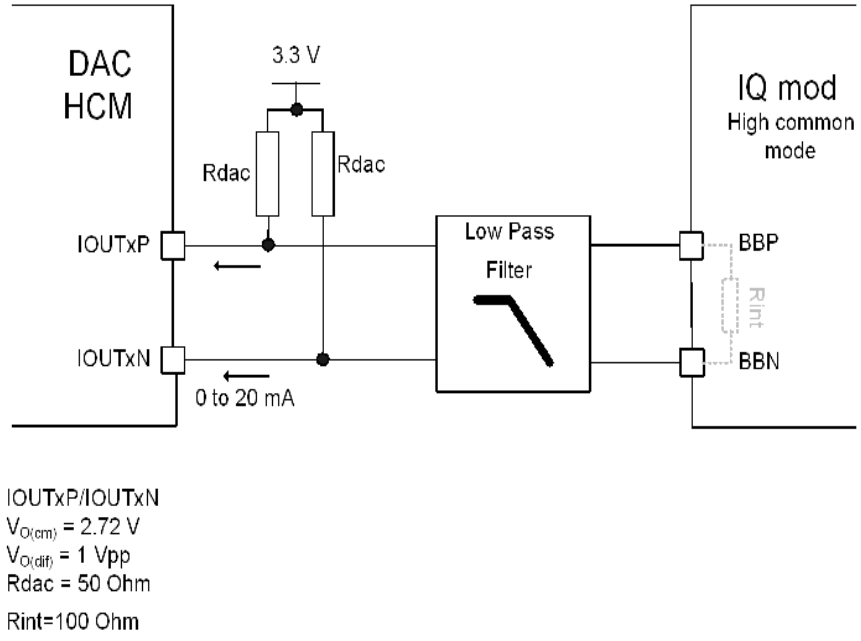
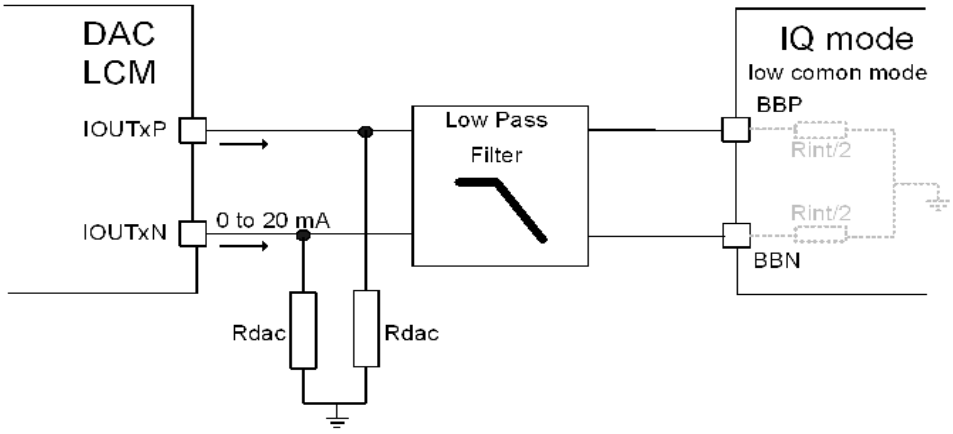


Fig 73. DAC1658Q (High common mode version) interface to IQ-modulator in $1V_{pp}$, DC coupling

11.11.2 DAC1653Q: Low common-mode output voltage

The DAC1653Q can easily be interfaced with the low common mode IQ-modulator. Figure 74 is showing a typical connection in a 1Vpp configuration



IOUTxP/IOUTxN
Idc = Ifs/2 + Ibias
Rint= 100 Ohm, Rdac = 50 Ohm
$V_{O(cm)}$ = Idc * (Rint/2 // Rdac) = 290 mV
$V_{O(dif)}$ = 1 Vpp

Fig 74. DAC1653Q (Low common mode version) interface to IQ-modulator in $1V_{pp}$, DC coupling

11.12 Design recommendations : power and grounding

Use a separate LDO power supply regulator for the generation of the $V_{DDA(1V2)}$ and $V_{DDD(1V2)}$ to ensure optimal performance.
V_{DDJ_SO} (JESD204B SYNCB power supply) , V_{DDD_IO} (IO interface power supply) , $V_{DDD(1V2)}$ (Digital core power supply), and $V_{DDj(1V2)}$ (JESD204B lane power supply) can use dedicated or shared power supply. LDO or switch power supply for these power supplies.
Use Low noise power supply for the generation of $V_{DDA(1V2)}$, $V_{DDA(out)}$ power supplies in order to ensure optimal performance.
Include individual LC decoupling for the following nine sets of power pins:

- $V_{DDA(1V2)\_DAC\_AB}$ (pins 65, 68, 69, 72)
- $V_{DDA(1V2)\_DAC\_CD}$ (pins 55, 58, 59, 62)
- $V_{DDA(1V2)\_BIASING}$ (pins 50, 53)
- $V_{DDA(1V2)\_CLOCK}$ (pins 2)
- $V_{DDD(1V2)}$ (pins 8, 15, 40, 47) , V_{DDD_IO} (pin 41) and V_{DDJ_SO} (pin 39)
- $V_{DDJ(1V2)}$ (pins 16, 23, 32)
- $V_{DDA(out)\_AB}$ (pins 1, 64)
  $V_{DDA(out)\_CD}$ (pins 54, 63)
- $V_{DDA(out)\_pll}$ (pins 5)

Use at least two capacitors for each power pin decoupling. Locate the smallest capacitors as close as possible to the DAC165xx power pins.

The die pad is used for both the power dissipation and electrical grounding. Insert several vias (typically 4*12 to connect the internal ground plane to the PCB top layer.

11.13 DAC165xQ registers control

11.13.1 Device register map (common device register)

Table 49 shows an overview all the SPI map of the common device register.

Table 49. DAC165xQ device register allocation map (common device register control)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
SPI configuration - Device ID											
0000h	SPI_CONFIG_A	R/W	SPI_RST	NOT USED	SPI_ASCEND	SPI_4W	MIRROR[3:0]				00h
0001h	SPI_CONFIG_B	R/W	SPI_SINGLE	NOT USED	SPI_READBUF	NOT USED					00h
0002h	DEV_PWR_MODE	R/W	NOT USED						DEV_PWR_MODE[1:0]		00h
0003h	CHIP_TYPE	R	CHIP_TYPE[7:0]								04h
0004h	CHIP_ID_0	R	CHIP_ID_0[7:0]								PP
0005h	CHIP_ID_1	R	CHIP_ID_1[7:0]								1Bh
0006h	CHIP_VERSION	R	CHIP_VS[7:0]								PP
000Ch	VENDOR_ID_LSB	R	VENDOR_ID[7:0]								26h
000Dh	VENDOR_ID_MSB	R	VENDOR_ID[15:8]								04h
000Fh	SPI_CONFIG_C	R/W	NOT USED							TRANS-FER_BIT	00h
Device Main Configuration											
0020h	MAINCONTROL	R/W		RE_INIT_MODE[2:0]			NOT USED	FORCE_RE-SET_PCLK	FORCE_RE-SET_DCLK	FORCE_RE-SET_WCLK	07h
0021h	DCSMU_CNTRL	R/W	MAN_PON_CNTRL	IGNORE_ASP_ERROR	AUTO_REG_TRANSFER	FORCE_LOCKDET	AUTO_QUICK_ENA	AUTO_LOCKDE-T_ENA	AUTO_AD-PLL_STARTUP	AUTO_ADPLL_-MODE	2Ch
0022h	POFF	R/W	POFF_RX[7:0]								00h
0028h	RX_PHY_LOCK	R/W								COMBINE_RX-_PHY_LOCK	00h
0029h	DCSMU_AUTO_CTRL1	W	REIN-IT_MC_ALARM_DIS	DCMSU_AD-PLL_ENA_INIT	-	WD_SYNC_-SENSITIVITY	WD_REINIT_-DISABLE	WD_BARK_ONCE	WD_DIS-ABLE_CD	WD_DIS-ABLE_AB	00h
	WD_STATUS	R	-	-	WD_CNT_IN-ACTIVE_CD	WD_CNT_END_CD	-	-	WD_CNT_IN-ACTIVE_AB	WD_CNT_END_AB	UUh
002Ah	PD_ANA_CNTRL	W	-	-	RFTX_ENA_P-D_ANA_CD	PD_ANA_EN-ABLE_CD	-	-	RFTX_ENA_P-D_ANA_AB	PD_ANA_EN-ABLE_AB	22h
	ANA_RES_STATUS	R	ANA_RES_CD[3:0]				ANA_RES_AB[3:0]				UUh
002Bh	CDI_CNTRL	R/W	SR_CDI_CD	CDI_MS_CD	CDI_MODE_CD[1:0]		SR_CDI_AB	CDI_MS_AB	CDI_MODE_AB[1:0]		00h
002Ch	SRC_SELECT_CNTRL	R/W	NOT USED	MDS_SE-LECT_E	SYNCB_SELECT_E[1:0]		NOT USED	MDS_SE-LECT_W	SYNCB_SELECT_W[1:0]		uuh
002Eh	DCSMU_WDTIMER0	R/W	WATCHDOG[7:0]								80h
002Fh	DCSMU_WDTIMER1	R/W	WATCHDOG[15:8]								00h
0030h	IO_MUX_CNTRL0	R/W	IO_SELECT_0[7:0]								15h
0031h	IO_MUX_CNTRL1	R/W	IO_SELECT_1[7:0]								15h
0032h	IO_MUX_CNTRL2	R/W	IO_SELECT_2[7:0]								15h

Table 49. DAC165xQ device register allocation map (common device register control)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0033h	IO_MUX_CNTRL3	R/W	IO_SELECT_3[7:0]								15h
0034h	IO_MUX_CNTRL4	R/W	IO_SELECT_4[7:0]								00h
0035h	IO_CNTRL	R/W	IO_ENA[3:0]				IO_EHS[1:0]		SDO_EHS[1:0]		AAh
0036h	RF_TX_INPUT_CNTRL	R/W	NOT USED	RF_TX_X-OR_CD	RF_TX_SEL_CD[1:0]		NOT USED	RF_TX_XOR_AB	RF_TX_SEL_AB[1:0]		31h
0037h	DCSMU_XTIMER0	W	RXPHY_ENA_LOW_TIME[7:0]								01h
0037h	MON_DCLK_AB	R	MON_D-CLK_XY_STOP	NOT USED			MON_DCLK_AB[3:0]				uu
0038h	DCSMU_XTIMER1	W	CDR_ENA_LOW_TIME[7:0]								01h
0038h	MON_DCLK_XY_FLAGS	R	MON_DCLK_XY_FLAGS[7:0]								uu
0039h	DCSMU_XTIMER2	W	WAIT_FOR_LOCK_TIME[7:0]								01h
0039h	MON_DCLK_CD	R	MON_D-CLK_C-D_STOP	NOT USED			MON_DCLK_CD[3:0]				uu
003Ah	DCSMU_XTIMER3	W	WAIT_FOR_TRACK_TIME[7:0]								18h
003Ah	MON_DCLK_CD_-FLAGS	R	MON_DCLK_CD_FLAGS[7:0]								uu
003Bh	DCSMU_XTIMER4	W	TRACK_RUNIN_TIME[7:0]								01h
003Bh	MON-DCMSU_0	R	RESERVED								uu

Table 49. DAC165xQ device register allocation map (common device register control)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Common Quad DAC Configuration Controls											
01A0h	AUX_-DAC_HIGH_RESab	R/W	RESERVED (must be =0)	AUX_-DAC_HIGH_RESab	RESERVED (must be =0)						00h
0247h	AUX_-DAC_HIGH_REScd	R/W	RESERVED (must be =0)							AUX_DAC_HIGH_REScd	00h
01ACh	PON_CFG_NC	R/W	PON_I-SOURCE_-CLKDIV_2	PON_I-SOURCE_-CLKDIV_1	PON_I-SOURCE_AD-PLLBUF_IBIAS	PON_I-SOURCE_AD-PLLBUF_ICAS	PON_I-SOURCE_-CLKCAS	PON_I-SOURCE_CLK	PON_BIAS_COMMON	PON_GAP	0Fh
01ADh	CLKGENCFG1	R/W					WCLK_DIV_BYPASS	WCLK_DIV_SEL[2:0]			02h
01AFh	CLKDIV_CFG	R/W				CLK_DIV_SEL_FREQ	CLK_DIV_BY-PASS	CLK_DIV_RE-SET	CLK_DIV_SEL[1:0]		08h

Table 49. DAC165xQ device register allocation map (common device register control)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Temperature Sensor											
01B3h	TEMPS_CNTRL	R/W	TEMP_-SENS_PON	TS_RST_ALARM	TS_FULL-RANGE	TS_TOGGLE	TS_RST_MAX	TS_RST_MIN	TS_MODE[1:0]		00h
01B4h	TEMPS_LEVEL	Wr			TEMP_EL_MAN[5:0]						00h
01B4h	TEMPS_OUT	R	TEMP_-SENS_OUT	TEMP_ALARM	TEMP_ACTUAL[5:0]						uu
01B5h	TEMPS_MAX	Wr	TS_CLKDIV[7:0]								00h
01B5h	TEMPS_MAX	R			TEMP_MAX[5:0]						uu
01B6h	TEMPS_MIN	Wr	TS_TIMER[7:0]								00h
01B6h	TEMPS_MIN	R			TEMP_MIN[5:0]						uu
01B7h	MDS_IO_CNTRL0	R/W	PON_I-SOURCE_MDS_E	-	-	MDS_SEL_RT_E	PON_I-SOURCE_MDS_W	-	-	MDS_SEL_RT_W	88h
01B8h	MDS_IO_CNTRL1	R/W	MDS_RESYN-C_SYSREF	-	MDS_SYS-REF_POL_E	MDS_SYS-REF_POL_W	MDS_SET_DELAY_E[1:0]		MDS_SET_DELAY_W[1:0]		05h
01C8h	ADPLL_PREDIV	R/W					ADPLL_PREDIV[3:0]				00h
01C9h	ADPLL_POSTDIV	R/W					ADPLL_POSTDIV[2:0]				01h
01CAh	ADPLL_CNTRL	Wr	ADPLL_-SOFT_RST_N	ENA_DRIFT_-COMP	ADPLL_LOCK_TOGGLE	PON_PCLK	ADPLL_DIG_PON	ADPLL_PRE-DIV_PON	ADPLL_PRE-DIV_BYPASS	ADPLL_BY-PASS	01h
01CAh	ADPLL_SU_STATUS	R	NOT USED	ASP_STARTUP_SEL[2:0]			ADPLL_LIN_RDY	ADPLL_BB_RDY	FORCE_AD-PLL_LOCKED	ADPLL_LOCKED_XOR	uu
01CCh	ADPLL_DCO_CTF_0	R	ADPLL_DCO_CTF[7:0]								uu
01CDh	ADPLL_DCO_CTF_1	R	ADPLL_DCO_CTF[15:8]								00

11.13.2 Dual core block register map (DAC AB and/or DAC CD)

Table 50 shows an overview all the dual core block register map (DAC AB and/or DAC CD).

- adress from 040h to 1FFh is reserved for dual DAC AB.
- adress from 240h to 3FFh is reserved for dual DAC CD.
- adress from 440h to 5FFh is reserved for dual write access to DAC AB and DAC CD (only write access possible).

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Dual DAC XY Core Configuration											
Analog Gain - Auxiliary DACs											
0040h 0240h 0440h	XY_PON_DDCCFG_0	R/W	NOT USED		XY_PON_BIAS	XY_PON_CGU	XY_PON_-DAC_Y	XY_PON_COM-M_Y	XY_PON_-DAC_X	XY_PON_COM-M_X	FFh
0042h 0242h 0442h	XY_CLKGENCFG2	Wr		XY_CLK-GEN_EN_DIV_DETECT(MON)	XY_CLK-GEN_INIT_DIV	NOT USED					52h
		R	CLK_MON_RESET (STA-TUS)								52h
0054h 0254h 0454h	XY_CLK_DIV_CFG	R/W	XY_CLKDIV_PHASE[2:0]								88h
0057h 0257h 0457h	XY_CSA_CFG_X_0	R/W	XY_CSA_BIAS_X[7:0]								20h
0058h 0258h 0458h	XY_CSA_CFG_X_0	R/W	XY_PON_CSA_X	NOT USED				XY_CSA_-MULT2_X	XY_CSA_BIAS_X[9:8]		83h
0059h 0259h 0459h	XY_CSA_CFG_Y_0	R/W	XY_CSA_BIAS_Y[7:0]								20h
005Ah 025Ah 045Ah	XY_CSA_CFG_Y_1	R/W	XY_PON_CSA_Y	NOT USED				XY_CSA_-MULT2_Y	XY_CSA_BIAS_Y[9:8]		83h
005Bh 025Bh 045Bh	XY_AUX_CFG_X_0	R/W	XY_AUX_DAC_X[7:0]								00h
005Ch 025Ch 045Ch	XY_AUX_CFG_X_0	R/W	XY_PON_AUX_DAC_X	NOT USED					XY_AUX_DAC_X[9:8]		82h
005Dh 025Dh 045Dh	XY_AUX_CFG_Y_0	R/W	XY_AUX_DAC_Y[7:0]								00h
005Eh 025Eh 045Eh	XY_AUX_CFG_Y_1	R/W	XY_PON_AUX_DAC_Y	NOT USED					XY_AUX_DAC_Y[9:8]		82h
Digital Signal Processing (DSP) for Dual DAC XY											

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
NCO Frequency Phase correction											
0060h 0260h 0460h	XY_TXCFG	R/W	XY_NCO_EN	XY_NCO_LOW-POWER	XY_INV_SINC_EN	XY_MODE[2:0]			XY_INT_FIR[1:0]		01h
0062h 0262h 0462h	XY_PHINCO_LSB	R/Wb	XY_PHI_NCO[7:0]								00h
0063h 0263h 0463h	XY_PHINCO_MSB	R/Wb	XY_PHI_NCO[15:8]								00h
0064h 0264h 0464h	XY_FREQNCO_B0	R/Wb	XY_FREQ_NCO[7:0]								89h
0065h 0265h 0465h	XY_FREQNCO_B1	R/Wb	XY_FREQ_NCO[15:8]								67h
0066h 0266h 0466h	XY_FREQNCO_B2	R/Wb	XY_FREQ_NCO[23:16]								66h
0067h 0267h 0467h	XY_FREQNCO_B3	R/Wb	XY_FREQ_NCO[31:24]								66h
0068h 0268h 0468h	XY_FREQNCO_B4	R/Wb	XY_FREQ_NCO[39:32]								26h
0069h 0269h 0469h	XY_PHASECORR_CNTRL0	R/Wb	XY_PHASE_CORR[7:0]								00h
006Ah 026Ah 046Ah	XY_PHASECORR_CNTRL1	R/Wb	XY_PHASE_CORR_ENABLE	XY_PHASE_CORR_SWAP[1:0]		XY_PHASE_CORR[12:8]					00h
Digital Gain and Offset DAC XY											
006Bh 026Bh 046Bh	XY_DSP_X_GAIN_LSB	R/Wb	XY_DSP_X_GAIN[7:0]								50h
006Ch 026Ch 046Ch	XY_DSP_X_GAIN_MSB	R/Wb					XY_DSP_X_GAIN[11:8]				0Bh
006Dh 026Dh 046Dh	XY_DSP_Y_GAIN_LSB	R/Wb	XY_DSP_Y_GAIN[7:0]								50h
006Eh 026Eh 046Eh	XY_DSP_Y_GAIN_MSB	R/Wb					XY_DSP_Y_GAIN[11:8]				0Bh
006Fh 026Fh 046Fh	XY_DSP_OUT_CNTRL	R/Wb					XY_DSP_X_GAIN_EN	XY_DSP_Y_GAIN_EN	XY_MINUS_3DB_GAIN	XY_CLIP_LEV_EN	00h
0070h 0270h 0470h	XY_DSP_CLIPLEV	R/Wb	XY_CLIPLEV[7:0]								FFh

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0071h 0271h 0471h	XY_DSP_X_OFFSET_LSB	R/Wb	XY_DSP_X_OFFSET[7:0]								00h
0072h 0272h 0472h	XY_DSP_X_OFFSET_MSB	R/Wb	XY_DSP_X_OFFSET[15:8]								00h
0073h 0273h 0473h	XY_DSP_Y_OFFSET_LSB	R/Wb	XY_DSP_Y_OFFSET[7:0]								00h
0074h 0274h 0474h	XY_DSP_Y_OFFSET_MSB	R/Wb	XY_DSP_Y_OFFSET[15:8]								00h

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Data Format And IQ Levels DAC XY											
0075h 0275h 0475h	XY_IQ_LEV_CNTRL	R/Wb	XY_DATA_-FORMAT	NOT USED			XY_I_LEV_CNTR[1:0]		XY_Q_LEV_CNTRL[1:0]		85h
0076h 0276h 0476h	XY_I_DC_LEVEL_LSB	R/Wb	XY_I_DC_LEVEL[7:0]								00h
0077h 0277h 0477h	XY_I_DC_LEVEL_MSB	R/Wb	XY_I_DC_LEVEL[15:8]								80h
0078h 0278h 0478h	XY_Q_DC_LEVEL_LSB	R/Wb	XY_Q_DC_LEVEL[7:0]								00h
0079h 0279h 0479h	XY_Q_DC_LEVEL_MSB	R/Wb	XY_Q_DC_LEVEL[15:8]								80h
Signal Power Detector DAC XY											
007Ah 027Ah 047Ah	XY_SPD_CNTRL	R/Wb	XY_SPD_ENA	NOT USED			XY_SPD_WINLENGTH[3:0]				00h
007Bh 027Bh 047Bh	XY_SPD_THRESH-OLD_LSB	R/Wb	XY_SPD_THRESHOLD[7:0]								00h
007Ch 027Ch 047Ch	XY_SPD_THRESH-OLD_MSB	R/Wb	XY_SPD_THRESHOLD[15:8]								00h
007Dh 027Dh 047Dh	XY_SPD_AVER-AGE_LSB	R	XY_SPD_AVERAGE[7:0]								uu
007Eh 027Eh 047Eh	XY_SPD_AVER-AGE_MSB	R	XY_SPD_AVERAGE[15:8]								uu
MUTE Controller DAC XY											
0080h 0280h 0480h	XY_MUTE_CNTRL_0	R/W	XY_MUTE_ENABLE	XY_SW_MUTE_ENA	XY_MC_ALARM_CLR	XY_HOLD_-DATA	NOT USED	XY_CLIPDE-T_ENA	XY_CLIP_SEL[1:0]		90h
0081h 0281h 0481h	XY_MUTE_CNTRL_1	R/W	XY_INCIDENT_CFG[1:0]		XY_DATA_CFG[1:0]		XY_ALARM_CFG[1:0]		XY_DIRECT_CFG[1:0]		77h
0082h 0282h 0482h	XY_MUTE_CNTRL_2	R/W	XY_IGNORE_ALARM	XY_IGNORE_RFTX_ENA	XY_IGNORE_MDS_BUSY	XY_IGNORE_-DATA_V_IQ	NOT USED	XY_ENA_IQR_INCIDENT	XY_ENA_SP-D_INCIDENT	XY_ENA_ER-F_INCIDENT	81h
0083h 0283h 0483h	XY_MUTE_AL_ENA_0	R/W	XY_MC_AL_ENA[7]	XY_MC_AL_ENA[6]	XY_MC_AL_ENA[5]	XY_MC_AL_ENA[4]	XY_MC_AL_ENA[3]	XY_MC_AL_ENA[2]	XY_MC_AL_ENA[1]	XY_MC_AL_ENA[0]	00h
0084h 0284h 0484h	XY_MUTE_AL_ENA_1	R/W	NOT USED						XY_MC_AL_ENA[9]	XY_MC_AL_ENA[8]	00h
0085h 0285h 0485h	XY_MUTE_RATE_CN-TRL_0	R/W	XY_ALARM_MRATE[3:0]				XY_DIRECT_MRATE[3:0]				7Ch

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0086h 0286h 0486h	XY_MUTE_RATE_CNTRL_1	R/W	XY_INCIDENT_MRATE[3:0]				XY_DATA_MRATE[3:0]				7Ch
0087h 0287h 0487h	XY_MUTE_WAITPERIOD_LSB	R/W	XY_MUTE_WAITPERIOD[7:0]								40h
0088h 0288h 0488h	XY_MUTE_WAITPERIOD_MSB	R/W	XY_MUTE_WAITPERIOD[15:8]								00h
0089h 0289h 0489h	XY_IQ_RANGE_LIMIT_LSB	R/Wb	XY_IQ_RANGE_LIMIT[7:0]								00h
008Ah 028Ah 048Ah	XY_IQ_RANGE_LIMIT_MSB	R/Wb	XY_IQ_RANGE_LIMIT[15:8]								80h
Interrupt DAC XY											
008Ch 028Ch 048Ch	XY_INTR_CNTRL	R/W					XY_INTR_CLEAR	XY_INTR_MON_DCLK_RANGE[2:0]			08h
008Dh 028Dh 048Dh	XY_INTR_ENA_0	R/W	XY_INTR_ENA[7:0]								00h
008Eh 028Eh 048Eh	XY_INTR_ENA_1	R/W	NOT USED	XY_INTR_ENA[9:8]							00h
008Fh 028Fh 048Fh	XY_INTR_FLAGS_0	R	XY_INTR_DLP	XY_(NOT MDS_BUSY)	XY_MDS_BUSY	XY_TEMP_ALARM	XY_CLIP_DET_OR	XY_CA_ERROR	XY_CLK_MON	XY_MON_DCLK_ERR	uu
0090h 0290h 0490h	XY_INTR_FLAGS_1	R	NOT USED	XY_ERR_RPT_FLAG	XY_MC_ALARM	NOT USED					uu
Digital Signal Processing Strobe controls											
0099h 0299h 0499h	XY_DSP_SAMPLE_CNRL	R/W				XY_DSP_READ_SEL	XY_DSP_STROBE	XY_DSP_SMPL_SEL[2:0]			00h
009Ah 029Ah 049Ah	XY_DSP_READ_LSB	R	XY_DSP_READ[7:0]								uu
009Bh 029Bh 049Bh	XY_DSP_READ_LSIB	R	XY_DSP_READ[15:8]								uu
009Ch 029Ch 049Ch	XY_DSP_READ_MSIB	R	XY_DSP_READ[23:16]								uu
009Dh 029Dh 049Dh	XY_DSP_READ_MSB	R	XY_DSP_READ[31:24]								uu

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Multiples Device Synchronization Controls DAC XY											
00A0h 02A0h 04A0h	XY_MDS_MAIN	R/W	XY_MDS_EQCHECK[1:0]		XY_MDS_MAN	XY_MDS_S-REF_DIS	XY_MDS_EAST_WEST	XY_MDS_MODE[1:0]		XY_MDS_ENA	E0h
00A1h 02A1h 04A1h	XY_MDS_VS1_CNTRL	R/W	XY_DLP_ISSUE_COND[1:0]		XY_IGNORE_ENA_CORR	NOT USED	XY_I_REINIT_MODE[1:0]		XY_MDS_-COPY	XY_MDS_CAP-TURE_ENA	05h
00A2h 02A2h 04A2h	XY_MDS_IO_CNTRL	R/W	XY_MDS_MAN_SEL_FE_E	XY_MDS_MAN_SEL_FE_W	XY_MDS_IO_PON_E	XY_MDS_IO_PON_W	XY_MDS_SEL_FE_E	-	XY_MDS_SEL_FE_W	-	30h
00A3h 02A3h 04A3h	XY_MDS_MISCCNTRL0	R/W	XY_MDS_RUN	XY_MDS_NCO	XY_MDS_N-CO_PULSE	XY_MDS_EVAL_ENA	XY_MDS_PRERUN_ENA	XY_MDS_PULSEWIDTH[2:0]			10h
00A4h 02A4h 04A4h	XY_MDS_MAN_AD-JUSTDLY	R/W	XY_MDS_MAN_ADJUSTDLY[7:0]								80h
00A5h 02A5h 04A5h	XY_MDS_AUTO_CY-CLES	R/W	XY_MDS_AUTO_CYCLES[7:0]								80h
00A6h 02A6h 04A6h	XY_MDS_MISCCNTRL1	R/W	XY_MDS_S-R_CKEN	XY_MDS_S-R_LOCKOUT	XY_MDS_S-R_LOCK	XY_MDS_RE-LOCK	XY_MDS_LOCK_DELAY				0Fh
00A7h 02A7h 04A7h	XY_MDS_OFFSET_DLY	R/W				XY_MDS_OFFSET_DLY[4:0]					00h
00A8h 02A8h 04A8h	XY_MDS_WIN_LOW	R/W	XY_MDS_WIN_PERIOD_A[7:0]								0Fh
00A9h 02A9h 04A9h	XY_MDS_WIN_HIGH	R/W	XY_MDS_WIN_PERIOD_B[7:0]								07h
00AAh 02AAh 04AAh	XY_LMFC_PERIOD	R/W	XY_LMFC_PERIOD[7:0]								10h
00ABh 02ABh 04ABh	XY_LMFC_PRESET	R/W	XY_LMFC_PRESET[7:0]								04h
00ACh 02ACh 04ACh	XY_MDS_CNT_PRESET	R/W	XY_MDS_CNT_PRESET[7:0]								02h
00ADh 02ADh 04ADh	XY_SYNC_LMFC_PE	R/W	XY_SYNC_LMFC_PE[7:0]								04h
00AEh 02AEh 04AEh	XY_MDS_SYNC_CNTRL	R/W				XY_MDS_SYNC_INIT	XY_MDS_AU-TO_SYNC_PE	XY_SYNC_FINE_DLY[2:0]			0Dh
00AFh 02AFh 04AFh	XY_MDS_WIN_DLY	R/W		XY_MDS_AU-TO_PRESET	XY_MDS_AU-TO_WIN_DLY	XY_MDS_WIN_DLY[4:0]					60h

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Multiples Device Synchronization Status DAC XY											
00B2h 02B2h 04B2h	XY_MDS_SEARCH_CY-CLE	R	XY_MDS_SEARCH_CYCLE[7:0]								20h
00B5h 02B5h 04B5h	XY_MDS_ADJDELAY	R	XY_MDS_ADJDELAY[7:0]								uu
00B6h 02B6h 04B6h	XY_MDS_STATUS0	R	XY_ER-R_RPT_FLAG	-	-	XY_ADD_ER-ROR	XY_EAR-LY_ERROR	XY_LATE_ER-ROR	-	XY_MDS_AC-TIVE	uu
00B7h 02B7h 04B7h	XY_MDS_STATUS1	R	XY_I_BUSY	XY_I_STATE_ERR	XY_I_LOCK_-DET	XY_I_DLP_LO CK -	XY_I_STATE[3:0]				uu
00B8h 02B8h 04B8h	XY_MDS_STATUS2	R	XY_MDS_LO CK	RESERVED			XY_EQUAL_-CHECK	RESERVED			uu
00BBh 02BBh 04BBh	XY_MDS_STATUS5	R	XY_DELAY_CNT[7:0]								uu
00BCh 02BCh 04BCh	XY_MDS_STATUS6	R	XY_I_ENA_SAMPLE[7:0]								uu
00BDh 02BDh 04BDh	XY_MDS_STATUS7	R	-	-	XY_MDS_PRE-RUN	XY_MDS _LOCKO UT	-	-	XY_ENA_PHASE		uu
Digital Lane Processing (DLP) DAC XY **Lanes Swapping, Polarity control, SYNC control, SCRambler control**											
00C7h 02C7h 04C7h	XY_ILA_CNTRL	R/W	XY_COM-BINE_ILA_CN TRL	XY_SEL_ILA[1:0]		XY_SEL_LOCK[2:0]			XY_-SUP_LANE_S YN	XY_EN_SCR	63h
00C8h 02C8h 04C8h	XY_ALIGN_CNTRL	R/W	XY_-FORCE_1ST_ SMPL_LOW	XY_USE_/Q/ 0:	-	-	XY_SUB_CLA SS0	XY_FRAME_ALI GN_ENA	XY_DY-N_ALIGN_ENA	XY_-FORCE_ALIGN	86h
00CBh 02CBh 04CBh	XY_ERR_HANDLING_0	R/W	XY_EN_K-OUT_UNEX-P_LN3	XY_EN_K-OUT_UNEX-P_LN2	XY_EN_K-OUT_UNEX-P_LN1	XY_EN_K-OUT_UNEX-P_LN0	XY_EN_NIT_E RR_LN3	XY_EN_NIT_ER-R_LN2	XY_EN_NIT_E RR_LN1	XY_EN_NIT_ER R_LN0	FFh
00CCh 02CCh 04CCh	XY_SYNCOUT_MODE	R/W	XY_SEL_RE_INIT[2:0]			XY_COM-BINE_SYN-C_CNTRL	XY_SYN-C_INIT_LEVEL	XY_SEL_SYNC[2:0]			00h
00CDh 02CDh 04CDh	XY_LANE_POLARITY	R/W				XY_SYN-C_POL	XY_POL_P_L N3	XY_POL_P_LN2	XY_POL_P_L N1	XY_POL_P_LN 0	00h
00CEh 02CEh 04CEh	XY_LANE_SELECT	R/W	XY_LANE_SEL_L_LN#3[1:0]		XY_LANE_SEL_L_LN#2[1:0]		XY_LANE_SEL_L_LN#1[1:0]		XY_LANE_SEL_L_LN#0[1:0]		E4h
Scramblers Initialization values DAC XY											
00D0h 02D0h 04D0h	XY_SOFT_RE-SET_SCRAMBLER	R/W			XY_S-R_NO_F20_AC T_FLAG	XY_SR_ILA	XY_S-R_SCR_LN3	XY_S-R_SCR_LN2	XY_S-R_SCR_LN1	XY_S-R_SCR_LN0	00h

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00D1h 02D1h 04D1h	XY_INIT_SCR_S15T8_LN0	R/W	XY_INIT_DESCR_P_LN0[15:8]								FFh
00D2h 02D2h 04D2h	XY_INIT_SCR_S7T1_LN0	R/W		XY_INIT_DESCR_P_LN00[7:1]							00h
00D3h 02D3h 04D3h	XY_INIT_SCR_S15T8_LN1	R/W	XY_INIT_DESCR_P_LN01[15:8]								FFh
00D4h 02D4h 04D4h	XY_INIT_SCR_S7T1_LN1	R/W		XY_INIT_DESCR_P_LN01[7:1]							00h
00D5h 02D5h 04D5h	XY_INIT_SCR_S15T8_LN2	R/W	XY_INIT_DESCR_P_LN02[15:8]								FFh
00D6h 02D6h 04D6h	XY_INIT_SCR_S7T1_LN2	R/W		XY_INIT_DESCR_P_LN02[7:1]							00h
00D7h 02D7h 04D7h	XY_INIT_SCR_S15T8_LN3	R/W	XY_INIT_DESCR_P_LN03[15:8]								FFh
00D8h 02D8h 04D8h	XY_INIT_SCR_S7T1_LN3	R/W		XY_INIT_DESCR_P_LN03[7:1]							00h
Initial Lane Alignment initialization, Error handling, DLP strobe, LMF configuration											
00D9h 02D9h 04D9h	XY_INIT_ILA_BUFPTR_L_LN01	R/W	XY_INIT_ILA_BUFPTR_L_LN#1[3:0]				XY_INIT_ILA_BUFPTR_L_LN#0[3:0]				88h
00DAh 02DAh 04DAh	XY_INIT_ILA_BUFPTR_L_LN23	R/W	XY_INIT_ILA_BUFPTR_L_LN#3[3:0]				XY_INIT_ILA_BUFPTR_L_LN#2[3:0]				88h
00DBh 02DBh 04DBh	XY_ERR_HANDLING_1	R/W	XY_EN_DISP_ERR_P_LN	XY_EN_DISP_ERR_P_LN2	XY_EN_DISP_ERR_P_LN1	XY_EN_DISP_ERR_P_LN0	XY_CONCEAL_MODE	XY_SEL_CS_LIMIT	XY_IGNORE_ERR[1:0]		F8h
00DCh 02DCh 04DCh	XY_REINIT_CNTRL	R/W	XY_REINIT_ILA_L_LN#3	XY_REINIT_ILA_L_LN#2	XY_REINIT_ILA_L_LN#1	XY_REINIT_ILA_L_LN#0	XY_RESYNC_OLINK_P_LN3	XY_RESYNC_OLINK_P_LN2	XY_RESYNC_OLINK_P_LN	XY_RESYNC_OLINK_P_LN0	FFh
00DDh 02DDh 04DDh	XY_MISC_CNTRL	R/W	XY_DLP-STROBE	NOT USED							00h
00DEh 02DEh 04DEh	XY_LMF_CNTRL	R/W	XY_L[2:0]			XY_M[1:0]		XY_F[2:0]			92h
Digital Lane Processing monitoring DAC XY											
00E0h 02E0h 04E0h	XY_ILA_MON_1_0	R	XY_ILA_MON_L_LN#1[3:0]				XY_ILA_MON_L_LN#0[3:0]				uu
00E1h 02E1h 04E1h	XY_ILA_MON_3_2	R	XY_ILA_MON_L_LN#3[3:0]				XY_ILA_MON_L_LN#2[3:0]				uu

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00E2h 02E2h 04E2h	XY_ILA_BUF_ERR	R					XY_ILA_BUF_ERR_L_LN#3	XY_ILA_BUF_ERR_L_LN#2	XY_ILA_BUF_ERR_L_LN#1	XY_ILA_BUF_ERR_L_LN#0	uu

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
8b10b decoder flags											
00E4h 02E4h 04E4h	XY_DEC_FLAGS	R	XY_-DEC_NIT_ERR_P_LN3	XY_-DEC_NIT_ERR_P_LN2	XY_-DEC_NIT_ERR_P_LN1	XY_-DEC_NIT_ERR_P_LN0	XY_-DEC_DISP_ERR_P_LN3	XY_-DEC_DISP_ERR_P_LN2	XY_-DEC_DISP_ERR_P_LN1	XY_-DEC_DISP_ERR_P_LN0	uu
00E5h 02E5h 04E5h	XY_KOUT_FLAG	R					XY_DEC_K-OUT_P_LN3	XY_DEC_K-OUT_P_LN2	XY_DEC_K-OUT_P_LN1	XY_DEC_K-OUT_P_LN0	uu
00E6h 02E6h 04E6h	XY_K28_LN0_FLAG	R	XY_P_LN0_ILA_MFR_ERR	XY_P_LN0_ILA_QT4_ERR	XY_P_LN0_ILA_LT4_ERR	XY_K28_7_LN0	XY_K28_5_P_LNXY_K28_4_P_LN0	XY_K28_4_P_LN0	XY_K28_3_P_LN0	XY_K28_0_P_LN0	uu
00E7h 02E7h 04E7h	XY_K28_LN1_FLAG	R	XY_P_LN1_ILA_MFR_ERR	XY_P_LN1_ILA_QT4_ERR	XY_P_LN1_ILA_LT4_ERR	XY_K28_7_P_LN1	XY_K28_5_P_LN1	XY_K28_4_P_LN1	XY_K28_3_P_LN1	XY_K28_0_P_LN1	uu
00E8h 02E8h 04E8h	XY_K28_LN2_FLAG	R	XY_P_LN2_ILA_MFR_ERR	XY_P_LN2_ILA_QT4_ERR	XY_P_LN2_ILA_LT4_ERR	XY_K28_7_P_LN2	XY_K28_5_P_LN2	XY_K28_4_P_LN2	XY_K28_3_P_LN2	XY_K28_0_P_LN2	uu
00E9h 02E9h 04E9h	XY_K28_LN3_FLAG	R	XY_P_LN3_ILA_MFR_ERR	XY_P_LN3_ILA_QT4_ERR	XY_P_LN3_ILA_LT4_ERR	XY_K28_7_P_LN3	XY_K28_5_P_LN3	XY_K28_4_P_LN3	XY_K28_3_P_LN3	XY_K28_0_P_LN3	uu
00EAh 02EAh 04EAh	XY_KOUT_UNEXPECT-ED_FLAG	R					XY_DEC_K-OUT_UNEX-P_LN3	XY_DEC_K-OUT_UNEX-P_LN2	XY_DEC_K-OUT_UNEX-P_LN1	XY_DEC_K-OUT_UNEX-P_LN0	uu
RX-PHY lock and Code Group Synchronization State Machine monitoring											
00EBh 02EBh 04EBh	XY_LOCK_CNT_MON_P_LN01	R	XY_LOCK_CNT_MON_P_LN1[3:0]				XY_LOCK_CNT_MON_P_LN0[3:0]				uu
00ECh 02ECh 04ECh	XY_LOCK_CNT_MON_P_LN23	R	XY_LOCK_CNT_MON_P_LN3[3:0]				XY_LOCK_CNT_MON_P_LN2[3:0]				uu
00EDh 02EDh 04EDh	XY_CS_STATE_P_LNX	R	XY_CS_STATE_P_LN3[1:0]		XY_CS_STATE_P_LN2[1:0]		XY_CS_STATE_P_LN1[1:0]		XY_CS_STATE_P_LN0[1:0]		uu
Flags counters and DLP interrupt controls											
00EEh 02EEh 04EEh	XY_MISC_FLAG_CN-TRL	R/W	XY_RST_BUF_ERR_FLAGS	XY_AU-TO_RST_-FLAGCNTS	XY_-FLAGCNT_HOLD_MODE	NOT USED					00h
00EFh 02EFh 04EFh	XY_INTR_MISC_ENA	R/W	XY_IN-TR_ENA_CS_INIT_P_LN3	XY_IN-TR_ENA_CS_INIT_P_LN2	XY_IN-TR_ENA_CS_INIT_P_LN1	XY_IN-TR_ENA_CS_INIT_P_LN0	XY_IN-TR_ENA_BUF_ERR_LN3	XY_IN-TR_ENA_BUF_ERR_LN2	XY_IN-TR_ENA_BUF_ERR_LN1	XY_IN-TR_ENA_BUF_ERR_LN0	00h
00F0h 02F0h 04F0h	XY_FLAG_CNT_LS-B_LN0	R	XY_FLAG_CNT_LN0[7:0]								uu
00F1h 02F1h 04F1h	XY_FLAG_CNT_MS-B_LN0	R	XY_FLAG_CNT_LN0[15:8]								uu
00F2h 02F2h 04F2h	XY_FLAG_CNT_LS-B_LN1	R	XY_FLAG_CNT_LN1[7:0]								uu
00F3h 02F3h 04F3h	XY_FLAG_CNT_MS-B_LN1	R	XY_FLAG_CNT_LN1[15:8]								uu

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
00F4h 02F4h 04F4h	XY_FLAG_CNT_LSB_LN2	R	XY_FLAG_CNT_LN2[7:0]								uu
00F5h 02F5h 04F5h	XY_FLAG_CNT_MSB_LN2	R	XY_FLAG_CNT_LN2[15:8]								uu
00F6h 02F6h 04F6h	XY_FLAG_CNT_LSB_LN3	R	XY_FLAG_CNT_LN3[7:0]								uu
00F7h 02F7h 04F7h	XY_FLAG_CNT_MSB_LN3	R	XY_FLAG_CNT_LN3[15:8]								uu
00F8h 02F8h 04F8h	XY_ERR_MIX_CNTRL	R/W	XY_EM								FFh
00F9h 02F9h 04F9h	XY_INTR_ENA0	R/W	-	-	-	-	XY_INTR_STLTP_ERR	XY_INTR_BER_LN<I>	XY_INTR_ILA_RCV	XY_INTR_NO_ACT_F20	00h
00FAh 02FAh 04FAh	XY_INTR_ENA1	R/W	XY_INTR_ENA_NIT	XY_INTR_ENA_DISP	XY_INTR_ENA_K-OUT	XY_INTR_ENA_K-OUT_UNEXP	XY_INTR_ENA_K28_7	XY_INTR_ENA_K28_5	XY_INTR_ENA_K28_3	XY_INTR_ENA_MISC	00h
00FBh 02FBh 04FBh	XY_CNTRL_FLAGCNT_LN01	R/W	XY_RST_CFC_LN1	XY_SEL_CFC_LN1[2:0]			XY_RST_CFC_LN0	XY_SEL_CFC_LN0[2:0]			55h
00FCh 02FCh 04FCh	XY_CNTRL_FLAGCNT_LN23	R/W	XY_RST_CFC_LN3	XY_SEL_CFC_LN3[2:0]			XY_RST_CFC_LN2	XY_SEL_CFC_LN2[2:0]			55h
00FDh 02FDh 04FDh	XY_MON_FLAGS_RESET	R/W	XY_RST_NIT_ERRFLAGS	XY_RST_DISP_ERR_FLAGS	XY_RST_K-OUT_FLAGS	XY_RST_K-OUT_UNEXPECTED_FLAGS	XY_RST_K28_LN3_FLAGS	XY_RST_K28_LN2_FLAGS	XY_RST_K28_LN1_FLAGS	XY_RST_K28_LN0_FLAGS	00h
00FEh 02FEh 04FEh	XY_DBG_CNTRL	R/W	XY_BER_MODE	XY_DBG_INTR_CLEAR	XY_INTR_MODE			NOT USED			00h
PRBS, JTSPAT, BER controls and indicator DAC XY											
0100h 0300h 0500h	XY_BER_CNTRL_0	R/W	XY_SEL_XBERT_LN[1:0]		XY_CHECK_PRBS	NOT USED	XY_XBERT_CNTRL[2: 0]			XY_SR_XBERT_CNT	00h
0101h 0301h 0501h	XY_BER_CNTRL_1	R/W		XY_START_WIN_JTSPAT[6:0]							00h
0102h 0302h 0502h	XY_BER_CNTRL_2	R/W		XY_STOP_WIN_JTSPAT[6:0]							75h
0103h 0303h 0503h	XY_BER_CNTRL_3	W	XY_STLTP_LN_MASK[3:0]				-	-	XY_RST_STLTP_FLAG	XY_RST_XBERT_FLAG	F0h
	XY_AB_SWAP_STATUS	R			XBERT_FLAG	XY_STLTP_ERR_FLAG	XY_AB_SWAP_LN3	XY_AB_SWAP_LN2	XY_AB_SWAP_LN1	XY_AB_SWAP_LN0	uu
0104h 0304h 0504h	XY_XBERT_CNT_LSB	R	XY_XBERT_CNT[7:0]								uu

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0105h 0305h 0505h	XY_XBERT_CNT_MSB	R	XY_XBERT_CNT[15:8]								uu
010Ch 030Ch 050Ch	XY_FIRSTBER_JSTPAT	R	NOT USED	XY_FIRSTBER_JSTPAT[6:0]							uu
0110h 0310h 0510h	XY_FIRSTXBER-PAT_LSB	R	XY_FIRSTBERPAT[7:0]								uu
0111h 0311h 0511h	XY_FIRSTXBER-PAT_MSB	R	NOT USED					XY_FIRSTBERPAT_LN0[9:8]			uu
0112h 0312h 0512h	XY_BER_LEVEL_P_LN0_LSB	R/W	XY_BER_LEVEL_P_LN0[7:0]								00h
0113h 0313h 0513h	XY_BER_LEVEL_P_LN0_MSB	R/W	XY_BER_LEVEL_P_LN0[15:8]								00h
0114h 0314h 0514h	XY_BER_LEVEL_P_LN1_LSB	R/W	XY_BER_LEVEL_P_LN1[7:0]								00h
0115h 0315h 0515h	XY_BER_LEVEL_P_LN1_MSB	R/W	XY_BER_LEVEL_P_LN1[15:8]								00h
0116h 0316h 0516h	XY_BER_LEVEL_P_LN2_LSB	R/W	XY_BER_LEVEL_P_LN2[7:0]								00h
0117h 0317h 0517h	XY_BER_LEVEL_P_LN2_MSB	R/W	XY_BER_LEVEL_P_LN2[15:8]								00h
0118h 0318h 0518h	XY_BER_LEVEL_P_LN3_LSB	R/W	XY_BER_LEVEL_P_LN3[7:0]								00h
0119h 0319h 0519h	XY_BER_LEVEL_P_LN3_MSB	R/W	XY_BER_LEVEL_P_LN3[15:8]								00h
011Ah 031Ah 051Ah	XY_MAN_MFB_LN0	W		XY_MAN_MFB_LN0[6:0]							20h
		R		XY_MFB_LN0[6:0]							uu
011Bh 031Bh 051Bh	XY_MAN_MFB_LN1	W		XY_MAN_MFB_LN1[6:0]							20h
		R		XY_MFB_LN1[6:0]							uu
011Ch 031Ch 051Ch	XY_MAN_MFB_LN2	W		XY_MAN_MFB_LN2[6:0]							20h
		R		XY_MFB_LN2[6:0]							uu
011Dh 031Dh 051Dh	XY_MAN_MFB_LN3	W		XY_MAN_MFB_LN3[6:0]							20h
		R		XY_MFB_LN3[6:0]							uu
011Eh 031Eh 051Eh	XY_FORCE_MFB_LN(X)	R/W					XY_-FORCE_MF-B_LN3	XY_FORCE_MF-B_LN2	XY_-FORCE_MF-B_LN1	XY_FORCE_M-FB_LN0	00h

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Configuration Data of Physical Lane 0 DAC XY											
0120h 0320h 0520h	XY_P_LN0_CFG_0	R	XY_P_LN0_DID[7:0]								uu
0121h 0321h 0521h	XY_P_LN0_CFG_1	R	XY_P_LN0_ADJCNT[3:0]				XY_P_LN0_BID[3:0]				uu
0122h 0322h 0522h	XY_P_LN0_CFG_2	R		XY_P_LN0_-ADJDIR	XY_P_LN0_PH-ADJ	XY_P_LN0_LID[4:0]					uu
0123h 0323h 0523h	XY_P_LN0_CFG_3	R	XY_P_LN0_SCR	NOT USED		XY_P_LN0_L[4:0]					uu
0124h 0324h 0524h	XY_P_LN0_CFG_4	R	XY_P_LN0_F[7:0]								uu
0125h 0325h 0525h	XY_P_LN0_CFG_5	R				XY_P_LN0_K[4:0]					uu
0126h 0326h 0526h	XY_P_LN0_CFG_6	R	XY_P_LN0_M[7:0]								uu
0127h 0327h 0527h	XY_P_LN0_CFG_7	R	XY_P_LN0_CS[1:0]		NOT USED	XY_P_LN0_N[4:0]					uu
0128h 0328h 0528h	XY_P_LN0_CFG_8	R	XY_P_LN0_SUBCLASSV[2:0]			XY_P_LN0_N[4:0]'					uu
0129h 0329h 0529h	XY_P_LN0_CFG_9	R	XY_P_LN0_JESDV[2:0]			XY_P_LN0_S[4:0]					uu
012Ah 032Ah 052Ah	XY_P_LN0_CFG_10	R	XY_P_LN0_HD	NOT USED		XY_P_LN0_CF[4:0]					uu
012Bh 032Bh 052Bh	XY_P_LN0_CFG_11	R	XY_P_LN0_RES1[7:0]								uu
012Ch 032Ch 052Ch	XY_P_LN0_CFG_12	R	XY_P_LN0_RES2[7:0]								uu
012Dh 032Dh 052Dh	XY_P_LN0_CFG_13	R	XY_P_LN0_FCHK[7:0]								uu
DLP strobe read data for Physical Lane 0 or 1 DAC XY											
012Eh 032Eh 052Eh	XY_LN10_SAMPLE_LSB	R	XY_LN10_SAMPLE[7:0]								uu
012Fh 032Fh 052Fh	XY_LN10_SAM-PLE_MSB	R	XY_LN10_SAMPLE[15:8]								uu

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Configuration Data of Physical Lane 1 DAC XY											
0130h 0330h 0530h	XY_P_LN1_CFG_0	R	XY_P_LN1_DID[7:0]								uu
0131h 0331h 0531h	XY_P_LN1_CFG_1	R	XY_P_LN1_ADJCNT[3:0]				XY_P_LN1_BID[3:0]				uu
0132h 0332h 0532h	XY_P_LN1_CFG_2	R		XY_P_LN1_-ADJDIR	XY_P_LN1_PH-ADJ	XY_P_LN1_LID[4:0]					uu
0133h 0333h 0533h	XY_P_LN1_CFG_3	R	XY_P_LN1_SCR	NOT USED		XY_P_LN1_L[4:0]					uu
0134h 0334h 0534h	XY_P_LN1_CFG_4	R	XY_P_LN1_F[7:0]								uu
0135h 0335h 0535h	XY_P_LN1_CFG_5	R				XY_P_LN1_K[4:0]					uu
0136h 0336h 0536h	XY_P_LN1_CFG_6	R	XY_P_LN1_M[7:0]								uu
0137h 0337h 0537h	XY_P_LN1_CFG_7	R	XY_P_LN1_CS[1:0]		NOT USED	XY_P_LN1_N[4:0]					uu
0138h 0338h 0538h	XY_P_LN1_CFG_8	R	XY_P_LN1_SUBCLASSV[2:0]			XY_P_LN1_N[4:0]'					uu
0139h 0339h 0539h	XY_P_LN1_CFG_9	R	XY_P_LN1_JESDV[2:0]			XY_P_LN1_S[4:0]					uu
013Ah 033Ah 053Ah	XY_P_LN1_CFG_10	R	XY_P_LN1_HD	NOT USED		XY_P_LN1_CF[4:0]					uu
013Bh 033Bh 053Bh	XY_P_LN1_CFG_11	R	XY_P_LN1_RES1[7:0]								uu
013Ch 033Ch 053Ch	XY_P_LN1_CFG_12	R	XY_P_LN1_RES2[7:0]								uu
013Dh 033Dh 053Dh	XY_P_LN1_CFG_13	R	XY_P_LN1_FCHK[7:0]								uu
DLP strobe Lane selection for Physical Lane 0 and 1 DAC XY											
013Eh 033Eh 053Eh	XY_LN10_SELECT	W	NOT USED							XY_LN10_SEL	00h

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Configuration Data of Physical Lane 2 DAC XY											
0140h 0340h 0540h	XY_P_LN2_CFG_0	R	XY_P_LN2_DID[7:0]								uu
0141h 0341h 0541h	XY_P_LN2_CFG_1	R	XY_P_LN2_ADJCNT[3:0]				XY_P_LN2_BID[3:0]				uu
0142h 0342h 0542h	XY_P_LN2_CFG_2	R		XY_P_LN2_-ADJDIR	XY_P_LN2_PH-ADJ	XY_P_LN2_LID[4:0]					uu
0143h 0343h 0543h	XY_P_LN2_CFG_3	R	XY_P_LN2_SCR	NOT USED		XY_P_LN2_L[4:0]					uu
0144h 0344h 0544h	XY_P_LN2_CFG_4	R	XY_P_LN2_F[7:0]								uu
0145h 0345h 0545h	XY_P_LN2_CFG_5	R				XY_P_LN2_K[4:0]					uu
0146h 0346h 0546h	XY_P_LN2_CFG_6	R	XY_P_LN2_M[7:0]								uu
0147h 0347h 0547h	XY_P_LN2_CFG_7	R	XY_P_LN2_CS[1:0]		NOT USED	XY_P_LN2_N[4:0]					uu
0148h 0348h 0548h	XY_P_LN2_CFG_8	R	XY_P_LN2_SUBCLASSV[2:0]			XY_P_LN2_N[4:0]'					uu
0149h 0349h 0549h	XY_P_LN2_CFG_9	R	XY_P_LN2_JESDV[2:0]			XY_P_LN2_S[4:0]					uu
014Ah 034Ah 054Ah	XY_P_LN2_CFG_10	R	XY_P_LN2_HD	NOT USED		XY_P_LN2_CF[4:0]					uu
014Bh 034Bh 054Bh	XY_P_LN2_CFG_11	R	XY_P_LN2_RES1[7:0]								uu
014Ch 034Ch 054Ch	XY_P_LN2_CFG_12	R	XY_P_LN2_RES2[7:0]								uu
014Dh 034Dh 054Dh	XY_P_LN2_CFG_13	R	XY_P_LN2_FCHK[7:0]								uu
DLP strobe read data for Physical Lane 0 or 1 DAC XY											
014Eh 034Eh 054Eh	XY_LN32_SAMPLE_LSB	R	XY_LN32_SAMPLE[7:0]								uu
014Fh 034Fh 054Fh	XY_LN32_SAM-PLE_MSB	R	XY_LN32_SAMPLE[15:8]								uu

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Configuration Data of Physical Lane 3 DAC XY											
0150h 0350h 0550h	XY_P_LN3_CFG_0	R	XY_P_LN3_DID[7:0]								uu
0151h 0351h 0551h	XY_P_LN3_CFG_1	R	XY_P_LN3_ADJCNT[3:0]				XY_P_LN3_BID[3:0]				uu
0152h 0352h 0552h	XY_P_LN3_CFG_2	R		XY_P_LN3_-ADJDIR	XY_P_LN3_PH-ADJ	XY_P_LN3_LID[4:0]					uu
0153h 0353h 0553h	XY_P_LN3_CFG_3	R	XY_P_LN3_SCR	NOT USED		XY_P_LN3_L[4:0]					uu
0154h 0354h 0554h	XY_P_LN3_CFG_4	R	XY_P_LN3_F[7:0]								uu
0155h 0355h 0555h	XY_P_LN3_CFG_5	R				XY_P_LN3_K[4:0]					uu
0156h 0356h 0556h	XY_P_LN3_CFG_6	R	XY_P_LN3_M[7:0]								uu
0157h 0357h 0557h	XY_P_LN3_CFG_7	R	XY_P_LN3_CS[1:0]		NOT USED	XY_P_LN3_N[4:0]					uu
0158h 0358h 0558h	XY_P_LN3_CFG_8	R	XY_P_LN3_SUBCLASSV[2:0]			XY_P_LN3_N[4:0]'					uu
0159h 0359h 0559h	XY_P_LN3_CFG_9	R	XY_P_LN3_JESDV[2:0]			XY_P_LN3_S[4:0]					uu
015Ah 035Ah 055Ah	XY_P_LN3_CFG_10	R	XY_P_LN3_HD	NOT USED		XY_P_LN3_CF[4:0]					uu
015Bh 035Bh 055Bh	XY_P_LN3_CFG_11	R	XY_P_LN3_RES1[7:0]								uu
015Ch 035Ch 055Ch	XY_P_LN3_CFG_12	R	XY_P_LN3_RES2[7:0]								uu
015Dh 035Dh 055Dh	XY_P_LN3_CFG_13	R	XY_P_LN3_FCHK[7:0]								uu
DLP strobe Lane selection for Physical Lane 2 and 3 DAC XY											
015Eh 035Eh 055Eh	XY_LN32_SELECT	W	NOT USED							XY_LN32_SEL	00h

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
RX PHY controls DAC XY											
0160h 0360h 0560h	XY_REF_ENA	R/W						XY_HS_REF_TUNE_ENABLE	XY_HS_REF_CALIBRATE_ENABLE	XY_HS_REF_ENABLE	05h
0162h 0362h 0562h	XY_HS_RX_CDR_DIV	R/W	XY_HS_RX-_CDR_LOW_-SPEED_ENABLE	XY_HS_RX_CDR_DIVM[1:0]		XY_HS_RX_CDR_DIVN[4:0]					02h
0167h 0367h 0567h	XY_HS_RX_EQ_CNTRL					XY_HS_RX-_EQ_AUTO_ZERO_ENABLE	XY_HS_RX-_3_EQ_ENABLE	XY_HS_RX-_2_EQ_ENABLE	XY_HS_RX-_1_EQ_ENABLE	XY_HS_RX-_0_EQ_ENABLE	1Fh
0168h 0368h 0568h	XY_HS_RX_0_EQ_GAIN	R/W						XY_HS_RX_0_EQ_IF_GAIN[2:0]			03h
0169h 0369h 0569h	XY_HS_RX_1_EQ_GAIN	R/W						XY_HS_RX_1_EQ_IF_GAIN[2:0]			03h
016Ah 036Ah 056Ah	XY_HS_RX_2_EQ_GAIN	R/W						XY_HS_RX_2_EQ_IF_GAIN[2:0]			03h
016Bh 036Bh 056Bh	XY_HS_RX_3_EQ_GAIN	R/W						XY_HS_RX_3_EQ_IF_GAIN[2:0]			03h
0170h 0370h 0570h	XY_HS_RX_RT_VCM	R/W			XY_HS_RX-_RT_VCMSEL	XY_HS_RX_RT_VCMREF[4:0]					25h
0171h 0371h 0571h	XY_HS_RX_RT_CNTRL	R/W	XY_HS_RX-_3_RT_HIZ_ENABLE	XY_HS_RX-_2_RT_HIZ_ENABLE	XY_HS_RX-_1_RT_HIZ_ENABLE	XY_HS_RX-_0_RT_HIZ_ENABLE	XY_HS_RX-_3_RT_ENABLE	XY_HS_RX-_2_RT_ENABLE	XY_HS_RX-_1_RT_ENABLE	XY_HS_RX-_0_RT_ENABLE	0Fh
0172h 0372h 0572h	XY_HS_RX_0_RT_REFSIZE	R/W	XY_HS_RX_0_RT_REFSIZE[8:1]								50h
0173h 0373h 0573h	XY_HS_RX_1_RT_REFSIZE	R/W	XY_HS_RX_1_RT_REFSIZE[8:1]								50h
0174h 0374h 0574h	XY_HS_RX_2_RT_REFSIZE	R/W	XY_HS_RX_2_RT_REFSIZE[8:1]								50h
0175h 0375h 0575h	XY_HS_RX_0_RT_REFSIZE	R/W	XY_HS_RX_3_RT_REFSIZE[8:1]								50h
0176h 0376h 0576h	XY_HS_RX_X_RT_REFSIZE	R/W					XY_HS_RX-_3_RT_REFSIZE[0]	XY_HS_RX-_2_RT_REFSIZE[0]	XY_HS_RX-_1_RT_REFSIZE[0]	XY_HS_RX-_0_RT_REFSIZE[0]	00h

Table 50. Dual DAC core block register allocation map (DAC AB and/or DAC CD)

Addr.	Register name	R/W	Bit definition								Default
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
SYNC levels and Test mode DAC XY											
017Dh 037Dh 057Dh	XY_SYNC_CFG_CNTRL	R/W	XY_SYNC_ENABLE	XY_SYNC_SET_VCM[2:0]			NOT USED	XY_SYNC_SET_LEVEL[2:0]			C4h
017Eh 037Eh 057Eh	XY_SYNC_SEL_CNTRL	R/W	XY_SYNC_TEST_DATA_ENABLE	NOT USED	XY_SYNC_TEST_DATA_SEL[1:0]						00h

11.13.3 Device common register bit definition

Table 51 shows the detailed description of the bit definition of the common device register.

Table 51. Common registers for DACs ABCD (Continued)
Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
				SPI configuration - Device ID		
0000h	R/W	SPI_CONFIG_A	7	SPI_RST	0	no action
					1	set all registers to their defaults (except 0000h/0001h)
			6	NOT USED		
			5	SPI_ASCEND	0	ascend off (auto decrement next address)
					1	ascend on (auto increment next address)
			4	SPI_4W	0	3 wires SPI interface
					1	4 wires SPI interface
			3:0	MIRROR[3:0]		mirror check : write mirror [4:7]
0001h	R/W	SPI_CONFIG_B	7	SPI_SINGLE	0	streaming mode enable
					1	one byte mode
			6	NOT USED		
			5	SPI_READBUF	0	read back resynchronized registers
					1	read back buffer registers (i.c.o . double buffers)
			4:0	NOT USED		
0002h	R/W	DEV_PWR_MODE	7:2	NOT USED		
			1:0	DEV_PWR_MODE[1:0]		reserved for future usage
0003h	R	CHIP_TYPE	7:0	CHIP_TYPE[7:0]		chip type : high speed DAC
0004h	R	CHIP_ID_0	7:0	CHIP_ID_0[7:0]		identification of the chip
0005h	R	CHIP_ID_1	7:0	CHIP_ID_1[7:0]		identification of the chip
0006h	R	CHIP_VERSION	7:0	CHIP_VS[7:0]		version
000Ch	R	VENDOR_ID_LSB	7:0	VENDOR_ID[7:0]		vendor identification (LSB)
000Dh	R	VENDOR_ID_MSB	7:0	VENDOR_ID[15:8]		vendor identification (MSB)
000Fh	R/W	SPI_CONFIG_C	7:1	NOT USED		
			0	TRANSFER_BIT	0	double buffer registers preserves current value
					1	double buffer registers are updated with value set via spi (auto-clear bit)
				Device Main configuration		

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0020h	R/W	MAINCONTROL	6:4	RE_INIT_MODE[2:0]	000	DCMSU ignores reinit
					001	restart rx_phy
					010	restart rx_phy and cdi
					011	restart rx_phy, cdi and dsp
					100	restart rx_phy, cdi, dsp and adpll
			3	NOT USED		
			2	FORCE_RESET_PCLK	0	release reset_pclk
					1	force reset_pclk
			1	FORCE_RESET_DCLK	0	release reset_dclk
					1	force reset_dclk
			0	FORCE_RESET_WCLK	0	release reset_wclk
					1	force reset_wclk
0021h	R/W	DCSMU_AUTO_CNTRL	7	MAN_PON_CNTRL	0	pon_rx-phy and pon_dacs controlled by dcsmu
					1	manual control of pon_rx_phy and pon_dacs
			6	IGNORE_ASP_ERROR	0	no action
					1	dcmsu ignores absence of adpll_lock
			5	AUTO_REG_TRANSFER	0	no action
					1	reg_transfer when force_resets are released
			4	FORCE_LOCKDET	0	no action
					1	ignore internal lockdetectors
			3	AUTO_QUICK_ENA	0	don't enable rx-phy after power-up/spi-reset
					1	enable rx-phy after power-up/spi-reset
			2	AUTO_LOCKDET_ENA	0	disable automatic lockdetection
					1	enable automatic lockdetection
			1	AUTO_ADPLL_STARTUP	0	no action
					1	dcmsu will start up adpll
			0	AUTO_ADPLL_MODE	0	use linear mode for adpll startup
					1	use bangbang mode for adpll startup
0022h	R/W	POFF	7:0	POFF_RX[7:0]		power_off for rx_ln(i)
0028h	R/W	RX_PHY_LOCK	0	COMBINE_RX_PHY_LOCK	0	RX_PHY_LOCK are treated independently
					1	RX_PHY_LOCK are combined

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0029h	W	DCSMU_AUTO_CTRL1	7	REINIT_MC_ALARM_DIS	0	mc_alarm will be uses as re-init trigger
					1	disable usage of mc_alarm as re-init trigger
			6	DCMSU_ADPLL_ENA_INIT	0	auto-adpll-su 'resets' the adpll (via adpll_soft_rst_n)
					1	auto-adpll-su doesn't reset the adpll
			5	NOT USED		
			4	WD_SYNC_SENSITIVITY	0	watchdog reset at rising-edge SYNC ('0' -> '1')
					1	watchdog reset when SYNC = '1'
			3	WD_REINIT_DISABLE	0	when watchdog expires an re-init will be invoked
					1	watchdog will not invoke re-init
			2	WD_BARK_ONCE	0	watchdog timer keeps checking over and over again
					1	watchdog timer will check only once
			1	WD_DISABLE_CD	0	watchdog timer (cd) will be enabled
					1	disable usage of watchdog timer (cd)
			0	WD_DISABLE_AB	0	watchdog timer (ab) will be enabled
					1	disable usage of watchdog timer (ab)
	R	WD_STATUS	7:6	NOT USED	00	
			5	WD_CNT_INACTIVE_CD		watch_dog inactive (cd-site)
			4	WD_CNT_END_CD		watch_dog expired (cd-site)
			3:2	NOT USED	00	
			1	WD_CNT_INACTIVE_AB		watch_dog inactive (cd-site)
			0	WD_CNT_END_AB		watch_dog expired (cd-site)
002Ah	W	PD_ANA_CNTRL	7:6	NOT USED	00	
			5	RFTX_ENA_PD_ANA_CD	0	pd_analog_cd depends on pd_ana_enable_cd
					1	pd_analog_cd depends on rftx_ena
			4	PD_ANA_ENABLE_CD	0	no action
					1	power down analog_cd (non-clk modules only)
			3:2	NOT USED		
			1	RFTX_ENA_PD_ANA_AB	0	pd_analog_ab depends on pd_ana_enable_ab
					1	pd_analog_ab depends on rftx_ena
			0	PD_ANA_ENABLE_AB	0	no action
					1	power down analog_ab (non-clk modules only
	R	ANA_RES_STATUS	7:4	ANA_RES_CD[3:0]		ana_res_cd[3:0]
			3:0	ANA_RES_AB[3:0]		ana_res_ab[3:0]

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
002Bh	R/W	CDI_CNTRL	7	SR_CDI_CD	0	no action
					1	soft reset cdi_cd
			6	CDI_MS_CD	0	cdi_cd runs as master
					1	cdi_cd runs as slave
			5:4	CDI_MODE_CD[1:0]	00	cdi_mode 0 (^2 modes)
					01	cdi_mode 1 (^4 modes)
					10	cdi_mode 2 (^8 modes)
					11	unspecified
			3	SR_CDI_AB	0	no action
					1	soft reset cdi_ab
			2	CDI_MS_AB	0	cdi_ab runs as master
					1	cdi_ab runs as slave
			1:0	CDI_MODE_AB[1:0]	00	cdi_mode 0 (^2 modes)
					01	cdi_mode 1 (^4 modes)
					10	cdi_mode 2 (^8 modes)
					11	unspecified
002Ch	W	SRC_SELECT_CNTRL	7	NOT USED		
			6	MDS_SELECT_E	0	mds_ana_E controlled by mds_cntrl_ab
					1	mds_ana_E controlled by mds_cntrl_cd
			5:4	SYNCB_SELECT_E[1:0]	00	syncb_E <= syncb_ab
					01	syncb_E <= syncb_cd
					10	syncb_E <= xbert_flag_ab
					11	syncb_E <= xbert_flag_cd
			3	NOT USED		
			2	MDS_SELECT_W	0	mds_ana_W controlled by mds_cntrl_ab
					1	mds_ana_W controlled by mds_cntrl_cd
			1:0	SYNCB_SELECT_W[1:0]	00	syncb_W <= syncb_ab
					01	syncb_W <= syncb_cd
					10	syncb_W <= xbert_flag_ab
					11	syncb_W <= xbert_flag_cd
	R	MON_SYNCB	7	NO_ACT_F20_FLAG_CD		indicates inactivity of rx-phy clocks (cd)
			6	ILA_RCV_FLAG_CD		indicates that ILA-sequence has been received (cd)
			5	XBERT_FLAG_CD		xbert_flag as generated by DLP_cd (xbert_module)
			4	SYNCB_ CD		syncb as generated by DLP_cd (lane-controller)
			3	NO_ACT_F20_FLAG_AB		indicates inactivity of rx-phy clocks (ab)
			2	ILA_RCV_FLAG_AB		indicates that ILA-sequence has been received (ab)
			1	XBERT_FLAG_AB		xbert_flag as generated by DLP_cd (xbert_module)
			0	SYNCB_ AB		syncb as generated by DLP_cd (lane-controller)
002Eh	R/W	DCSMU_WDTIMER0		WATCHDOG[7:0]		set watchdog (LSB) @ WCLK)
002Fh	R/W	DCSMU_WDTIMER1		WATCHDOG[15:8]		set watchdog (MSB) @ WCLK)

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0030h	R/W	IO_MUX_CNTRL0	7:0	IO_SELECT_0[7:0]		io_mux select for io[0]
0031h	R/W	IO_MUX_CNTRL1	7:0	IO_SELECT_1[7:0]		io_mux select for io[1]
0032h	R/W	IO_MUX_CNTRL2	7:0	IO_SELECT_2[7:0]		io_mux select for io[2]
0033h	R/W	IO_MUX_CNTRL3	7:0	IO_SELECT_3[7:0]		io_mux select for io[3]
0034h	R/W	IO_MUX_CNTRL4	7:0	IO_SELECT_4[7:0]		io_mux select for io[3 to 0]
0035h	R/W	IO_CNTRL	7:4	IO_ENA[3:0]		Specify Input (1) or Output (0) mode for IO[3 to 0]
			3:2	IO_EHS[1:0]		EHS drive control IO[3 to 0]
			1:0	SDO_EHS[1:0]		EHS drive control SDO/SDIO
0036h	R/W	RF_TX_INPUT_CNTRL	7	NOT USED		
			6	RF_TX_XOR_CD	0	rf_tx_in_cd signal will enable the DAC output
					1	not(rf_tx_in_cd) signal will enable the DAC output
			5:4	RF_TX_SEL_CD[1:0]	00	rf_tx_in_cd signal is controlled by io[0] pin
					01	rf_tx_in_cd signal is controlled by io[1] pin
					10	rf_tx_in_cd signal is controlled by io[2] pin
					11	rf_tx_in_cd signal is controlled by io[3] pin
			3	NOT USED		
			2	RF_TX_XOR_AB	0	rf_tx_in_ab signal will enable the DAC output
					1	not(rf_tx_in_ab) signal will enable the DAC output
			1:0	RF_TX_SEL_AB[1:0]	00	rf_tx_in_ab signal is controlled by io[0] pin
					01	rf_tx_in_ab signal is controlled by io[1] pin
					10	rf_tx_in_ab signal is controlled by io[2] pin
					11	rf_tx_in_ab signal is controlled by io[3] pin
0037h	W	DCSMU_XTIMER0	7:0	RXPHY_ENA_LOW_TIME[7:0]		set low time rx_phy_ena (ana_res = “000”)
	R	MON_MISC_AB	7	MON_DCLK_XY_STOP		cdi clock domain phase monitor locked (@ 0x5)
			6:4	NOT USED		
			3:0	MON_DCLK_AB[3:0]		cdi clock domain phase monitor
0038h	W	DCSMU_XTIMER1	7:0	CDR_ENA_LOW_TIME[7:0]		set low time cdr_ena (ana_res = “001”)
	R	MON_DCLK_AB_FLAGS	7:0	MON_DCLK_AB_FLAGS[7:0]		cdi clock domain phase monitor flags
0039h	W	DCSMU_XTIMER2	7:0	WAIT_FOR_LOCK_TIME[7:0]		sets wait-time before lockcheck (ana_res = “011”)
	R	MON_MISC_CD	7	MON_DCLK_CD_STOP		cdi clock domain phase monitor locked (@ 0x5)
			6:4	NOT USED		
			3:0	MON_DCLK_CD[3:0]		cdi clock domain phase monitor
003Ah	W	DCSMU_XTIMER3	7:0	WAIT_FOR_TRACK_TIME[7:0]		sets wait-time before tracking (ana_res = “101”)
	R	MON_DCLK_CD_FLAGS	7:0	MON_DCLK_CD_FLAGS[7:0]		cdi clock domain phase monitor flags
003Bh	W	DCSMU_XTIMER4	7:0	TRACK_RUNIN_TIME[7:0]		sets track runin time (ana_res = “110”)
	R	MON-DCMSU_0	7:0	RESERVED		reserved
1A0h	R/W	AUX_DAC_HRESab	7	AUX_DAC_HRESab	0	set AUX DAC ab in high resolution mode
					1	set AUX DAC ab in normal resolution mode
			6:0		0	reserved (=0)

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
247h	R/W	AUX_DAC_HREScd	7:1	AUX_DAC_HREScd	0	reserved (0)
			0	AUX_DAC_HREScd	0	set AUX DAC cd in high resolution mode
					1	set AUX DAC cd in normal resolution mode
Common Quad DAC Configuration Controls						
01ACh	R/W	PON_CFG_NC	7	PON_ISOURCE_CLKDIV_2	0	clkdiv_2 bias current disabled (powerdown)
					1	clkdiv_2 bias current enabled
			6	PON_ISOURCE_CLKDIV_1	0	clkdiv_1 bias current disabled (powerdown)
					1	clkdiv_1 bias current enabled
			5	PON_ISOURCE_ADPLLBUF_IBIAS	0	cmlbuf _ibias bias current disabled (powerdown)
					1	cmlbuf_ibias bias current enabled
			4	PON_ISOURCE_ADPLLBUF_ICAS	0	cmlbuf_icas bias current disabled (powerdown)
					1	cmlbuf_icas bias current enabled
			3	PON_ISOURCE_CLKCAS	0	clkcas bias current disabled (powerdown)
					1	clkcas bias current enabled
			2	PON_ISOURCE_CLK	0	clk bias current disabled (powerdown)
					1	clk bias current enabled
			1	PON_BIAS_COMMON	0	common bias current disabled (powerdown)
					1	common bias current enabled
			0	PON_GAP	0	bandgap references switched off
					1	bandgap references switched on
01ADh	R/W	CLKGENCFG1	3	WCLK_DIV_BYPASS	0	wclk depends on wclk_div_sel
					1	wclk = dacclk
			2:0	WCLK_DIV_SEL[2:0]	000	wclk = dacclk 2
					001	wclk = dacclk 3
					010	wclk = dacclk 4
					011	wclk = dacclk 6
					100	wclk = dacclk 8
					101	wclk = dacclk 12
					110	wclk = dacclk 16
					111	wclk = dacclk 24

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
01AFh	R/W	CLKDIV_CFG	4	CLK_DIV_SEL_FREQ	0	high frequency mode
					1	low frequency mode
			3	CLK_DIV_BYPASS	0	dacclk depends on clkdiv_cfg
					1	dacclk = clkin
			2	CLK_DIV_RESET	0	no action
					1	reset dacclkdivider
			1:0	CLK_DIV_SEL[1:0]	00	dacclk = clkin/2
					01	dacclk = clkin/4
					10	dacclk = clkin/6
					11	dacclk = clkin/8

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
				Temperature Sensor		
01B3h	R/W	TEMPS_CNTRL	7	TEMP_SENS_PON	0	temperature sensor disabled (power down)
					1	temperature sensor enabled
			6	TS_RST_ALARM	0	no action
					1	reset temp_sensor_alarm flag
			5	TS_FULLRANGE	0	sweep 22...63
					1	sweep 0..63
			4	TS_TOGGLE	0	wait for 0 -> 1 transition
					1	wait for 1 -> 0 transition
			3	TS_RST_MAX	0	no action
					1	reset temp_max_value
			2	TS_RST_MIN	0	no action
					1	reset temp_min value
			1:0	TS_MODE[1:0]	00	raw mode (direct access to tempsensor)
					01	one shot measurement
					10	continuous measurement
					11	continuous measurement (hold temp_alarm_flag)
01B4h	Wr	TEMPS_LEVEL	5:0	TEMP_SEL_MAN[5:0]		usage depends on ts_mode
					ts_mode =00"	applied direct to temp_sensor
					ts_mode = others"	sets threshold for temp_alarm
	R	TEMPS_OUT	7	TEMP_SENS_OUT		temp_sensor_output (for use in rawmode)
			6	TEMP_ALARM		temp_actual > temp_threshold flag
			5:0	TEMP_ACTUAL[5:0]		temp_actual (result last measurement)
01B5h	Wr	TEMPS_MAX	7:0	TS_CLKDIV[7:0]		sets clockfrequency temp_sensor_cntrl (dclk / ts_clkdiv)
	R	TEMPS_MAX	5:0	TEMP_MAX[5:0]		maximum temp_actual found since last ts_rst_max
01B6h	Wr	TEMPS_TIMER	7:0	TS_TIMER[7:0]		sets nr_of_waitcycles between measurements
	R	TEMPS_MIN	5:0	TEMP_MIN[5:0]		minimum temp_actual found since last ts_rst_min
01B7h	Wr	MDS_IO_CNTRL0	7	PON_ISOURCE_MDS_E	0	mds_io_E biascurrent disabled (powerdown)
					1	mds_io_E biascurrent enabled
			6:5	NOT_USED	0	not used
			4	MDS_SEL_RT_E	0	mds_io_E internal resistor_termination inactive
					1	mds_io_E internal resistor_termination active
			3	PON_ISOURCE_MDS_W	0	mds_io_W biascurrent disabled (powerdown)
					1	mds_io_W biascurrent enabled
			2:1	NOT_USED	0	not used
			0	MDS_SEL_RT_W	0	mds_io_W internal resistor_termination inactive
					1	mds_io_W internal resistor_termination active

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
01B8h	Wr	MDS_IO_CNTRL1	7	MDS_RESYNC_SYSREF	0	sysref_W is passed direct to the EL-detector_W
					1	sysref_W is resynchronized to clkin
			6	NOT USED	0	not used
			5	MDS_SYSREF_POL_E	0	polarity of sysref_E is as received
					1	polarity of sysref_E is swapped internally
			4	MDS_SYSREF_POL_W	0	polarity of sysref_W is as received
					1	polarity of sysref_W is swapped internally
			3:2	MDS_SET_DELAY_E[1:0]		tweaks ‘equal’-window for capturing sysref_E
			1:0	MDS_SET_DELAY_W[1:0]		tweaks ‘equal’-window for capturing sysref_W
01C8h	R/W	ADPLL_PREDIV	3:0	ADPLL_PREDIV[3:0]		sets predividerratio
					0000	PCLK = CLK_IN /2
					0001	PCLK = CLK_IN /3
					0010	PCLK = CLK_IN /4
					0011	PCLK = CLK_IN /5
					0100	PCLK = CLK_IN /6
					0101	PCLK = CLK_IN /7
					0110	PCLK = CLK_IN /8
					0111	PCLK = CLK_IN /9
					1000	PCLK = CLK_IN /4
					1001	PCLK = CLK_IN /6
					1010	PCLK = CLK_IN /8
					1011	PCLK = CLK_IN /10
					1100	PCLK = CLK_IN /12
					1101	PCLK = CLK_IN /14
					1110	PCLK = CLK_IN /16
					1111	PCLK = CLK_IN /18
01C9h	R/W	ADPLL_POSTDIV	2:0	ADPLL_POSTDIV[2:0]		sets post divider ratio
					000	DAC_CLK = DCO_FREQ /2
					001	DAC_CLK = DCO_FREQ /3
					010	DAC_CLK = DCO_FREQ /4
					011	DAC_CLK = DCO_FREQ /5
					100	DAC_CLK = DCO_FREQ /6
					101	DAC_CLK = DCO_FREQ /7
					110	DAC_CLK = DCO_FREQ /8
					111	DAC_CLK = DCO_FREQ /9

Table 51. Common registers for DACs ABCD (Continued)

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
01CAh	W	ADPLL_CNTRL	7	ADPLL_SOFT_RST_N		0: reset adpll 1: normal operation
			6	ENA_DRIFT_COMP		0: ADPLL start up sequence will NOT enable temperature drift compensation 1:ADPLL start up sequence will enable temperature drift compensation
			5	ADPLL_LOCK_TOGGLE		0: adpll_lock_xor <- adpll_lock 1: adpll_lock_xor <- not adpll_lock
			4	PON_PCLK		0: pclk divider output disabled (power down) 1: pclk divider output enabled
			3	ADPLL_DIG_PON		0: LDO adpll_dig supply disabled 1: LDO adpll_dig supply active
			2	ADPLL_PREDIV_PON		0: ADPLL predivider disabled (power down) 1: ADPLL predivider active
			1	ADPLL_PREDIV_BYPASS		0: Fref <- PCLK 1: Fref <- Fclkin
			0	ADPLL_BYPASS		0: DAC core Clock = DCO_clock / Post_divider ratio 1: DAC core Clock = Fclkin (straight input)
	R	ADPLL_STATUS	7:5	NOT USED	000	
			4	ADPLL_DC_READY		indicates that su-controller has finished dc_setup
			3	ADPLL_LIN_RDY		indicates that su-controller has finished lin_setup
			2	ADPLL_BB_RDY		indicates that su-controller has finished bangbang_setup
			1	FORCE_ADPLL_LOCKED		indicates if DCMSU has forced lock for su_controller
			0	ADPLL_LOCKED_XOR		indicates if ADPLL is locked
01CCh	R/W	ADPLL_DCO_CTF_0	7:0	ADPLL_DCO_CTF[7:0]		DCO center frequency tuning
01CDh	R/W	ADPLL_DCO_CTF_1	7:0	ADPLL_DCO_CTF[15:8]		DCO center frequency tuning

11.13.4 Dual core DAC register bit definition (DAC AB and/or DAC CD)

Table 52 shows the detailed description of the bit definition of both DAC AB and DAC CD dual core register.

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
				Dual DAC XY Core configuration		
				Analog Gain - Auxiliary DACs		
0040h 0240h 0440h	R/W	XY_PON_DDCCFG_0	7:6	NOT USED		
			5	XY_PON_BIAS	0	BIAS module disabled (powerdown)
					1	BIAS module enabled
			4	XY_PON_CGU	0	CGU disabled (powerdown)
					1	CGU enabled
			3	XY_PON_DAC_Y	0	DAC_Y powerdown
					1	DAC_Y enabled
			2	XY_PON_COMM_Y	0	commutator Y disabled (powerdown)
					1	commutator Y enabled
			1	XY_PON_DAC_X	0	DAC_X powerdown
					1	DAC_X enabled
			0	XY_PON_COMM_X	0	commutator X disabled (powerdown)
					1	commutator X enabled
0042h 0242h 0442h	Wr	XY_CLKGENCFG2	6	XY_CLKGEN_EN_DIV_DETECT(MON)	0	disable divide detector
					1	enable divide detector
			5	XY_CLKGEN_INIT_DIV	0	freerunning clkgendiv (when clkgen_en_div_detect = 0)
					1	clear clkgendiv (when clkgen_en_div_detect = 0)
			4:0	NOT USED		
	R		7	XY_CLK_MON_RESET (status)		0 : no action (read 0 : clk_mon_ok)
						1 : reset_clk_mon_flag (read 1 : clk_mon_fail)
0054h 0254h 0454h	R/W	XY_CLKDIV_SEL_PHASE[2:0]	7:0	XY_CLKDIV_SEL_PHASE[2:0]		dacclkphase=<sel_phase[2:0]>*Ts/2; see Table 27
0057h 0257h 0457h	R/W	XY_CSA_CFG_X_0	7:0	XY_CSA_BIAS_X[7:0]		CSA_X bias current (LSB) setting used to adjust DAC output full scale current
0058h 0258h 0458h	R/W	XY_CSA_CFG_X_0	7	XY_PON_CSA_X	0	csa_X biascurrent disabled (powerdown)
					1	csa_X biascurrent enabled
			6:3	NOT USED		
			2	XY_CSA_MULT2_X	0	csa_X bias current range doubling disabled
					1	csa_X bias current range doubling enabled
			1:0	XY_CSA_BIAS_X[9:8]		CSA_X bias current (MSB) setting used to adjust DAC output full scale current
0059h 0259h 0459h	R/W	XY_CSA_CFG_Y_0	7:0	XY_CSA_BIAS_Y[7:0]		CSA_Y bias current (LSB) setting used to adjust DAC output full scale current

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
005Ah 025Ah 045Ah	R/W	XY_CSA_CFG_Y_1	7	XY_PON_CSA_Y	0	csa_Y biascurrent disabled (powerdown)
					1	csa_Y biascurrent enabled
			6:3	NOT USED		
			2	XY_CSA_MULT2_Y	0	csa_Y bias current range doubling disabled
					1	csa_Y bias current range doubling enabled
			1:0	XY_CSA_BIAS_Y[9:8]		CSA_X bias current (MSB) setting used to adjust DAC output full scale current
005Bh 025Bh 045Bh	R/W	XY_AUX_CFG_X_0	7:0	XY_AUX_DAC_X[7:0]		aux dac X lsbs'
005Ch 025Ch 045Ch	R/W	XY_AUX_CFG_X_0	7	XY_PON_AUX_DAC_X	0	auxiliary dac_x disabled (powerdown)
					1	auxiliary dac_x enabled
			6:2	NOT USED		
			1:0	XY_AUX_DAC_X[9:8]		aux dac X msbs'
005Dh 025Dh 045Dh	R/W	XY_AUX_CFG_Y_0	7:0	XY_AUX_DAC_Y[7:0]		aux dac Y lsbs'
005Eh 025Eh 045Eh	R/W	XY_AUX_CFG_Y_1	7	XY_PON_AUX_DAC_Y	0	auxiliary dac_y disabled(powerdown)
					1	auxiliary dac_y enabled
			6:2	NOT USED		
			1:0	XY_AUX_DAC_Y[9:8]		aux dac Ymsbs'
Digital Signal Processing (DSP) for Dual DAC XY						
NCO Frequency- Phase correction						
0060h 0260h 0460h	R/W	XY_TXCFG	7	XY_NCO_EN	0	NCO disabled
					1	NCO enabled
			6	XY_NCO_LOWPOWER	0	NCO with 40 bits resolution
					1	NCO low resolution (only use reg XY_FREQNCO_B4)
			5	XY_INV_SINC_EN	0	Inverse sin(x)/x function disabled
					1	Inverse sin(x)/x function enabled
			4:2	XY_MODE[2:0]	000	no modulation
					001	positive upper single sideband upconversion
					010	positive lower single sideband upconversion
					011	negative upper single sideband upconversion
					100	negative lower single sideband upconversion
						others (undefined)
			1:0	XY_INT_FIR[1:0]	00	interpolation disabled (2x samplerepetition)
					01	2x interpolation
					10	4x interpolation
					11	8x interpolation
0062h 0262h 0462h	R/Wb	XY_PHINCO_LSB	7:0	XY_PHI_NCO[7:0]		NCO_PhaseOffset[7 to 0]

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0063h 0263h 0463h	R/Wb	XY_PHINCO_MSB	7:0	XY_PHI_NCO[15:8]		NCO_PhaseOffset[15 to 8]
0064h 0264h 0464h	R/Wb	XY_FREQNCO_B0	7:0	XY_FREQ_NCO[7:0]		used to specify NCO frequency
0065h 0265h 0465h	R/Wb	XY_FREQNCO_B1	7:0	XY_FREQ_NCO[15:8]		used to specify NCO frequency
0066h 0266h 0466h	R/Wb	XY_FREQNCO_B2	7:0	XY_FREQ_NCO[23:16]		used to specify NCO frequency
0067h 0267h 0467h	R/Wb	XY_FREQNCO_B3	7:0	XY_FREQ_NCO[31:24]		used to specify NCO frequency
0068h 0268h 0468h	R/Wb	XY_FREQNCO_B4	7:0	XY_FREQ_NCO[39:32]		used to specify NCO frequency
0069h 0269h 0469h	R/Wb	XY_PHASECORR_CNTRL0	7:0	XY_PHASE_CORR[7:0]		lsbsphase_correction_factor'
006Ah 026Ah 046Ah	R/Wb	XY_PHASECORR_CNTRL1	7	XY_PHASE_CORR_ENABLE	0	phase_correction disabled
					1	phase_correction enabled
			6:5	XY_PHASE_CORR_SWAP[1:0]	00	I(A)=I ; Q(B) =Q
					01	I(A)=Q ; Q(B) =I
					10	I(A)=I ; Q(B) =I
					11	I(A)=Q ; Q(B) =Q
			4:0	XY_PHASE_CORR[12:8]		msbsphase_correction_factor'
Digital Gain and Offset DAC XY						
006Bh 026Bh 046Bh	R/Wb	XY_DSP_X_GAIN_LSB	7:0	XY_DSP_X_GAIN[7:0]		digital gain control path X
006Ch 026Ch 046Ch	R/Wb	XY_DSP_X_GAIN_MSB	3:0	XY_DSP_X_GAIN[11:8]		digital gain control path X
006Dh 026Dh 046Dh	R/Wb	XY_DSP_Y_GAIN_LSB	7:0	XY_DSP_Y_GAIN[7:0]		digital gain control path Y
006Eh 026Eh 046Eh	R/Wb	XY_DSP_Y_GAIN_MSB	3:0	XY_DSP_Y_GAIN[11:8]		digital gain control path Y
006Fh 026Fh 046Fh	R/Wb	XY_DSP_OUT_CNTRL	3	XY_DSP_X_GAIN_EN	0	dsp_X_gain disabled
					1	dsp_X_gain enabled
			2	XY_DSP_Y_GAIN_EN	0	dsp_Y_gain disabled
					1	dsp_Y_gain enabled
			1	XY_MINUS_3DB_GAIN	0	unity gain
					1	3 dB gain
			0	XY_CLIP_LEV_EN	0	cliplev_control disabled
					1	cliplevcontrol enabled
0070h 0270h 0470h	R/Wb	XY_DSP_CLIPLEV	7:0	XY_CLIPLEV[7:0]		cliplevel = [0..255]

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0071h 0271h 0471h	R/Wb	XY_DSP_X_OFFSET_LSB	7:0	XY_DSP_X_OFFSET[7:0]		digital offset path X
0072h 0272h 0472h	R/Wb	XY_DSP_X_OFFSET_MSB	7:0	XY_DSP_X_OFFSET[15:8]		digital offset path X
0073h 0273h 0473h	R/Wb	XY_DSP_Y_OFFSET_LSB	7:0	XY_DSP_Y_OFFSET[7:0]		digital offset path X
0074h 0274h 0474h	R/Wb	XY_DSP_Y_OFFSET_MSB	7:0	XY_DSP_Y_OFFSET[15:8]		digital offset path X

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
				Data Format and IQ Levels DAC XY		
0075h 0275h 0475h	R/Wb	XY_IQ_LEV_CNTRL	7	XY_DATA_FORMAT	0	signed (twos complement) format'
					1	unsigned format
			6:5	NOT USED		
			3:2	XY_I_LEV_CNTR[1:0]		
					00	data coming from RX PHY is direclty used by DSP
					01	data coming from RX PHY is used by the DSP when the State Machine enters the sate DATA (after end of ILA)
			1:0	XY_Q_LEV_CNTRL[1:0]	1x	DSP is using fixed value specified in i_dc_level registers
					00	data coming from RX PHY is direclty used by DSP
					01	data coming from RX PHY is used by the DSP when the State Machine enters the sate DATA (after end of ILA)
					1x	DSP is using fixed value specified in q_dc_level registers
0076h 0276h 0476h	R/Wb	XY_I_DC_LEVEL_LSB	7:0	XY_I_DC_LEVEL[7:0]		lsbsi_dc_level'
0077h 0277h 0477h	R/Wb	XY_I_DC_LEVEL_MSB	7:0	XY_I_DC_LEVEL[15:8]		msbsi_dc_level'
0078h 0278h 0478h	R/Wb	XY_Q_DC_LEVEL_LSB	7:0	XY_Q_DC_LEVEL[7:0]		lsbsq_dc_level'
0079h 0279h 0479h	R/Wb	XY_Q_DC_LEVEL_MSB	7:0	XY_Q_DC_LEVEL[15:8]		msbsq_dc_level'
				Signal Power Detector		

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
007Ah 027Ah 047Ah	R/Wb	XY_SPD_CNTRL	7	XY_SPD_ENA	0	SignalPowerDetector disabled
					1	SignalPowerDetector enabled
			6:4	NOT USED		
			3:0	XY_SPD_WINLENGTH[3:0]		SPD averages 2^(winlength+6) IQpairs
					0000	average 64 IQpairs (2^6 samples)
					0001	average 128 IQpairs (2^7 samples)
					0010	average 256 IQpairs (2^8 samples)
					0011	average 512 IQpairs (2^9 samples)
					0100	average 1024 IQpairs (2^10 samples)
					0101	average 2048 IQpairs (2^11 samples)
					0110	average 4096 IQpairs (2^12 samples)
					0111	average 8192 IQpairs (2^13 samples)
					1000	average 16384 IQpairs (2^14 samples)
					1001	average 32768 IQpairs (2^15 samples)
					1010	average 65536 IQpairs (2^16 samples)
					1011	average 131072 IQpairs (2^17 samples)
					1100	average 262144 IQpairs (2^18 samples)
					1101	average 524288 IQpairs (2^19 samples)
					1110	average 1048576 IQpairs (2^20 samples)
					1111	average 2097152 IQpairs (2^21 samples)
007Bh 027Bh 047Bh	R/Wb	XY_SPD_THRESHOLD_LSB	7:0	XY_SPD_THRESHOLD[7:0]		spd_threshold lsbs'
007Ch 027Ch 047Ch	R/Wb	XY_SPD_THRESHOLD_MSB	7:0	XY_SPD_THRESHOLD[15:8]		spd_threshold msbs'
007Dh 027Dh 047Dh	R	XY_SPD_AVERAGE_LSB	7:0	XY_SPD_AVERAGE[7:0]		spd_average lsbs'
007Eh 027Eh 047Eh	R	XY_SPD_AVERAGE_MSB	7:0	XY_SPD_AVERAGE[15:8]		spd_average msbs'
MUTE controller DAC XY						

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0080h 0280h 0480h	R/W	XY_MUTE_CNTRL_0	7	XY_MUTE_ENABLE	0	disable mute feature
					1	enable mute feature
			6	XY_SW_MUTE_ENA	0	no action
					1	mutesignal (uses xy_direct_cfg)
			5	XY_MC_ALARM_CLR	0	no action
					1	clear mc_alarm flags
			4	XY_HOLD_DATA	0	disables holdfeature
					1	enables hold (i.c.o. conditional event)
			3	NOT USED		
			2	XY_CLIPDET_ENA	0	disable clipping detection
					1	enable clipping detection
			1:0	XY_CLIP_SEL[1:0]		only used if clip_det enabled
					00	no mute action
					01	mute on clip_det_a
					10	mute on clip_det_b
					11	mute on clip_det_a or clip_det_b
0081h 0281h 0481h	R/W	XY_MUTE_CNTRL_1	7:6	XY_INCIDENT_CFG[1:0]		incident mute style
			5:4	XY_DATA_CFG[1:0]		data mute style
			3:2	XY_ALARM_CFG[1:0]		alarm mute style
			1:0	XY_DIRECT_CFG[1:0]		direct mute style
0082h 0282h 0482h	R/W	XY_MUTE_CNTRL_2	7	XY_IGNORE_ALARM		ignore alarm trigger (for mute action, not for intr_mute)
			6	XY_IGNORE_RFTX_ENA		ignore state rftx_ena (link to xy_rf_tx_in)
			5	XY_IGNORE_MDS_BSY		ignore state mds_busy
			4	XY_IGNORE_DATA_V_IQ		ignore state internal data invalid
			3	NOT USED		
			2	XY_ENA_IQR_INCIDENT		enable IQ out-of-Range detector as incident
			1	XY_ENA_SPD_INCIDENT		enable SignalPowerDetect as incident
			0	XY_ENA_ERF_INCIDENT		enable ErrorReportFlag (from RX PHY) as incident
0083h 0283h 0483h	R/W	XY_MUTE_AL_ENA_0	7	XY_DATA_IQ_VALID_AL_ENA		data_iq_valid 1 -> 0
			6	XY_MDS_BSY_AL_ENA		mds_busy 0 -> 1
			5	XY_LVL_DET_OR_AL_ENA		clip_det_or 0 -> 1
			4	XY_ERR_RPT_FLAG_AL_ENA		err_rpt_flag 0 -> 1
			3	XY_TEMP_ALARM_AL_ENA		temp_alarm 0 -> 1
			2	XY_CA_ERR_AL_ENA		ca_error 0 -> 1
			1	XY_MON_DCLK_ERR_AL_ENA		mon_dclk_err 0 -> 1
			0	XY_CLK_MON_AL_ENA		clk_mon 0 -> 1
0084h 0284h 0484h	R/W	XY_MUTE_AL_ENA_1	7:2	NOT USED		
			1	XY_IQR_ERR_AL_ENA		iqr_err 0 -> 1
			0	XY_SPD_OVF_AL_ENA		spd_ovf 0 -> 1

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0085h 0285h 0485h	R/W	XY_MUTE_RATE_CNTRL_0	7:4	XY_ALARM_MRATE[3:0]		sets mute and demute rate in case of alarm event. it is recomneded to set all mute rates with the same value.
			3:0	XY_DIRECT_MRATE[3:0]		sets mute and demute rate in case of direct mute control. it is recomneded to set all mute rates with the same value
0086h 0286h 0486h	R/W	XY_MUTE_RATE_CNTRL_1	7:4	XY_INCIDENT_MRATE[3:0]		sets mute and demute rate in case of incident. it is recomneded to set all mute rates with the same value
			3:0	XY_DATA_MRATE[3:0]		sets mute and demute rate in case of data invalid state. it is recomneded to set all mute rates with the same value change
0087h 0287h 0487h	R/W	XY_MUTE_WAITPERIOD_LSB	7:0	XY_MUTE_WAITPERIOD[7:0]		mute wait period (lsb's)
0088h 0288h 0488h	R/W	XY_MUTE_WAITPERIOD_MSB	7:0	XY_MUTE_WAITPERIOD[15:8]		mute wait period (msb's)
0089h 0289h 0489h	R/Wb	XY_IQ_RANGE_LIMIT_LSB	7:0	XY_IQ_RANGE_LIMIT[7:0]		IQ Range Limit (lsb's)
008Ah 028Ah 048Ah	R/Wb	XY_IQ_RANGE_LIMIT_MSB	7:0	XY_IQ_RANGE_LIMIT[15:8]		IQ Range Limit (msb's)
Interrupt DAC XY						
008Ch 028Ch 048Ch	R/W	XY_INTR_CNTRL	3	XY_INTR_CLEAR	0	no action
					1	clears i_intr and intr_flags
			2:0	XY_INTR_MON_DCLK_RANGE[2:0]	000	mon_dclk_flag when mon_dclk drifts to (1 | 9)
					001	mon_dclk_flag when mon_dclk drifts to (2 | 8)
					010	mon_dclk_flag when mon_dclk drifts to (3 | 7)
					011	mon_dclk_flag when mon_dclk drifts to (4 | 6)
					100	mon_dclk_flag when mon_dclk drifts to (5)
					others	mon_dclk_flag disabled
008Dh 028Dh 048Dh	R/W	XY_INTR_ENA_0	7:0	XY_INTR_ENA[7:0]		enables usage of intr_src[7 to 0] for intr_flags[7 to 0]
008Eh 028Eh 048Eh	R/W	XY_INTR_ENA_1	7	NOT USED		
			6:5	XY_INTR_ENA[9:8]		enables usage of intr_src[9 to 8] for intr_flags[9 to 8]
008Fh 028Fh 048Fh	R	XY_INTR_FLAGS_0 (INTR_FLAG[7:0])	7	XY_INTR_DLP		indicates transition 0 -> 1 on intr_dlp
			6	XY_(NOT MDS_BUSY)		indicates transition 1 -> 0 on mds_busy
			5	XY_MDS_BUSY		indicates transition 0 -> 1 on mds_busy
			4	XY_TEMP_ALARM		indicates transition 0 -> 1 on temp_alarm
			3	XY_CLIP_DET_OR		indicates transition 0 -> 1 on clip_detect(a or b)
			2	XY_CA_ERROR		indicates transition 0 -> 1 on clock_align_monitor
			1	XY_CLK_MON		indicates transition 0 -> 1 on clkmon(div8)
			0	XY_MON_DCLK_ERR		indicates transition 0 -> 1 on mon_dclk_error_flags
0090h 0290h 0490h	R	XY_INTR_FLAGS_1 (INTR_FLAG[14:8])	7	NOT USED		
			6	XY_ERR_RPT_FLAG		indicates transition 0 -> 1 on err_rpt_flag
			5	XY_MC_ALARM		indicates alarm event detected by mute_cntrl
			4:0	NOT USED		
Digital Signal Processin Strobe controls						

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0099h 0299h 0499h	R/W	XY_DSP_SAMPLE_CNRL	4	XY_DSP_READ_SEL	0	dsp_read[31:0] <= mc_status[31:0]
					1	dsp_read[31:0] <= dsp_sample[31:0]
			3	XY_DSP_STROBE	0	no action
					1	update dsp_sample
			2:0	XY_DSP_SMPL_SEL[2:0]	000	dsp_sample <= q_0 & i_0
					001	dsp_sample <= q_1 & i_1
					010	dsp_sample <= q_2 & i_2
					011	dsp_sample <= q_3 & i_3
					100	dsp_sample <= q_tst & i_tst
					101	dsp_sample <= x_tst
					110	dsp_sample <= mc_tst
009Ah 029Ah 049Ah	R	XY_DSP_READ_LSB	7:0	XY_DSP_READ[7:0]		
009Bh 029Bh 049Bh	R	XY_DSP_READ_LSIB	7:0	XY_DSP_READ[15:8]		
009Ch 029Ch 049Ch	R	XY_DSP_READ_MSIB	7:0	XY_DSP_READ[23:16]		
009Dh 029Dh 049Dh	R	XY_DSP_READ_MSB	7:0	XY_DSP_READ[31:24]		

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
				Multiple Device Synchronization controls DAC XY		
00A0h 02A0h 04A0h	R/W	XY_MDS_MAIN	7:6	XY_MDS_EQCHECK[1:0]	00	(early=1 & late=1)
					01	late
					10	early
					11	(start early and late) or (start late and early)
			5	XY_MDS_MAN	0	auto control adjustment delays
					1	manual control adjustment delays
			4	XY_MDS_SREF_DIS	1	disable sref_generation
					0	enable sref_generation
			3	XY_MDS_EAST_WEST	0	SYSREF_WEST used as input
					1	SYSREF_EAST used as input
			2:1	XY_MDS_MODE[1:0]	00	Alternate mode
					01	not used
					10	JESD204B suclass1 mode
					11	not used
			0	XY_MDS_ENA	0	disable mds function
					1	enable mds function
00A1h 02A1h 04A1h	R/W	XY_MDS_VS1_CNTRL	7:6	XY_DLP_ISSUE_COND[1:0]	00	dlp_issue <= (not dlp_lock) or (not dlp_sync)
					01	dlp_issue <= (not dlp_lock) and (not dlp_sync)
					10	dlp_issue <= (not dlp_lock)
					11	dlp_issue <= (not dlp_sync)
			5	XY_IGNORE_ENA_CORR	0	compensate for DLP/CDI latency uncertainty
					1	no correction for DLP/CDI latency uncertainty
			4	NOT USED	0	
			3:2	XY_I_REINIT_MODE[1:0]	00	assert sync request
					01	assert sync request and reset DLP
					10	assert sync request and reset mds controller
					11	no action (ignore dlp_issue)
			1	XY_MDS_COPY	0	normal operation
					1	local MDS_cntrl copies settings neighbor MDS_cntrl
			0	XY_MDS_CAPTURE_ENA	0	local MDS_cntrl uses captured reference of it's neighbor.
					1	local MDS_cntrl captures sysref as reference

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00A2h 02A2h 04A2h	R/W	XY_MDS_IO_CNTRL	7	XY_MDS_MAN_SEL_FE_E	0	mds_sel_fe_E set by mds-cntrl
					1	mds_sel_fe_E set by mds_io_cntrl(3)
			6	XY_MDS_MAN_SEL_FE_W	0	mds_sel_fe_W set by mds-cntrl
					1	mds_sel_fe_W set by mds_io_cntrl(1)
			5	XY_MDS_IO_PON_E	0	mds_io_E disabled (power down)
					1	mds_io_E enabled (only when mds_ena = ‘1)
			4	XY_MDS_IO_PON_W	0	mds_io_W disabled (power down)
					1	mds_io_W enabled (only when mds_ena = ‘1)
			3	XY_MDS_SEL_FE_E	0	mds_io_E operates at falling edge i_dacclk
					1	mds_io_E operates at rising edge i_dacclk
			2	NOT USED		not used
			1	XY_MDS_SEL_FE_W	0	mds_io_W operates at falling edge i_dacclk
					1	mds_io_W operates at rising edge i_dacclk
			0	NOT USED		not used
00A3h 02A3h 04A3h	R/W	XY_MDS_MISCCNTRL0	7	XY_MDS_RUN	0	no action
					1	(0 ? 1) transition restarts evaluation_counter
			6	XY_MDS_NCO	0	no action
					1	nco synchronization enabled
			5	XY_MDS_NCO_PULSE	0	no action
					1	manual control w.r.t. NCO tuning
			4	XY_MDS_EVAL_ENA	0	mds_evaluation disabled
					1	mds_evaluation enabled
			3	XY_MDS_PRERUN_ENA	0	no mds_win/mds_ref generation in advance
					1	mds_win/mds_ref runin before mds_evaluation
			2:0	XY_MDS_PULSEWIDTH[2:0]		width of mds_a (in wclk = dacclkperiods)
					000	1T
					001	2T
					010	111: (mds_pulsewidth 1) 4T
00A4h 02A4h 04A4h	R/W	XY_MDS_MAN_ADJUSTDLY	7:0	XY_MDS_MAN_ADJUSTDLY[7:0]	mds_man = 0	initial value adjustment delay
					mds_man = 1	controls adjustment delay
00A5h 02A5h 04A5h	R/W	XY_MDS_AUTO_CYCLES	7:0	XY_MDS_AUTO_CYCLES[7:0]		number of evaluation cycles applied for MDS

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00A6h 02A6h 04A6h	R/W	XY_MDS_MISCCNTRL1	7	XY_MDS_SR_CKEN	0	freerunning mds_cken
					1	mds_cken forced low
			6	XY_MDS_SR_LOCKOUT	0	mds_lockout in use
					1	mds_lockout forced low
			5	XY_MDS_SR_LOCK	0	mds_lock in use
					1	mds_lock forced low
			4	XY_MDS_RELOCK	0	no action
					1	relock when lockout occurs
			3:0	XY_MDS_LOCK_DELAY		number of succeeding equal'detectionsuntillock'
				Multiple Device Synchronization Status DAC XY		
00A7h 02A7h 04A7h	R/W	XY_MDS_OFFSET_DLY	7:0	XY_MDS_OFFSET_DLY[7:0]		delay_offset for data flow (two's complement[-128..127])'
00A8h 02A8h 04A8h	R/W	XY_MDS_WIN_LOW	7:0	XY_MDS_WIN_PERIOD_A[7:0]		determines mds_window lowtime
00A9h 02A9h 04A9h	R/W	XY_MDS_WIN_HIGH	7:0	XY_MDS_WIN_PERIOD_B[7:0]		determines mds_window hightime
00AAh 02AAh 04AAh	R/W	XY_LMFC_PERIOD	7:0	XY_LMFC_PERIOD[7:0]		determines lmfc_period
00ABh 02ABh 04ABh	R/W	XY_LMFC_PRESET	7:0	XY_LMFC_PRESET[7:0]		determines position lmfc w.r.t. i_mds_ref
00ACh 02ACh 04ACh	R/W	XY_MDS_CNT_PRESET	7:0	XY_MDS_CNT_PRESET[7:0]		determines position i_mds_ref w.r.t. sysref_C only used in manual mode
00ADh 02ADh 04ADh	R/W	XY_SYNC_LMFC_PE	7:0	XY_SYNC_LMFC_PE[7:0]		determines position pos_edge SYNCB w.r.t. lmfc
00AEh 02AEh 04AEh	R/W	XY_MDS_SYNC_CNTRL	4	XY_MDS_SYNC_INIT	0	initial state SYNCB = 0"
					1	initial state SYNCB= 1"
			3	XY_MDS_AUTO_SYNC_PE	0	SYNCB pos edge depends on sync_lmfc_pe
					1	SYNCB pos edge internally calculated
			2:0	XY_SYNC_FINE_DLY[2:0]		fine tuning position SYNCB (sync_rq(dacclkaccuracy))
00AFh 02AFh 04AFh	R/W	XY_MDS_WIN_DLY	6	XY_MDS_AUTO_PRESET	0	i_mds_ref depends on mds_cnt_preset
					1	i_mds_ref internally calculated
			5	XY_MDS_AUTO_WIN_DLY	0	internal mds_win delay depends on mds_win_dly
					1	internal mds_win delay internally calculated
			4:0	XY_MDS_WIN_DLY[4:0]		mds_w_dly = 6T + mds_win_dly
00B2h 02B2h 04B2h	R	XY_MDS_SEARCH_CYCLE	7:0	XY_MDS_SEARCH_CYCLE[7:0]		number of cycles used to verify presence of sysref
00B5h 02B5h 04B5h	R	XY_MDS_ADJDELAY	7:0	XY_MDS_ADJDELAY[7:0]		actual value adjustment delay

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00B6h 02B6h 04B6h	R	XY_MDS_STATUS0	7	XY_ERR_RPT_FLAG		error_rpt_flag_state
			6:5	NOT USED		
			4	XY_ADD_ERROR		delay_offset can't be applied in available range
			3	XY_EARLY_ERROR		adjustment delay maximum value stops the search
			2	XY_LATE_ERROR		adjustment delay minimum value stops the search
			1	NOT USED		
			0	XY_MDS_ACTIVE		eval_logic active
00B7h 02B7h 04B7h	R	XY_MDS_STATUS1	7	XY_I_BUSY		indicates that i_state-controller is busy
			6	XY_I_STATE_ERR		indicates that i_state-controller is at illegal state
			5	XY_I_LOCK_DET		internal used by i_state-controller
			4	XY_I_DLP_LOCK		internal used by i_state-controller
			3:0	XY_I_STATE[3:0]		actual state i-state-controller
00B8h 02B8h 04B8h	R	XY_MDS_STATUS2	7	XY_MDS_LOCK		mds search /eval has found the sysref-edge
			6:4	RESERVED		reserved
			3	XY_EQUAL_CHECK		equal_check has been started (reads as '0')
			2:0	RESERVED		reserved
00BBh 02BBh 04BBh	R	XY_MDS_STATUS5	7:0	XY_DELAY_CNT[7:0]		mds correction #1 (sysref capture)
00BCh 02BCh 04BCh	R	XY_MDS_STATUS6	7:0	XY_I_ENA_SAMPLE[7:0]		mds correction #2 (dlp- dsp alignment)
00BDh 02BDh 04BDh	R	XY_MDS_STATUS7	7:6	NOT USED		
			5	XY_MDS_PRERUN		mds-prerun phase active flag (only for mds_vs0)
			4	XY_MDS_LOCKOUT		mds lockout detected flag (only for mds_vs0)
			3:2	NOT USED		
			1:0	XY_ENA_PHASE	00	enable_phase=0
					01	enable_phase=1 (only possible for ^2)
					10	enable_phase=2 (only possible for ^2 or ^4)
					11	enable_phase=3 (only possible for ^2)

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
Digital Lane Processing (DLP) DAC XY						
Lanes Swapping, Polarity control, SYNC control, SCRambler control						
00C7h 02C7h 04C7h	R/W	XY_ILA_CNTRL	7	XY_COMBINE_ILA_CNTRL	0	independent ILA cntrl (local)
					1	ILA control depends on neighbouring ILA cntrl
			6:5	XY_SEL_ILA[1:0]	00	ila is done after receiving 1 /A/symbol
					01	ila is done after receiving 2 /A/symbols
					10	ila is done after receiving 3 /A/symbols
					11	ila is done after receiving 4 /A/symbols (recommended)
			4:2	XY_SEL_LOCK[2:0]		usage depends on L_value
			1	XY_SUP_LANE_SYN	0	inter lane alignment synchronization disabled
					1	inter lane alignment synchronization enabled
			0	XY_EN_SCR	0	data descrambling disabled
					1	data descrambling enabled
00C8h 02C8h 04C8h	R/W	XY_ALIGN_CNTRL	7	XY_FORCE_1ST_SMPL_LOW	0	no action
					1	data_enable is kept low for the first sample
			6	XY_USE_/Q/		0: ignore /Q/ for cfg_data_extraction
						1: use /Q/ for cfg_data_extraction
			5:4	NOT USED		
			3	XY_SUB_CLASS0		0: ila_sequence_length = 4 mfr (subclass 1,2)
						0: ila_sequence_length> = 4 mfr (subclass 1,2)
			2	XY_FRAME_ALIGN_ENA	0	no action
					1	enable framealignment
			1	XY_DYN_ALIGN_ENA	0	no dynamic realignment
					1	dynamic realignment (and monitoring) enabled
			0	XY_FORCE_ALIGN	0	automatic lane alignment based on /A/symbols
					1	manual lane alignment based on man_align_lnx

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00CBh 02CBh 04CBh	R/W	XY_ERR_HANDLING_0	7	XY_EN_KOUT_UNEXP_LN3	0	sample assembly ignores kout_unexp_ln3 flags
					1	sample assembly uses kout_unexp_ln3 flags
			6	XY_EN_KOUT_UNEXP_LN2	0	sample assembly ignores kout_unexp_ln2 flags
					1	sample assembly uses kout_unexp_ln2 flags
			5	XY_EN_KOUT_UNEXP_LN1	0	sample assembly ignores kout_unexp_ln1 flags
					1	sample assembly uses kout_unexp_ln1 flags
			4	XY_EN_KOUT_UNEXP_LN0	0	sample assembly ignores kout_unexp_ln0 flags
					1	sample assembly uses kout_unexp_ln0 flags
			3	XY_EN_NIT_ERR_LN3	0	sample assembly ignores nit_err_ln3 flags
					1	sample assembly uses nit_err_ln3 flags
			2	XY_EN_NIT_ERR_LN2	0	sample assembly ignores nit_err_ln2 flags
					1	sample assembly uses nit_err_ln2 flags
			1	XY_EN_NIT_ERR_LN1	0	sample assembly ignores nit_err_ln1 flags
					1	sample assembly uses nit_err_ln1 flags
			0	XY_EN_NIT_ERR_LN0	0	sample assembly ignores nit_err_ln0 flags
					1	sample assembly uses nit_err_ln0 flags
00CCh 02CCh 04CCh	R/W	XY_SYNCOUT_MODE	7:5	XY_SEL_RE_INIT[2:0]	000	i_re_init when 1 of the enabled lane_rst's is active'
					001	i_re_init when all enabled lane_rst's are active'
					010	i_re_init when rst_ln0 is active
					011	i_re_init when rst_ln1 is active
					100	i_re_init when rst_ln2 is active
					101	i_re_init when rst_ln3 is active
					110	i_re_init remains 1''
					111	i_re_init remains 0''
			4	XY_COMBINE_SYNC_CNTRL	0	sync_out depends only on local lanes
					1	sync_out depends also on neighbouring DLP
			3	XY_SYNC_INIT_LEVEL	0	sync starts with 0''
					1	sync starts with 1''
			2:0	XY_SEL_SYNC[2:0]	000	sync when 1 of the enabled lane_syncsisactive'
					001	sync when all enabled lane_syncsareactive'
					010	sync when sync_ln0 is active
					011	sync when sync_ln1 is active
					100	sync when sync_ln2 is active
					101	sync when sync_ln3 is active
					110	sync remains fixed 1''
					111	sync remains fixed 0''

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00CDh 02CDh 04CDh	R/W	XY_LANE_POLARITY	4	XY_SYNC_POL	0	sync_out is active when low
					1	sync_out is active when high
			3	XY_POL_P_LN3	0	no action
					1	invert all databits of physical lane ln3[9:0]
			2	XY_POL_P_LN2	0	no action
					1	invert all databits of physical lane ln2[9:0]
			1	XY_POL_P_LN1	0	no action
					1	invert all databits of physical lane ln1[9:0]
			0	XY_POL_P_LN0	0	no action
					1	invert all databits of physical laneln0[9:0]
00CEh 02CEh 04CEh	R/W	XY_LANE_SELECT	7:6	XY_LANE_SEL_L_LN#3[1:0]	00	Logical lane#3 = Physical lane 0
					01	Logical lane#3 = Physical lane 1
					10	Logical lane#3 = Physical lane 2
					11	Logical lane#3 = Physical lane 3
			5:4	XY_LANE_SEL_L_LN#2[1:0]	00	Logical lane#2 = Physical lane 0
					01	Logical lane#2 = Physical lane 1
					10	Logical lane#2 = Physical lane 2
					11	Logical lane#2 = Physical lane 3
			3:2	XY_LANE_SEL_L_LN#1[1:0]	00	Logical lane#1 = Physical lane 0
					01	Logical lane#1 = Physical lane 1
					10	Logical lane#1 = Physical lane 2
					11	Logical lane#1 = Physical lane 3
			1:0	XY_LANE_SEL_L_LN#0[1:0]	00	Logical lane#0 = Physical lane 0
					01	Logical lane#0 = Physical lane 1
					10	Logical lane#0 = Physical lane 2
					11	Logical lane#0 = Physical lane 3
Scramblers initialization values DAC XY						
00D0h 02D0h 04D0h	R/W	XY_SOFT_RESET_SCRAMBLER	7:6	XY_NOT USED	0	no action
			5	XY_SR_NO_F20_ACT_FLAG	0	no action
					1	soft reset no_f20_activity_flag
			4	XY_SR_ILA	0	no action
					1	soft reset inter-lane-alignment
			3	XY_SR_SCR_LN3	0	no action
					1	soft reset scrambler of lane0
			2	XY_SR_SCR_LN2	0	no action
					1	soft reset scrambler of lane1
			1	XY_SR_SCR_LN1	0	no action
					1	soft_reset scrambler of lane2
			0	XY_SR_SCR_LN0	0	no action
					1	soft_reset scrambler of lane3

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00D1h 02D1h 04D1h	R/W	XY_INIT_SCR_S15T8_LN0	7:0	XY_INIT_DESCR_P_LN00[15:8]		init value for ln0 descramblerbits s15 to s8
00D2h 02D2h 04D2h	R/W	XY_INIT_SCR_S7T1_LN0	6:0	XY_INIT_DESCR_P_LN00[7:1]		init value for ln0 descramblerbits s7 to s1
00D3h 02D3h 04D3h	R/W	XY_INIT_SCR_S15T8_LN1	7:0	XY_INIT_DESCR_P_LN01[15:8]		init value for ln1 descramblerbits s15 to s8
00D4h 02D4h 04D4h	R/W	XY_INIT_SCR_S7T1_LN1	6:0	XY_INIT_DESCR_P_LN01[7:1]		init value for ln1 descramblerbits s7 to s1
00D5h 02D5h 04D5h	R/W	XY_INIT_SCR_S15T8_LN2	7:0	XY_INIT_DESCR_P_LN02[15:8]		init value for ln2 descramblerbits s15 to s8
00D6h 02D6h 04D6h	R/W	XY_INIT_SCR_S7T1_LN2	6:0	XY_INIT_DESCR_P_LN02[7:1]		init value for ln2 descramblerbits s7 to s1
00D7h 02D7h 04D7h	R/W	XY_INIT_SCR_S15T8_LN3	7:0	XY_INIT_DESCR_P_LN03[15:8]		init value for ln3 descramblerbits s15 to s8
00D8h 02D8h 04D8h	R/W	XY_INIT_SCR_S7T1_LN3	6:0	XY_INIT_DESCR_P_LN03[7:1]		init value for ln3 descramblerbits s7 to s1
Initial Lane Alignment initialization, Error handling, DLP strobe, LMF configuration						
00D9h 02D9h 04D9h	R/W	XY_INIT_ILA_BUFPTR_L_LN01	7:4	XY_INIT_ILA_BUFPTR_L_LN#1[3:0]		init value for ila bufptr ln#1
			3:0	XY_INIT_ILA_BUFPTR_L_LN#0[3:0]		init value for ila bufptr ln#0
00DAh 02DAh 04DAh	R/W	XY_INIT_ILA_BUFPTR_L_LN23	7:4	XY_INIT_ILA_BUFPTR_L_LN#3[3:0]		init value for ila bufptr ln#3
			3:0	XY_INIT_ILA_BUFPTR_L_LN#2[3:0]		init value for ila bufptr ln#2
00DBh 02DBh 04DBh	R/W	XY_ERR_HANDLING_1	7	XY_EN_DISP_ERR_P_LN3	0	sample assembly ignores disp_err_ln3 flags
					1	sample assembly uses disp_err_ln3 flags
			6	XY_EN_DISP_ERR_P_LN2	0	sample assembly ignores disp_err_ln2 flags
					1	sample assembly uses disp_err_ln2 flags
			5	XY_EN_DISP_ERR_P_LN1	0	sample assembly ignores disp_err_ln1 flags
					1	sample assembly uses disp_err_ln1 flags
			4	XY_EN_DISP_ERR_P_LN0	0	sample assembly ignores disp_err_ln0 flags
					1	sample assembly uses disp_err_ln0 flags
			3	XY_CONCEAL_MODE	0	conceal by repeating one sample
					1	conceal by repeating two samples
			2	XY_SEL_CS_LIMIT	0	use <4,3,4> wclksaslimitforcs_kivcounters'
					1	use <2,2,2> wclksaslimitforcs_kivcounters'
			1:0	XY_IGNORE_ERR[1:0]	00	take disparity & nit-errors into account
					01	ignore niterrors at lane controller
					10	ignore disparity errors at lane controller
					11	ignore disparity & nit errors at lane controller

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00DCh 02DCh 04DCh	R/W	XY_REINIT_CNTRL	7	XY_REINIT_ILA_L_LN#3	0	no action
					1	logical lane#3 ila buffer out of range_error will activate re-init
			6	XY_REINIT_ILA_L_LN#2	0	no action
					1	logical lane#2 ila buffer out of range error will activate re-init
			5	XY_REINIT_ILA_L_LN#1	0	no action
					1	logical lane#1 ila buffer out of range error will activate re-init
			4	XY_REINIT_ILA_L_LN#0	0	no action
					1	logical lane#0 ila buffer out of range error will activate re-init
			3	XY_RESYNC_OLINK_P_LN3	0	no action
					1	ln3 lane controller checks for k28.5 /K/symbols
			2	XY_RESYNC_OLINK_P_LN2	0	no action
					1	ln2 lane controller checks for k28.5 /K/symbols
			1	XY_RESYNC_OLINK_P_LN1	0	no action
					1	ln1 lane controller checks for k28.5 /K/symbols
			0	XY_RESYNC_OLINK_P_LN0	0	no action
					1	ln0 lane controller checks for k28.5 /K/symbols
00DDh 02DDh 04DDh	R/W	XY_MISC_CNTRL	7	XY_DLPSTROBE	0	no action
					1	update dlp sample
			6:0	NOT USED		
00DEh 02DEh 04DEh	R/W	XY_LMF_CNTRL	7:5	XY_L[2:0]		(L) Number of lanes [1,2 or 4]
			4:3	XY_M[1:0]		(M) Number of converters [2]
			2:0	XY_F[2:0]		(F) Number of octets per frame [1,2 or 4]
Digital Lane Processing monitoring DAC XY						
00E0h 02E0h 04E0h	R	XY_ILA_MON_1_0	7:4	XY_ILA_MON_L_LN#1[3:0]		ILA alignement buffer pointer for logical lane#1
			3:0	XY_ILA_MON_L_LN#0[3:0]		ILA alignement buffer pointer for logical lane#0
00E1h 02E1h 04E1h	R	XY_ILA_MON_3_2	7:4	XY_ILA_MON_L_LN#3[3:0]		ILA alignement buffer pointer for logical lane#3
			3:0	XY_ILA_MON_L_LN#2[3:0]		ILA alignement buffer pointer for logical lane#2
00E2h 02E2h 04E2h	R	XY_ILA_BUF_ERR	3	XY_ILA_BUF_ERR_L_LN#3		ILA alignement buffer pointer out of range for logical lane#3
			2	XY_ILA_BUF_ERR_L_LN#2		ILA alignement buffer pointer out of range for logical lane#2
			1	XY_ILA_BUF_ERR_L_LN#1		ILA alignement buffer pointer out of range for logical lane#1
			0	XY_ILA_BUF_ERR_L_LN#0		ILA alignement buffer pointer out of range for logical lane#0
8b10b decoder flags						

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00E4h 02E4h 04E4h	R	XY_DEC_FLAGS	7	XY_DEC_NIT_ERR_P_LN3		NotInTable error flag lane_3
			6	XY_DEC_NIT_ERR_P_LN2		NotInTable error flag lane_2
			5	XY_DEC_NIT_ERR_P_LN1		NotInTable error flag lane_1
			4	XY_DEC_NIT_ERR_P_LN0		NotInTable error flag lane_0
			3	XY_DEC_DISP_ERR_P_LN3		Disparity error flag lane_3
			2	XY_DEC_DISP_ERR_P_LN2		Disparity error flag lane_2
			1	XY_DEC_DISP_ERR_P_LN1		Disparity error flag lane_1
			0	XY_DEC_DISP_ERR_P_LN0		Disparity error flag lane_0
00E5h 02E5h 04E5h	R	XY_KOUT_FLAG	3	XY_DEC_KOUT_P_LN3		/K/symbols found in lane_3
			2	XY_DEC_KOUT_P_LN2		/K/symbols found in lane_2
			1	XY_DEC_KOUT_P_LN1		/K/symbols found in lane_1
			0	XY_DEC_KOUT_P_LN0		/K/symbols found in lane_0
00E6h 02E6h 04E6h	R	XY_K28_LN0_FLAG	7	XY_P_LN0_ILA_MFR_ERR		irregular mfr-length during ila in lane_0
			6	XY_P_LN0_ILA_QT4_ERR		ila sequence with more than 4 mfr in lane_0 (subc 1,2)
			5	XY_P_LN0_ILA_LT4_ERR		ila sequene shorter than 4 mfr in _lane_0
			4	XY_K28_7_P_LN0		k28_7 /F/ symbols found in lane_0
			3	XY_K28_5_P_LN0		k28_5 /K/ symbols found in lane_0
			2	XY_K28_4_P_LN0		k28_4 /Q/ symbols found in lane_0
			1	XY_K28_3_P_LN0		k28_3 /A/ symbols found in lane_0
			0	XY_K28_0_P_LN0		k28_0 /R/ symbols found in lane_0
00E7h 02E7h 04E7h	R	XY_K28_LN1_FLAG	7	XY_P_LN1_ILA_MFR_ERR		irregular mfr-length during ila in lane_1
			6	XY_P_LN1_ILA_QT4_ERR		ila sequence with more than 4 mfr in lane_1 (subc 1,2)
			5	XY_P_LN1_ILA_LT4_ERR		ila sequene shorter than 4 mfr in _lane_1
			4	XY_K28_7_P_LN1		k28_7 /F/ symbols found in lane_1
			3	XY_K28_5_P_LN1		k28_5 /K/ symbols found in lane_1
			2	XY_K28_4_P_LN1		k28_4 /Q/ symbols found in lane_1
			1	XY_K28_3_P_LN1		k28_3 /A/ symbols found in lane_1
			0	XY_K28_0_P_LN1		k28_0 /R/ symbols found in lane_1
00E8h 02E8h 04E8h	R	XY_K28_LN2_FLAG	7	XY_P_LN2_ILA_MFR_ERR		irregular mfr-length during ila in lane_2
			6	XY_P_LN2_ILA_QT4_ERR		ila sequence with more than 4 mfr in lane_2 (subc 1,2)
			5	XY_P_LN2_ILA_LT4_ERR		ila sequene shorter than 4 mfr in _lane_2
			4	XY_K28_7_P_LN2		k28_7 /F/ symbols found in lane_2
			3	XY_K28_5_P_LN2		k28_5 /K/ symbols found in lane_2
			2	XY_K28_4_P_LN2		k28_4 /Q/ symbols found in lane_2
			1	XY_K28_3_P_LN2		k28_3 /A/ symbols found in lane_2
			0	XY_K28_0_P_LN2		k28_0 /R/ symbols found in lane_2

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00E9h 02E9h 04E9h	R	XY_K28_LN3_FLAG	7	XY_P_LN3_ILA_MFR_ERR		irregular mfr-length during ila in lane_3
			6	XY_P_LN3_ILA_QT4_ERR		ila sequence with more than 4 mfr in lane_3 (subc 1,2)
			5	XY_P_LN3_ILA_LT4_ERR		ila sequene shorter than 4 mfr in _lane_3
			4	XY_K28_7_P_LN3		k28_7 /F/ symbols found in lane_3
			3	XY_K28_5_P_LN3		k28_5 /K/ symbols found in lane_3
			2	XY_K28_4_P_LN3		k28_4 /Q/ symbols found in lane_3
			1	XY_K28_3_P_LN3		k28_3 /A/ symbols found in lane_3
			0	XY_K28_0_P_LN3		k28_0 /R/ symbols found in lane_3
00EAh 02EAh 04EAh	R	XY_KOUT_UNEXPECTED_FLAG	3	XY_DEC_KOUT_UNEXP_LN3		Unexpected /K/symbols found in lane_3
			2	XY_DEC_KOUT_UNEXP_LN2		Unexpected /K/symbols found in lane_2
			1	XY_DEC_KOUT_UNEXP_LN1		Unexpected /K/symbols found in lane_1
			0	XY_DEC_KOUT_UNEXP_LN0		Unexpected /K/symbols found in lane_0
RX-PHY lock and Code Group Synchronization State Machine monitoring						
00EBh 02EBh 04EBh	R	XY_LOCK_CNT_MON_P_LN01	7:4	XY_LOCK_CNT_MON_P_LN1[3:0]		lock_state monitor sync word alignment physical lane1
			3:0	XY_LOCK_CNT_MON_P_LN0[3:0]		lock_state monitor sync word alignment physical lane0
00ECh 02ECh 04ECh	R	XY_LOCK_CNT_MON_P_LN23	7:4	XY_LOCK_CNT_MON_P_LN3[3:0]		lock_state monitor sync word alignment physical lane3
			3:0	XY_LOCK_CNT_MON_P_LN2[3:0]		lock_state monitor sync word alignment physical lane2
00EDh 02EDh 04EDh	R	XY_CS_STATE_P_LNX	7:6	XY_CS_STATE_P_LN3[1:0]		monitor cs_state physical lane3
			5:4	XY_CS_STATE_P_LN2[1:0]		monitor cs_state physical lane2
			3:2	XY_CS_STATE_P_LN1[1:0]		monitor cs_state physical lane1
			1:0	XY_CS_STATE_P_LN0[1:0]		monitor cs_state physical lane0
Flags counters and DLP interrupt controls						
00EEh 02EEh 04EEh	R/W	XY_MISC_FLAG_CNTRL	7	XY_RST_BUF_ERR_FLAGS		reset ila buf out of range_flags
			6	XY_AUTO_RST_FLAGCNTS		flagcnts are also reset when DLP is resetted
			5	XY_FLAGCNT_HOLD_MODE	0	flagcnt<i> holds when flagcnt<i>= flagcnt<i>_max
					1	flagcnt<i> holds when flagcnt<x>=flagcnt<x>_max
			4:0	NOT USED		
00EFh 02EFh 04EFh	R/W	XY_INTR_MISC_ENA	7	XY_INTR_ENA_CS_INIT_P_LN3		intr_misc in case cs_state_ln3 = cs_init
			6	XY_INTR_ENA_CS_INIT_P_LN2		intr_misc in case cs_state_ln2 = cs_init
			5	XY_INTR_ENA_CS_INIT_P_LN1		intr_misc in case cs_state_ln1 = cs_init
			4	XY_INTR_ENA_CS_INIT_P_LN0		intr_misc in case cs_state_ln0 = cs_init
			3	XY_INTR_ENA_BUF_ERR_LN3		intr_misc in case ila_bufcnt_ln3 out of range
			2	XY_INTR_ENA_BUF_ERR_LN2		intr_misc in case ila_bufcnt_ln2 out of range
			1	XY_INTR_ENA_BUF_ERR_LN1		intr_misc in case ila_bufcnt_ln1 out of range
			0	XY_INTR_ENA_BUF_ERR_LN0		intr_misc in case ila_bufcnt_ln0 out of range
00F0h 02F0h 04F0h	R	XY_FLAG_CNT_LSB_LN0	7:0	XY_FLAG_CNT_LN0[7:0]		lsb's of flag_counterln0'
00F1h 02F1h 04F1h	R	XY_FLAG_CNT_MSB_LN0	7:0	XY_FLAG_CNT_LN0[15:8]		msb's of flag_counterln0'

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00F2h 02F2h 04F2h	R	XY_FLAG_CNT_LSB_LN1	7:0	XY_FLAG_CNT_LN1[7:0]		lsb's of flag_counterln1'
00F3h 02F3h 04F3h	R	XY_FLAG_CNT_MSB_LN1	7:0	XY_FLAG_CNT_LN1[15:8]		msb's of flag_counterln1'
00F4h 02F4h 04F4h	R	XY_FLAG_CNT_LSB_LN2	7:0	XY_FLAG_CNT_LN2[7:0]		lsb's of flag_counterln2'
00F5h 02F5h 04F5h	R	XY_FLAG_CNT_MSB_LN2	7:0	XY_FLAG_CNT_LN2[15:8]		msb's of flag_counterln2'
00F6h 02F6h 04F6h	R	XY_FLAG_CNT_LSB_LN3	7:0	XY_FLAG_CNT_LN3[7:0]		lsb's of flag_counterln3'
00F7h 02F7h 04F7h	R	XY_FLAG_CNT_MSB_LN3	7:0	XY_FLAG_CNT_LN3[15:8]		msb's of flag_counterln3'
00F8h 02F8h 04F8h	R/W	XY_ERR_MIX_CNTRL	7	XY_EM	0	k28_0_ln<i> available for selection
					1	err_mix_ln<i> available for selection
					0	no action
					1	kout_unexp_ln<i> used for err_mix_ln<i>
					0	no action
					1	disp_err_ln<i> used for err_mix_ln<i>
					0	no action
					1	nit_err_ln<i> used for err_mix_ln<i>
					0	no action
					1	ila_buf_err_ln<i> used for err_rpt_flag generation
					0	no action
					1	kout_unexp_ln<i> used for err_rpt_flag generation
					0	no action
					1	disp_err_ln<i> used for err_rpt_flag generation
					0	no action
					1	nit_err_ln<i> used for err_rpt_flag generation
00F9h 02F9h 04F9h	R/W	XY_INTR_ENA0	7:4	NOT USED		
			3	XY_INTR_STLTP_ERR	0	no action
					1	stltp_err_flag affects i_ln<x>
			2	XY_INTR_BER_LN<I>	0	no action
					1	ber_ln<x> affects i_ln<x>
			1	XY_INTR_ILA_RCV	0	no action
					1	ila_rcv_flag affects i_ln<x>
			0	XY_INTR_NO_ACT_F20	0	no action
					1	no_active_f20_ln<x> affects i_ln<x>

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00FAh 02FAh 04FAh	R/W	XY_INTR_ENA1	7	XY_INTR_ENA_NIT	0	no action
					1	nit error in In<x> affects i_In<x>
			6	XY_INTR_ENA_DISP	0	no action
					1	disparity error in In<x> affects i_In<x>
			5	XY_INTR_ENA_KOUT	0	no action
					1	detection k control character in In<x> affects i_In<x>
			4	XY_INTR_ENA_KOUT_UNEXP	0	no action
					1	detection unexpected k character in In<x> affects i_In<x>
			3	XY_INTR_ENA_K28_7	0	no action
					1	detection k28_7 in In<x> affects i_In<x>
			2	XY_INTR_ENA_K28_5	0	no action
					1	detection k28_5 in In<x> affects i_In<x>
			1	XY_INTR_ENA_K28_3	0	no action
					1	detection k28_3 in In<x> affects i_In<x>
			0	XY_INTR_ENA_MISC	0	no action
					1	detection depends on intr_misc_ena
00FBh 02FBh 04FBh	R/W	XY_CNTRL_FLAGCNT_LN01	7	XY_RST_CFC_LN1		reset flagcnt In1
			6:4	XY_SEL_CFC_LN1[2:0]		select cnt enable flagcnt In1 (see Table 42)
			3	XY_RST_CFC_LN0		reset flagcnt In0
			2:0	XY_SEL_CFC_LN0[2:0]		select cnt enable flagcnt In0 (see Table 42)
00FCh 02FCh 04FCh	R/W	XY_CNTRL_FLAGCNT_LN23	7	XY_RST_CFC_LN3		reset flagcnt In3
			6:4	XY_SEL_CFC_LN3[2:0]		select cnt enable flagcnt In3 (see Table 42)
			3	XY_RST_CFC_LN2		reset flagcnt In2
			2:0	XY_SEL_CFC_LN2[2:0]		select cnt enable flagcnt In2 (see Table 42)
00FDh 02FDh 04FDh	R/W	XY_MON_FLAGS_RESET	7	XY_RST_NIT_ERRFLAGS		reset nit error monitor flags
			6	XY_RST_DISP_ERR_FLAGS		reset disparity monitor flags
			5	XY_RST_KOUT_FLAGS		reset k symbols monitor flags
			4	XY_RST_KOUT_UNEXPECTED_FLAGS		reset unexpected k symbols monitor flags
			3	XY_RST_K28_LN3_FLAGS		reset k28_x monitor flags for In3
			2	XY_RST_K28_LN2_FLAGS		reset k28_x monitor flags for In2
			1	XY_RST_K28_LN1_FLAGS		reset k28_x monitor flags for In1
			0	XY_RST_K28_LN0_FLAGS		reset k28_x monitor flags for In0

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
00FEh 02FEh 04FEh	R/W	XY_DBG_CNTRL	7	XY_BER_MODE	0	no action
					1	simple BER measurement enabled
			6	XY_DBG_INTR_CLEAR	0	no action
					1	clear interrupt (to 1')'
			5:3	XY_INTR_MODE	000	intr depends on i_ln0
					001	intr depends on i_ln1
					010	intr depends on i_ln2
					011	intr depends on i_ln3
					100	intr depends on i_ln0 or i_ln2
					101	intr depends on i_ln0 or i_ln1 or i_ln2 or i_ln3
					110	hold_flagcnt
					111	no interrupt
			2:0	NOT USED		
		PRBS, JTSPAT, BER controls and indicator DAC XY				
0100h 0300h 0500h	R/W	XY_BER_CNTRL_0	7:6	XY_SEL_XBERT_LN[1:0]	00	xbert operate on ln0
					01	xbert operate on ln1
					10	xbert operate on ln2
					11	xbert operate on ln3
			5	XY_CHECK_PRBS	0	sync to prbs sequence
					1	check prbs sequence
			4	NOT USED		
			3:1	XY_XBERT_CNTRL[2: 0]	000	idle mode
					001	enable JTSPAT
					010	enable prbs31
					011	enable prbs23
					100	enable prbs15
					101	enable prbs7
					others	idle
			0	XY_SR_XBERT_CNT	0	no action
					1	reset xbert_cnt
0101h 0301h	Wr	XY_BER_CNTRL_1	6:0	XY_START_WIN_JTSPAT[6:0]		start win jstpat gen
0501h	R	XY_CA_01_STATUS	7	XY_CA_ERR_FLG_LN1		
			6	XY_NO_ACT_F20_FLG_LN1		
			5	XY_F20_HT_WCLK_FLG_LN1		
			4	XY_F20_LT_WCLK_FLG_LN1		
			3	XY_CA_ERR_FLG_LN0		
			2	XY_NO_ACT_F20_FLG_LN0		
			1	XY_F20_HT_WCLK_FLG_LN0		
			0	XY_F20_LT_WCLK_FLG_LN0		

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0102h 0302h 0502h	Wr	XY_BER_CNTRL_2	6:0	XY_STOP_WIN_JTSPAT[6:0]		stop window jtspat gen
	R	XY_CA_02_STATUS	7	XY_CA_ERR_FLG_LN3		
			6	XY_NO_ACT_F20_FLG_LN3		
			5	XY_F20_HT_WCLK_FLG_LN3		
			4	XY_F20_LT_WCLK_FLG_LN3		
			3	XY_CA_ERR_FLG_LN2		
			2	XY_NO_ACT_F20_FLG_LN2		
			1	XY_F20_HT_WCLK_FLG_LN2		
			0	XY_F20_LT_WCLK_FLG_LN2		
0103h 0303h 0503h	Wr	XY_BER_CNTRL_3	7:4	XY_STLTP_LN_MASK[3:0]		indicates lanes used for stltp_err_flag
			3:2	NOT USED		
			1	XY_RST_STLTP_FLAG	0	normal operation
					1	reset stltp_err_flag
			0	XY_RST_XBERT_FLAG	0	normal operation
					1	reset xbert_flag
	R	XY_AB_SWAP_STATUS	5	XY_XBERT_FLAG		indicates if xbert_cnt exceeds ber_level_ln0
			4	XY_STLTP_ERR_FLAG		indicates if error occure in STLTP
			3	XY_AB_SWAP_LN3		xy_swap status for lane ln3
			2	XY_AB_SWAP_LN2		xy_swap status for lane ln2
			1	XY_AB_SWAP_LN1		xy_swap status for lane ln1
			0	XY_AB_SWAP_LN0		xy_swap status for lane ln0
0104h 0304h 0504h	R	XY_XBERT_CNT_LSB	7:0	XY_XBERT_CNT[7:0]		lsb's of xbertest counter'
0105h 0305h 0505h	R	XY_XBERT_CNT_MSB	7:0	XY_XBERT_CNT[15:8]		msb's of xbertest counter'
010Ch 030Ch 050Ch	R	XY_FIRSTBER_JSTPAT	7	NOT USED		
			6:0	XY_FIRSTBER_JSTPAT[6:0]		indicates first jtspat with ber for selected lane
0110h 0310h 0510h	R	XY_FIRSTXBERPAT_LSB	7:0	XY_FIRSTBERPAT[7:0]		first ber pattern (lsbs)'
0111h 0311h 0511h	R	XY_FIRSTXBERPAT_MSB	7:3	NOT USED		
			2:0	XY_FIRSTBERPAT_LN0[9:8]		first ber pattern (msbs)'
0112h 0312h 0512h	R/W	XY_BER_LEVEL_P_LN0_LSB	7:0	XY_BER_LEVEL_P_LN0[7:0]		lsb's of berlevel_ln#0 (used for BER test)
0113h 0313h 0513h	R/W	XY_BER_LEVEL_P_LN0_MSB	7:0	XY_BER_LEVEL_P_LN0[15:8]		msb's of berlevel_ln#0 (used for BER test)
0114h 0314h 0514h	R/W	XY_BER_LEVEL_P_LN1_LSB	7:0	XY_BER_LEVEL_P_LN1[7:0]		lsb's of berlevel_ln#1 (used for BER test)
0115h 0315h 0515h	R/W	XY_BER_LEVEL_P_LN1_MSB	7:0	XY_BER_LEVEL_P_LN1[15:8]		msb's of berlevel_ln#1 (used for BER test)
0116h 0316h 0516h	R/W	XY_BER_LEVEL_P_LN2_LSB	7:0	XY_BER_LEVEL_P_LN2[7:0]		lsb's of berlevel_ln#2 (used for BER test)

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0117h 0317h 0517h	R/W	XY_BER_LEVEL_P_LN2_MSB	7:0	XY_BER_LEVEL_P_LN2[15:8]		msb's of berlevel_ln#2 (used for BER test)
0118h 0318h 0518h	R/W	XY_BER_LEVEL_P_LN3_LSB	7:0	XY_BER_LEVEL_P_LN3[7:0]		lsb's of berlevel_ln#3 (used for BER test)
0119h 0319h 0519h	R/W	XY_BER_LEVEL_P_LN3_MSB	7:0	XY_BER_LEVEL_P_LN3[15:8]		msb's of berlevel_ln#30 (used for BER test)
011Ah 031Ah	Wr	XY_MAN_MFB_LN0	6:0	XY_MAN_MFB_LN0[6:0]		nr of multi fram ebytes i.s.o. force_mfb_ln0 is 1'
051Ah	R		6:0	XY_MFB_LN0[6:0]		measured nr of multiframe-bytes ln#0 (should be K-1)
011Bh 031Bh	Wr	XY_MAN_MFB_LN1	6:0	XY_MAN_MFB_LN1[6:0]		nr of multi frame bytes i.s.o. force_mfb_ln1 is 1'
051Bh	R		6:0	XY_MFB_LN1[6:0]		measured nr of multiframe-bytes ln#1 (should be K-1)
011Ch 031Ch	Wr	XY_MAN_MFB_LN2	6:0	XY_MAN_MFB_LN2[6:0]		nr of multi frame bytes i.s.o. force_mfb_ln2 is 1'
051Ch	R		6:0	XY_MFB_LN2[6:0]		measured nr of multiframe-bytes ln#2 (should be K-1)
011Dh 031Dh	Wr	XY_MAN_MFB_LN3	6:0	XY_MAN_MFB_LN3[6:0]		nr of multi frame bytes i.s.o. force_mfb_ln3 is 1'
051Dh	R		6:0	XY_MFB_LN3[6:0]		measured nr of multiframe-bytes ln#3 (should be K-1)
011Eh 031Eh 051Eh	R/W	XY_FORCE_MFB_LN(X)	3	XY_FORCE_MFB_LN3	0	no action
					1	force man_mfb_ln3 to ILA cntrl
			2	XY_FORCE_MFB_LN2	0	no action
					1	force man_mfb_ln3 to ILA cntrl
			1	XY_FORCE_MFB_LN1	0	no action
					1	force man_mfb_ln3 to ILA cntrl
			0	XY_FORCE_MFB_LN0	0	no action
					1	force man_mfb_ln3 to ILA cntrl
		Configuration Data of Physical Lane 0 DAC XY				
0120h 0320h 0520h	R	XY_P_LN0_CFG_0	7:0	XY_P_LN0_DID[7:0]		Device IDentification Link (physical lane0)
0121h 0321h 0521h	R	XY_P_LN0_CFG_1	7:4	XY_P_LN0_ADJCNT[3:0]		LMFC Adjustment Count# subclass2 (physical lane0)
			3:0	XY_P_LN0_BID[3:0]		Bank IDentification (physical lane0)
0122h 0322h 0522h	R	XY_P_LN0_CFG_2	6	XY_P_LN0_ADJDIR		LMFC Adjustment Direction# subclass2 (physical lane0)
			5	XY_P_LN0_PHADJ		Phase Adjustment request# subclass2 (physical lane0)
			4:0	XY_P_LN0_LID[4:0]		Lane Identification (physical lane0)
0123h 0323h 0523h	R	XY_P_LN0_CFG_3	7	XY_P_LN0_SCR		Scrambling Enabled (physical lane0)
			6:5	NOT USED		
			4:0	XY_P_LN0_L[4:0]		Number of Lanes (physical lane0)
0124h 0324h 0524h	R	XY_P_LN0_CFG_4	7:0	XY_P_LN0_F[7:0]		Number of Frames (physical lane0)
0125h 0325h 0525h	R	XY_P_LN0_CFG_5	4:0	XY_P_LN0_K[4:0]		Number of MultiFrames (physical lane0)
0126h 0326h 0526h	R	XY_P_LN0_CFG_6	7:0	XY_P_LN0_M[7:0]		Number of converters per device (physical lane0)

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0127h 0327h 0527h	R	XY_P_LN0_CFG_7	7:6	XY_P_LN0_CS[1:0]		Number of Controlbits per Sample (physical lane0)
			5	NOT USED		
			4:0	XY_P_LN0_N[4:0]		Converter resolution (physical lane0)
0128h 0328h 0528h	R	XY_P_LN0_CFG_8	7:5	XY_P_LN0_SUBCLASSV[2:0]		Device subclass version (physical lane0)
			4:0	XY_P_LN0_N[4:0]'		InputSample resolution (physical lane0)
0129h 0329h 0529h	R	XY_P_LN0_CFG_9	7:5	XY_P_LN0_JESDV[2:0]		JESD204 version (physical lane0)
			4:0	XY_P_LN0_S[4:0]		Number of Samples per Frame per Converter (physical lane0)
012Ah 032Ah 052Ah	R	XY_P_LN0_CFG_10	7	XY_P_LN0_HD		High Density Format (physical lane0)
			6:5	NOT USED		
			4:0	XY_P_LN0_CF[4:0]		Number of Control words per Frame per Link (physical lane0)
012Bh 032Bh 052Bh	R	XY_P_LN0_CFG_11	7:0	XY_P_LN0_RES1[7:0]		Reserved Field #1 (physical lane0)
012Ch 032Ch 052Ch	R	XY_P_LN0_CFG_12	7:0	XY_P_LN0_RES2[7:0]		Reserved Field #2 (physical lane0)
012Dh 032Dh 052Dh	R	XY_P_LN0_CFG_13	7:0	XY_P_LN0_FCHK[7:0]		CheckSum (physical lane0)
DLP strobe lane selection and read data for Physical Lane 0 or 1DAC XY						
012Eh 032Eh 052Eh	R	XY_LN10_SAMPLE_LSB	7:0	XY_LN10_SAMPLE[7:0]		ln0_ or ln1_data_ila (sampled by dlp_strobe)
012Fh 032Fh 052Fh	R	XY_LN10_SAMPLE_MSB	7:0	XY_LN10_SAMPLE[15:8]		ln0_ or ln1_data_ila (sampled by dlp_strobe)
Configuration Data of Physical Lane 1 DAC XY						
0130h 0330h 0530h	R	XY_P_LN1_CFG_0	7:0	XY_P_LN1_DID[7:0]		Device IDentification Link (physical lane1)
0131h 0331h 0531h	R	XY_P_LN1_CFG_1	7:4	XY_P_LN1_ADJCNT[3:0]		LMFC Adjustment Count# subclass2 (physical lane1)
			3:0	XY_P_LN1_BID[3:0]		Bank IDentification (physical lane1)
0132h 0332h 0532h	R	XY_P_LN1_CFG_2	6	XY_P_LN1_ADJDIR		LMFC Adjustment Direction# subclass2 (physical lane1)
			5	XY_P_LN1_PHADJ		Phase Adjustment request# subclass2 (physical lane1)
			4:0	XY_P_LN1_LID[4:0]		Lane Identification (physical lane1)
0133h 0333h 0533h	R	XY_P_LN1_CFG_3	7	XY_P_LN1_SCR		Scrambling Enabled (physical lane1)
			6:5	NOT USED		
			4:0	XY_P_LN1_L[4:0]		Number of Lanes (physical lane1)
0134h 0334h 0534h	R	XY_P_LN1_CFG_4	7:0	XY_P_LN1_F[7:0]		Number of Frames (physical lane1)
0135h 0335h 0535h	R	XY_P_LN1_CFG_5	4:0	XY_P_LN1_K[4:0]		Number of MultiFrames (physical lane1)
0136h 0336h 0536h	R	XY_P_LN1_CFG_6	7:0	XY_P_LN1_M[7:0]		Number of converters per device (physical lane1)

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0137h 0337h 0537h	R	XY_P_LN1_CFG_7	7:6	XY_P_LN1_CS[1:0]		Number of Controlbits per Sample (physical lane1)
			5	NOT USED		
			4:0	XY_P_LN1_N[4:0]		Converter resolution (physical lane1)
0138h 0338h 0538h	R	XY_P_LN1_CFG_8	7:5	XY_P_LN1_SUBCLASSV[2:0]		Device subclass version (physical lane1)
			4:0	XY_P_LN1_N[4:0]'		InputSample resolution (physical lane1)
0139h 0339h 0539h	R	XY_P_LN1_CFG_9	7:5	XY_P_LN1_JESDV[2:0]		JESD204 version (physical lane1)
			4:0	XY_P_LN1_S[4:0]		Number of Samples per Frame per Converter (physical lane1)
013Ah 033Ah 053Ah	R	XY_P_LN1_CFG_10	7	XY_P_LN1_HD		High Density Format (physical lane1)
			6:5	NOT USED		
			4:0	XY_P_LN1_CF[4:0]		Number of Control words per Frame per Link (physical lane1)
013Bh 033Bh 053Bh	R	XY_P_LN1_CFG_11	7:0	XY_P_LN1_RES1[7:0]		Reserved Field #1 (physical lane1)
013Ch 033Ch 053Ch	R	XY_P_LN1_CFG_12	7:0	XY_P_LN1_RES2[7:0]		Reserved Field #2 (physical lane1)
013Dh 033Dh 053Dh	R	XY_P_LN1_CFG_13	7:0	XY_P_LN1_FCHK[7:0]		CheckSum (physical lane1)
013Eh 033Eh 053Eh	W	XY_LN10_SELECT	7:1	NOT USED		
			0	XY_LN10_SEL	0	select ln0_data_ila for readout
					1	select ln1_data_ila for readout
Configuration Data of Physical Lane 2 DAC XY						
0140h 0340h 0540h	R	XY_P_LN2_CFG_0	7:0	XY_P_LN2_DID[7:0]		Device IDentification Link (physical lane2)
0141h 0341h 0541h	R	XY_P_LN2_CFG_1	7:4	XY_P_LN2_ADJCNT[3:0]		LMFC Adjustment Count# subclass2 (physical lane2)
			3:0	XY_P_LN2_BID[3:0]		Bank IDentification (physical lane2)
0142h 0342h 0542h	R	XY_P_LN2_CFG_2	6	XY_P_LN2_ADJDIR		LMFC Adjustment Direction# subclass2 (physical lane2)
			5	XY_P_LN2_PHADJ		Phase Adjustment request# subclass2 (physical lane2)
			4:0	XY_P_LN2_LID[4:0]		Lane Identification (physical lane2)
0143h 0343h 0543h	R	XY_P_LN2_CFG_3	7	XY_P_LN2_SCR		Scrambling Enabled (physical lane2)
			6:5	NOT USED		
			4:0	XY_P_LN2_L[4:0]		Number of Lanes (physical lane2)
0144h 0344h 0544h	R	XY_P_LN2_CFG_4	7:0	XY_P_LN2_F[7:0]		Number of Frames (physical lane2)
0145h 0345h 0545h	R	XY_P_LN2_CFG_5	4:0	XY_P_LN2_K[4:0]		Number of MultiFrames (physical lane2)
0146h 0346h 0546h	R	XY_P_LN2_CFG_6	7:0	XY_P_LN2_M[7:0]		Number of converters per device (physical lane2)
0147h 0347h 0547h	R	XY_P_LN2_CFG_7	7:6	XY_P_LN2_CS[1:0]		Number of Controlbits per Sample (physical lane2)
			5	NOT USED		
			4:0	XY_P_LN2_N[4:0]		Converter resolution (physical lane2)

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0148h 0348h 0548h	R	XY_P_LN2_CFG_8	7:5	XY_P_LN2_SUBCLASSV[2:0]		Device subclass version (physical lane2)
			4:0	XY_P_LN2_N[4:0]'		InputSample resolution (physical lane2)
0149h 0349h 0549h	R	XY_P_LN2_CFG_9	7:5	XY_P_LN2_JESDV[2:0]		JESD204 version (physical lane2)
			4:0	XY_P_LN2_S[4:0]		Number of Samples per Frame per Converter (physical lane2)
014Ah 034Ah 054Ah	R	XY_P_LN2_CFG_10	7	XY_P_LN2_HD		High Density Format (physical lane2)
			6:5	NOT USED		
			4:0	XY_P_LN2_CF[4:0]		Number of Control words per Frame per Link (physical lane2)
014Bh 034Bh 054Bh	R	XY_P_LN2_CFG_11	7:0	XY_P_LN2_RES1[7:0]		Reserved Field #1 (physical lane2)
014Ch 034Ch 054Ch	R	XY_P_LN2_CFG_12	7:0	XY_P_LN2_RES2[7:0]		Reserved Field #2 (physical lane2)
014Dh 034Dh 054Dh	R	XY_P_LN2_CFG_13	7:0	XY_P_LN2_FCHK[7:0]		CheckSum (physical lane2)
DLP strobe lane selection and read data for Physical Lane 2 or 3 DAC XY						
014Eh 034Eh 054Eh	R	XY_LN32_SAMPLE_LSB	7:0	XY_LN32_SAMPLE[7:0]		ln2_ or ln3_data_ila (sampled by dlp_strobe)
014Fh 034Fh 054Fh	R	XY_LN32_SAMPLE_MSB	7:0	XY_LN32_SAMPLE[15:8]		ln2_ or ln3_data_ila (sampled by dlp_strobe)
Configuration Data of Physical Lane 3 DAC XY						
0150h 0350h 0550h	R	XY_P_LN3_CFG_0	7:0	XY_P_LN3_DID[7:0]		Device IDentification Link (physical lane3)
0151h 0351h 0551h	R	XY_P_LN3_CFG_1	7:4	XY_P_LN3_ADJCNT[3:0]		LMFC Adjustment Count# subclass2 (physical lane3)
			3:0	XY_P_LN3_BID[3:0]		Bank IDentification (physical lane3)
0152h 0352h 0552h	R	XY_P_LN3_CFG_2	6	XY_P_LN3_ADJDIR		LMFC Adjustment Direction# subclass2 (physical lane3)
			5	XY_P_LN3_PHADJ		Phase Adjustment request# subclass2 (physical lane3)
			4:0	XY_P_LN3_LID[4:0]		Lane Identification (physical lane3)
0153h 0353h 0553h	R	XY_P_LN3_CFG_3	7	XY_P_LN3_SCR		Scrambling Enabled (physical lane3)
			6:5	NOT USED		
			4:0	XY_P_LN3_L[4:0]		Number of Lanes (physical lane3)
0154h 0354h 0554h	R	XY_P_LN3_CFG_4	7:0	XY_P_LN3_F[7:0]		Number of Frames (physical lane3)
0155h 0355h 0555h	R	XY_P_LN3_CFG_5	4:0	XY_P_LN3_K[4:0]		Number of MultiFrames (physical lane3)
0156h 0356h 0556h	R	XY_P_LN3_CFG_6	7:0	XY_P_LN3_M[7:0]		Number of converters per device (physical lane3)
0157h 0357h 0557h	R	XY_P_LN3_CFG_7	7:6	XY_P_LN3_CS[1:0]		Number of Controlbits per Sample (physical lane3)
			5	NOT USED		
			4:0	XY_P_LN3_N[4:0]		Converter resolution (physical lane3)

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0158h 0358h 0558h	R	XY_P_LN3_CFG_8	7:5	XY_P_LN3_SUBCLASSV[2:0]		Device subclass version (physical lane3)
			4:0	XY_P_LN3_N[4:0]'		InputSample resolution (physical lane3)
0159h 0359h 0559h	R	XY_P_LN3_CFG_9	7:5	XY_P_LN3_JESDV[2:0]		JESD204 version (physical lane3)
			4:0	XY_P_LN3_S[4:0]		Number of Samples per Frame per Converter (physical lane3)
015Ah 035Ah 055Ah	R	XY_P_LN3_CFG_10	7	XY_P_LN3_HD		High Density Format (physical lane3)
			6:5	NOT USED		
			4:0	XY_P_LN3_CF[4:0]		Number of Control words per Frame per Link (physical lane3)
015Bh 035Bh 055Bh	R	XY_P_LN3_CFG_11	7:0	XY_P_LN3_RES1[7:0]		Reserved Field #1 (physical lane3)
015Ch 035Ch 055Ch	R	XY_P_LN3_CFG_12	7:0	XY_P_LN3_RES2[7:0]		Reserved Field #2 (physical lane3)
015Dh 035Dh 055Dh	R	XY_P_LN3_CFG_13	7:0	XY_P_LN3_FCHK[7:0]		CheckSum (physical lane3)
015Eh 035Eh 055Eh	W	XY_LN32_SELECT	7:1	NOT USED		
			0	XY_LN32_SEL	0	select ln2_data_ila for readout
					1	select ln3_data_ila for readout
				RX-PHY controls DAC XY		
0160h 0360h 0560h	R/W	XY_HS_RX_CDR_DIV	2	XY_REF_TUNE_ENABLE	0	HS_REF is not continuous calibration mode
					1	HS_REF is in continuous calibration mode
			1	XY_HS_CALIBRATE_ENABLE	0	HS_REF not in calibration mode
					1	HS_REF in calibration mode (when hs_ref_tune_enable=0)
			0	XY_HS_REF_ENABLE	0	HS_REF module is disabled (power down)
					1	HS_REF module is enabled (active)
0162h 0362h 0562h	R/W	XY_HS_RX_CDR_DIV	7	XY_HS_RX_CDR_LOW_SPEED_ENABLE	0	low speed mode CDR disabled
					1	low speed mode CDR enabled
			6:5	XY_HS_RX_CDR_DIVM[1:0]		divm ratio used to divide refclk
			4:0	XY_HS_RX_CDR_DIVN[4:0]		divn ratio used in CDR reference loop
0167h 0367h 0567h		XY_HS_RX_EQ_CNTRL	4	XY_HS_RX_EQ_AUTO_ZERO_ENABLE	0	Equalizer auto zero mode disabled (for all lanes)
					1	Equalizer auto zero mode enabled (for all lanes)
			3	XY_HS_RX_3_EQ_ENABLE	0	Equalizer of rx_ln3 disabled (power down)
					1	Equalizer of rx_ln3 enabled (active)
			2	XY_HS_RX_2_EQ_ENABLE	0	Equalizer of rx_ln2 disabled (power down)
					1	Equalizer of rx_ln2 enabled (active)
			1	XY_HS_RX_1_EQ_ENABLE	0	Equalizer of rx_ln1 disabled (power down)
					1	Equalizer of rx_ln1 enabled (active)
			0	XY_HS_RX_0_EQ_ENABLE	0	Equalizer of rx_ln0 disabled (power down)
					1	Equalizer of rx_ln0 enabled (active)

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
0168h 0368h 0568h	R/W	XY_HS_RX_0_EQ_GAIN	2:0	XY_HS_RX_0_EQ_IF_GAIN[2:0]		sets ifgain for rx_ln0 equalizer
0169h 0369h 0569h	R/W	XY_HS_RX_1_EQ_GAIN	2:0	XY_HS_RX_1_EQ_IF_GAIN[2:0]		sets ifgain for rx_ln1 equalizer
016Ah 036Ah 056Ah	R/W	XY_HS_RX_2_EQ_GAIN	2:0	XY_HS_RX_2_EQ_IF_GAIN[2:0]		sets ifgain for rx_ln2 equalizer
016Bh 036Bh 056Bh	R/W	XY_HS_RX_3_EQ_GAIN	2:0	XY_HS_RX_3_EQ_IF_GAIN[2:0]		sets ifgain for rx_ln3 equalizer
0170h 0370h 0570h	R/W	XY_HS_RX_RT_VCM	5	XY_HS_RX_RT_VCMSEL	0	dontuse'
					1	rx_rt_modules configured for RXuse (all lanes)
			4:0	XY_HS_RX_RT_VCMREF[4:0]		sets common mode reference for hs_rx_rt (all lanes)
0171h 0371h 0571h	R/W	XY_HS_RX_RT_CNTRL	7	XY_HS_RX_3_RT_HIZ_ENABLE	0	hs_rx_ln3 input is 100 ? (differential impedance)
					1	hs_rx_ln3 input is highohmic
			6	XY_HS_RX_2_RT_HIZ_ENABLE	0	hs_rx_ln2 input is 100 ? (differential impedance)
					1	hs_rx_ln2 input is highohmic
			5	XY_HS_RX_1_RT_HIZ_ENABLE	0	hs_rx_ln1 input is 100 ? (differential impedance)
					1	hs_rx_ln1 input is highohmic
			4	XY_HS_RX_0_RT_HIZ_ENABLE	0	hs_rx_ln0 input is 100 ? (differential impedance)
					1	hs_rx_ln0 input is highohmic
			3	XY_HS_RX_3_RT_ENABLE	0	Termination of rx_ln3 disabled (power down)
					1	Termination of rx_ln3 enabled (active)
			2	XY_HS_RX_2_RT_ENABLE	0	Termination of rx_ln2 disabled (power down)
					1	Termination of rx_ln2 enabled (active)
			1	XY_HS_RX_1_RT_ENABLE	0	Termination of rx_ln1 disabled (power down)
					1	Termination of rx_ln1 enabled (active)
			0	XY_HS_RX_0_RT_ENABLE	0	Termination of rx_ln0 disabled (power down)
					1	Termination of rx_ln0 enabled (active)
0172h 0372h 0572h	R/W	XY_HS_RX_0_RT_REFSIZE	7:0	XY_HS_RX_0_RT_REFSIZE[8:1]		termination impedance finetuning hs_rx_ln0 (msbs)'
0173h 0373h 0573h	R/W	XY_HS_RX_1_RT_REFSIZE	7:0	XY_HS_RX_1_RT_REFSIZE[8:1]		termination impedance finetuning hs_rx_ln1 (msbs)'
0174h 0374h 0574h	R/W	XY_HS_RX_2_RT_REFSIZE	7:0	XY_HS_RX_2_RT_REFSIZE[8:1]		termination impedance finetuning hs_rx_ln2 (msbs)'
0175h 0375h 0575h	R/W	XY_HS_RX_0_RT_REFSIZE	7:0	XY_HS_RX_3_RT_REFSIZE[8:1]		termination impedance finetuning hs_rx_ln3 (msbs)'
0176h 0376h 0576h	R/W	XY_HS_RX_X_RT_REFSIZE	3	XY_HS_RX_3_RT_REFSIZE[0]		termination impedance finetuning hs_rx_ln3 (lsb)
			2	XY_HS_RX_2_RT_REFSIZE[0]		
			1	XY_HS_RX_1_RT_REFSIZE[0]		
			0	XY_HS_RX_0_RT_REFSIZE[0]		
SYNC levels and Test mode DAC XY						

Table 52. Dedicated registers (Continued)for DACs XY

Default settings are shown highlighted.

Address	Access	Register	Bit	Symbol	Value	Description
017Dh 037Dh 057Dh	R/W	XY_SYNC_CFG_CNTRL	7	XY_SYNC_ENABLE	0	sync buffer disabled (power down)
					1	sync buffer enabled (active)
			6:4	XY_SYNC_SET_VCM[2:0]		sets common mode outputvoltage of sync buffer
			3	NOT USED		
			2:0	XY_SYNC_SET_LEVEL[2:0]		sets output levels (swing) of sync buffer
017Eh 037Eh 057Eh	R/W	XY_SYNC_SEL_CNTRL	7	XY_SYNC_TEST_DATA_TX_ENABLE	0	normal operation (jesd204x syncb)
					1	test mode (sync output depends on sync_test_data_sel)
			6	NOT USED		
			5:4	XY_SYNC_TEST_DATA_SEL[1:0]	00	sync <= recovered clock from lane 0 / 20
					01	sync <= recovered clock from lane 1 / 20
					10	sync <= recovered clock from lane 2 / 20
					11	sync <= recovered clock from lane 3 / 20

12. PACKAGE OUTLINE

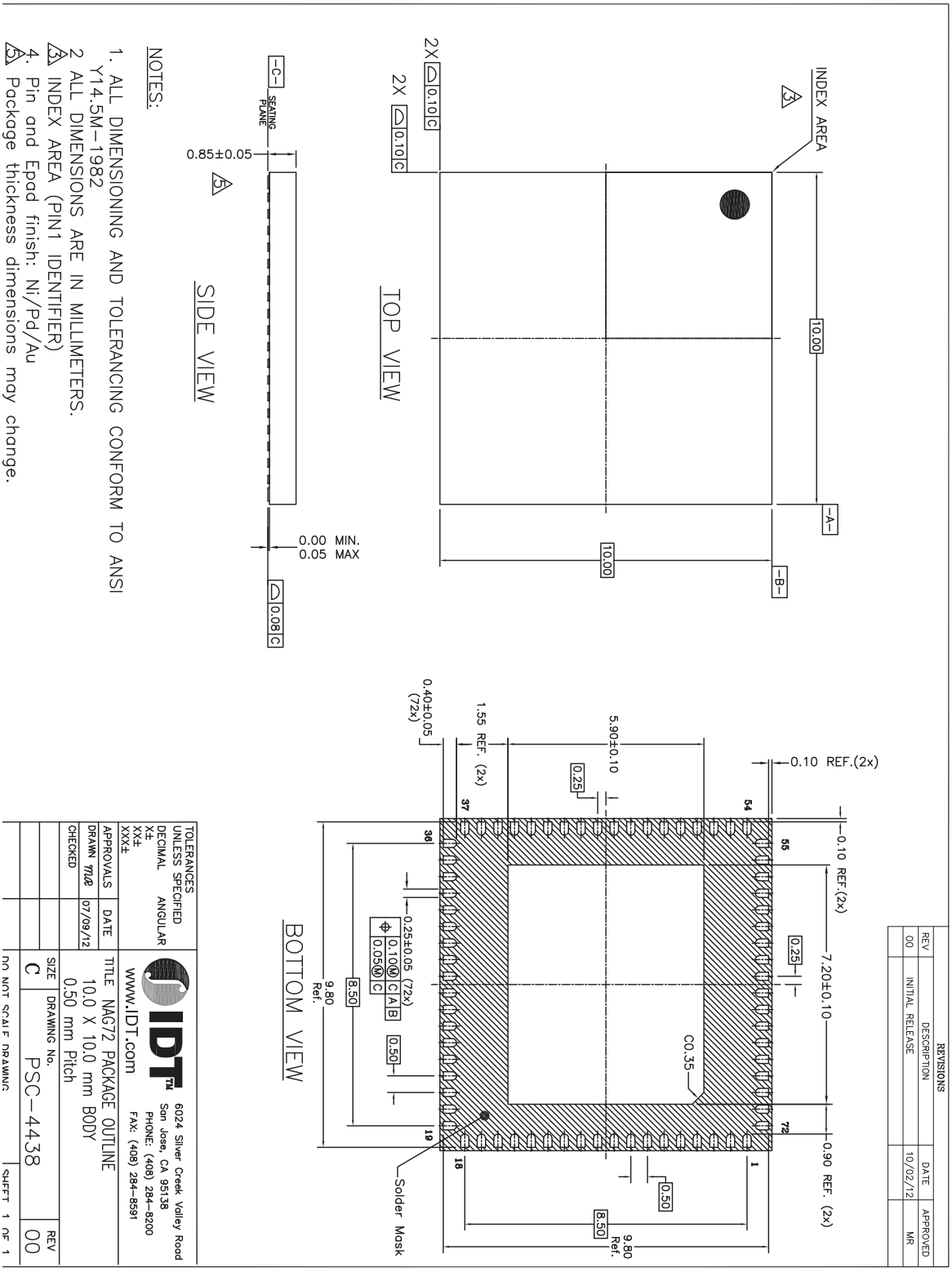


Fig 75. Package outline HLA72

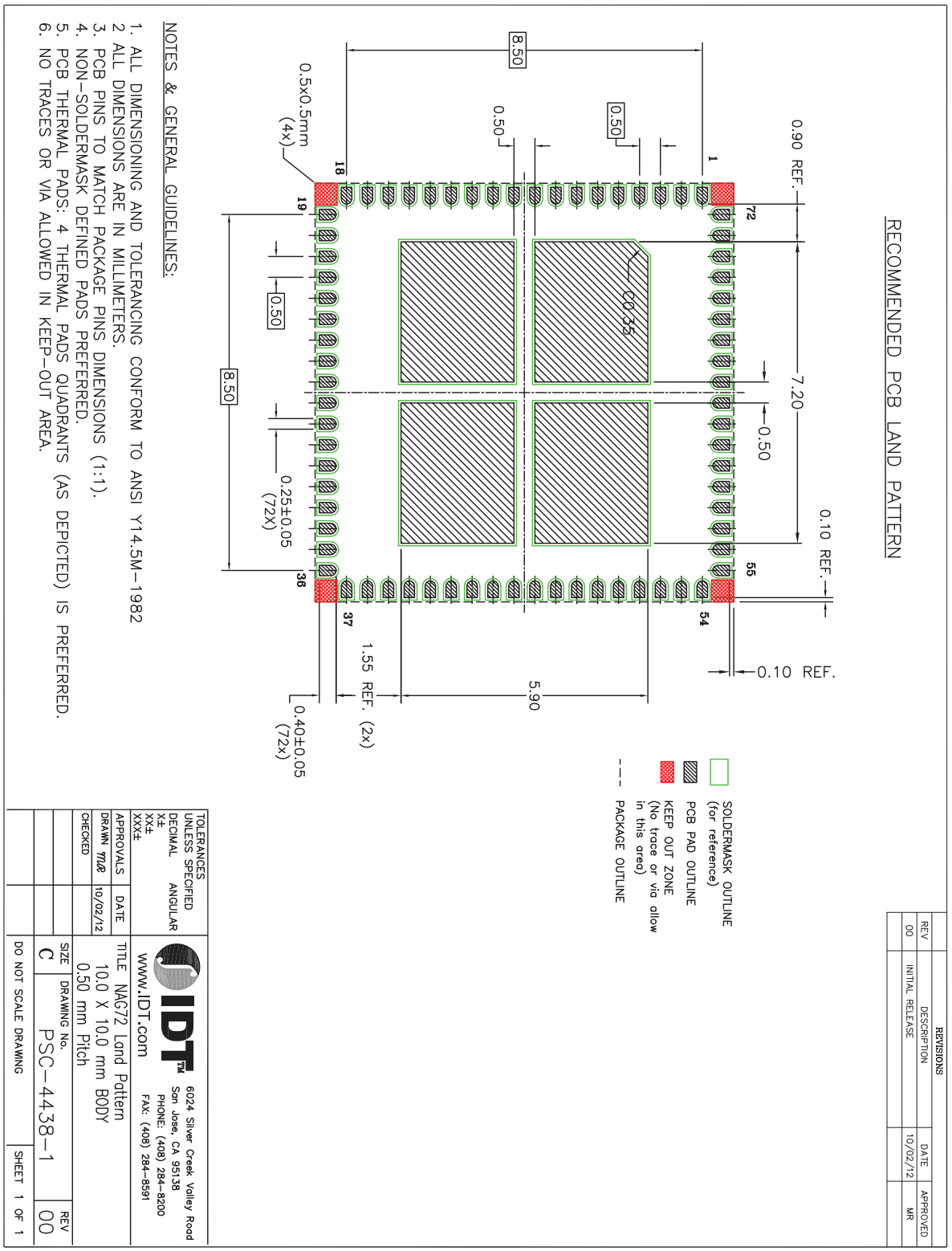


Fig 76. Footprint information for reflow soldering of HLA72 (PSC-4438) package

13. ABBREVIATIONS

Table 53. Abbreviations

Acronym	Description
BW	BandWidth
BWA	Broadband Wireless Access
CDI	Clock Domain Interface
CDMA	Code Division Multiple Access
CDR	Clock Data Recovery
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CTLE	Continuous Time Linear Equalization
DAC	Digital-to-Analog Converter
EDGE	Enhanced Data rates for GSM Evolution
FIR	Finite Impulse Response
GSM	Global System for Mobile communications
IF	Intermediate Frequency
IMD3	Third Order InterModulation
LMDS	Local Multipoint Distribution Service
LO	Local Oscillator
LTE	Long Term Evolution
LVDS	Low-Voltage Differential Signaling
MDS	Multiple Device Synchronization
MIMO	Multiple In Multiple Out
NCO	Numerically Controlled Oscillator
NMOS	Negative Metal-Oxide Semiconductor
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
SFDR	Spurious-Free Dynamic Range
SPI	Serial Peripheral Interface
WCDMA	Wide band Code Division Multiple Access
WLL	Wireless Local Loop

14. GLOSSARY

14.1 Static parameters

INL. The deviation of the transfer function from a best fit straight line (linear regression computation).

DNL. The difference between the ideal and the measured output value between successive DAC codes.

14.2 Dynamic parameters

Spurious-Free Dynamic Range (SFDR). The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the largest spurious observed (harmonic and non-harmonic, excluding DC component) in the frequency domain.

InterModulation Distortion (IMD). From a dual-tone digital input sine wave (these two frequencies being close together), the intermodulation distortion products IMD2 and IMD3 (second order and third order components) are defined below.

IMD2. The ratio between the RMS value of either tone and the RMS value of the worst second order intermodulation product.

IMD3. The ratio between the RMS value of either tone and the RMS value of the worst third order intermodulation product.

Total Harmonic Distortion (THD). The ratio between the RMS value of the harmonics of the output frequency and the RMS value of the output sine wave. Usually, the calculation of THD is done on the first 5 harmonics.

Signal-to-Noise Ratio (SNR). The ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise excluding the harmonics and the DC component.

Restricted BandWidth Spurious-Free Dynamic Range ($SFDR_{RBW}$). the ratio between the RMS value of the reconstructed output sine wave and the RMS value of the noise, including the harmonics, in a given bandwidth centered around f_{offset}.

15. Revision history

Table 54. Revision history

Document ID	Release date	Data sheet status
DAC1653Q; DAC1658Q v.2.20	2013/09/16	Advance data sheet
DAC1653Q; DAC1658Q v.2.21	2013/11/22	Advance data sheet
DAC1653Q; DAC1658Q v.2.3	2014/04/24	Advance data sheet. Apply for latest silicon revision .
DAC1653Q; DAC1658Q v.2.3.1	2014/06/05	Advance data sheet. Apply for latest silicon revision .

Table 55. Revision history

Item changed	Comments
previous revision to revision 2.3.1	
Maximum sampling rate	maximum sampling frequency changed from 1.5Gsps to 2 Gsps
Block diagram p. 4	typo corrected
Thermal characteristic	thermal behavior characteristics added.
PLL Fdco / Fref frequency range	value updated with latest silicon revision
Dynamics characteristics	all values and graph updated with latest silicon revision
Startup sequence	power up sequence and SPI start up sequence reviewed
Register name	register names aligned with SPI register map and updated with latest silicon revision
PLL	PLL chapter updated with latest silicon revision
AUX DAC	DAC1658Q device support also AUX DAC.
Equalizer	equalizer gain graph added
Register table	aligned with latest silicon revision
Mute rate	recommendation to use same mute rate for all mute events enabled
Minor typo error	

16. Contents

continued >>