

August 1991

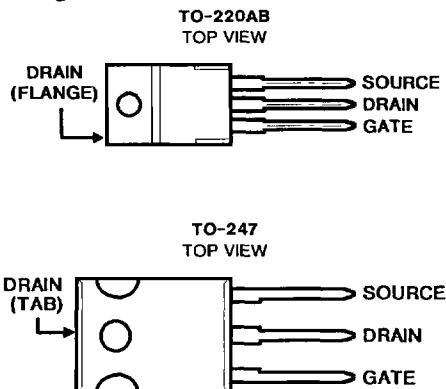
Features

- -30A, -50V
- $r_{DS(on)} = 0.065 \Omega$
- UIS SOA Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- 175°C Operating Temperature

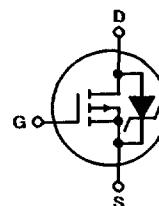
Description

The RFG30P05 and RFP30P05 p-channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFG30P05 is supplied in the JEDEC TO-247 plastic package and the RFP30P05 in the TO-220AB plastic package.

Packages

Terminal Diagram

P-CHANNEL ENHANCEMENT MODE


Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$), Unless Otherwise Specified

Drain-Source Voltage, V_{DSS}	-50V
Drain-Gate Voltage, ($R_{GS} = 1\text{m}\Omega$), V_{DGR}	-50V
Gate-Source Voltage, V_{GS}	$\pm 20\text{V}$
Drain Current:	
RMS Continuous, I_D	-30A
Pulsed, I_{DM}	-75A
Single Pulse Avalanche Rating, Refer to UIS SOA Curve	
Power Dissipation, P_D :	
$T_C = +25^\circ\text{C}$	120W
Derate Above $T_C = +25^\circ\text{C}$	0.8W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175°C

Specifications RFG30P05, RFP30P05

Electrical Characteristics ($T_C = +25^\circ\text{C}$) Unless Otherwise Specified

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 0.25 \text{ mA}, V_{GS} = 0\text{V}$	-50	-	V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{GS} = V_{DS}, I_D = 0.25 \text{ mA}$	2	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -40\text{V}, V_{GS} = 0\text{V}$	-	1	μA
		$T_C = 150^\circ\text{C}$		50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	100	nA
Static Drain-Source on Resistance	$r_{DS(\text{on})}$	$I_D = 30\text{A}, V_{GS} = -10\text{V}$	-	0.065	Ω
Turn-On Time	$t_{\text{(on)}}$	$V_{DD} = -25\text{V}, I_D = 15\text{A}$	-	80	ns
Turn-On Delay Time	$t_{d(\text{on})}$	$Ig1 = Ig2 = 0.8\text{A}$	15 (typ)	-	ns
Rise Time	t_r	$V_{GS(\text{clamp})}: -10\text{V}, +0.6\text{V}$	23 (typ)	-	ns
Turn-Off Delay Time	$t_{d(\text{off})}$	$R_L = 1.67\Omega$	28 (typ)	-	ns
Fall Time	t_f		18 (typ)	-	ns
Turn-Off Time	$t_{\text{off})}$		-	100	ns
Total Gate Charge	$Q_g(\text{total})$	$V_{GS} = 0 \text{ to } -20\text{V}$	-	200	nC
Gate Charge at -10V	$Q_g(-10\text{V})$	$V_{GS} = 0 \text{ to } -10\text{V}$	-	100	nC
Threshold Gate Charge	$Q_{g(\text{th})}$	$V_{GS} = 0 \text{ to } -2\text{V}$	-	2	nC
Plateau Voltage	$V_{(\text{plateau})}$	$I_D = 30\text{A}, V_{DS} = -15\text{V}$	-	-8	V
Turn-Off Energy Loss per Cycle	E_{off}	$V_{DD} = -25\text{V}, I_D = 15\text{A}, R_L = 1.67\Omega$ $L = 0.2\mu\text{H}, Ig1 = Ig2 = 0.8\text{A}$ $V_{GS(\text{clamp})}: -10\text{V}, +0.6\text{V}$	-	75	μJ
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	1.25	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$		-	80	$^\circ\text{C}/\text{W}$

Source-Drain Diode Ratings and Characteristics

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX.	
Diode Forward Voltage	V_{SD}	$I_{SD} = 30\text{A}$	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 30\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	150	ns

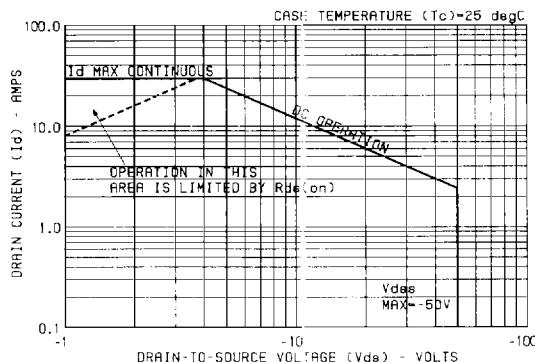


Figure 1 - Safe operating area curve. (Curves must be derated linearly with increase in temperature.)

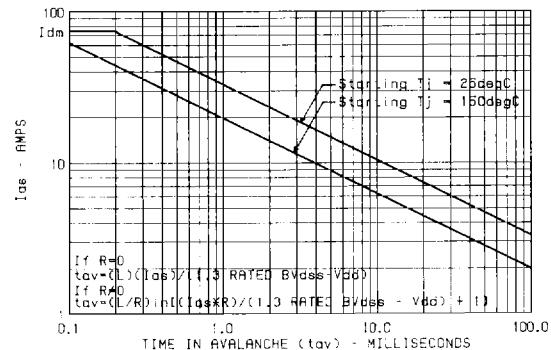


Figure 2 - Unclamped inductive-switching safe-operating-area curve. (Single pulse UIS SOA). See Figure 13 for test circuit.

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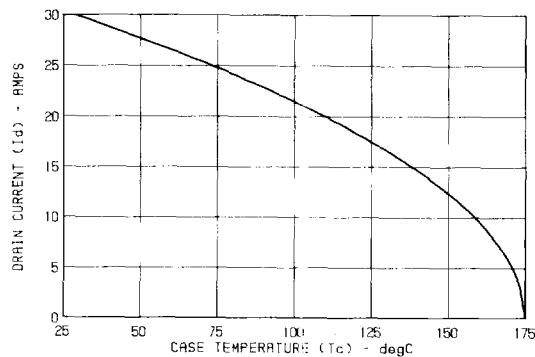


Figure 3 - Maximum continuous drain current vs case temperature.

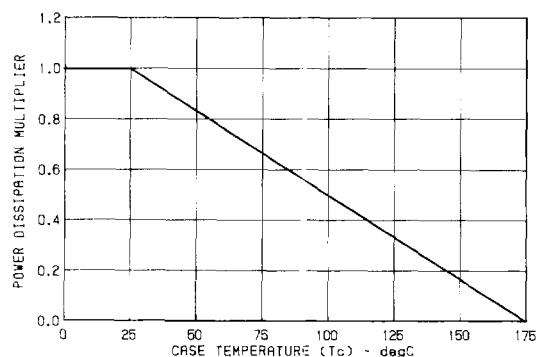


Figure 4 - Normalized power dissipation vs case temperature.

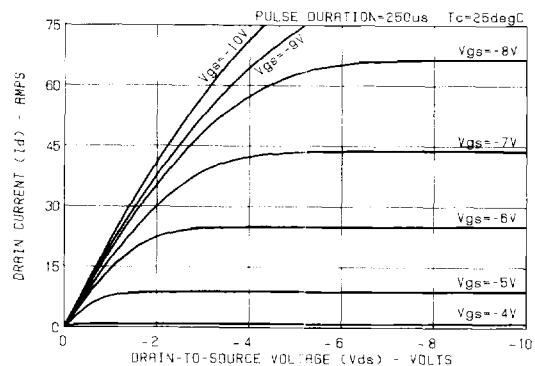


Figure 5 - Typical saturation characteristics.

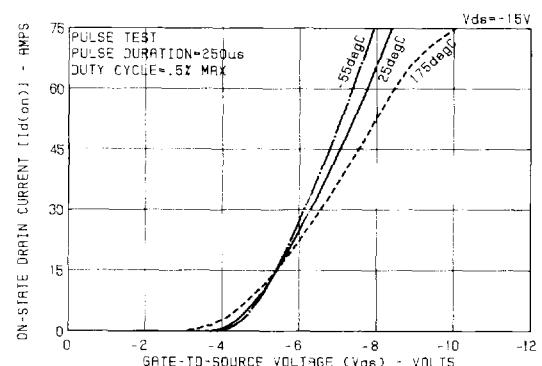


Figure 6 - Typical transfer characteristics.

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**P-CHANNEL
POWER MOSFETs**

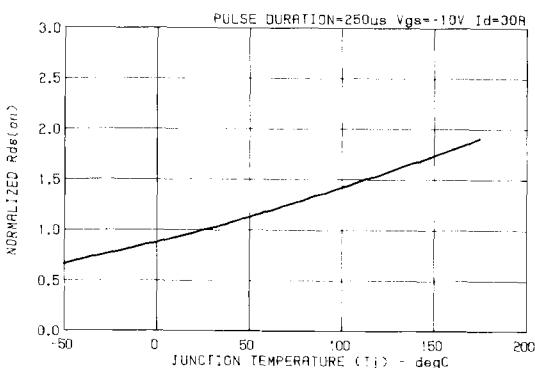


Figure 7 - Normalized on-state resistance vs junction temperature.

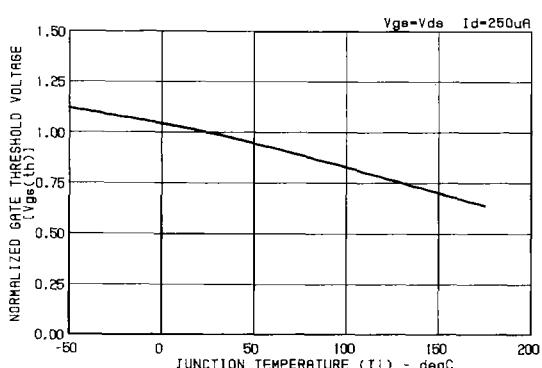


Figure 8 - Normalized gate threshold voltage vs junction temperature.

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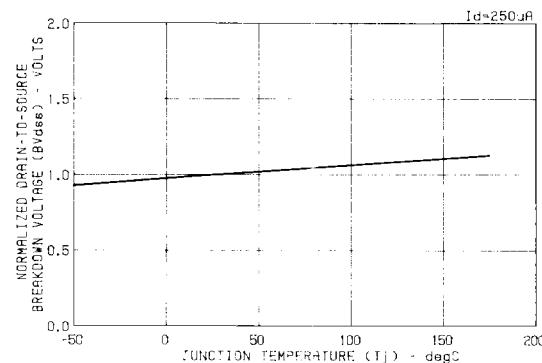


Figure 9 – Normalized drain source breakdown voltage vs junction temperature.

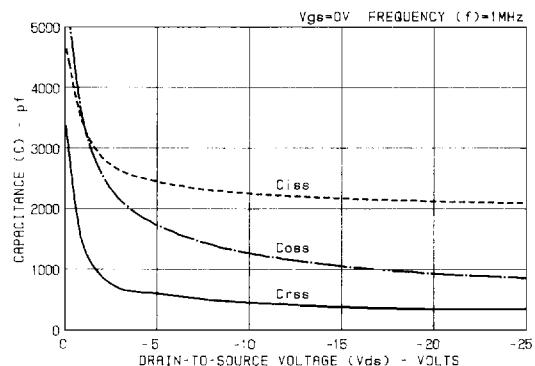


Figure 10 – Typical capacitance vs voltage.

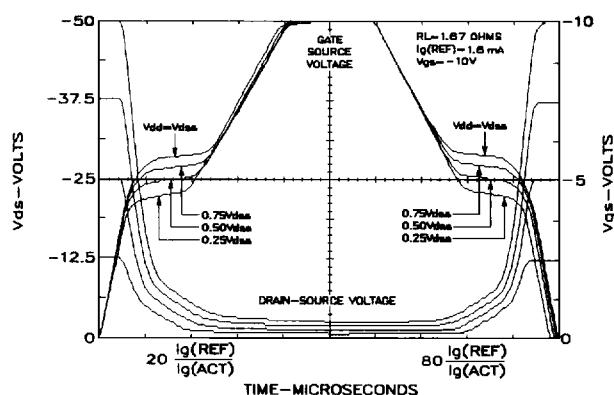


Figure 11 – Normalized switching waveforms for constant gate current.
(Refer to application notes AN-7254 and AN-7260.)

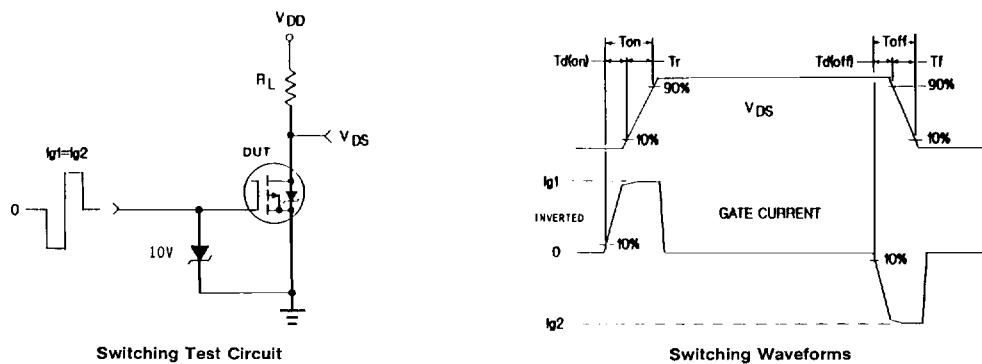


Figure 12 – Resistive switching.

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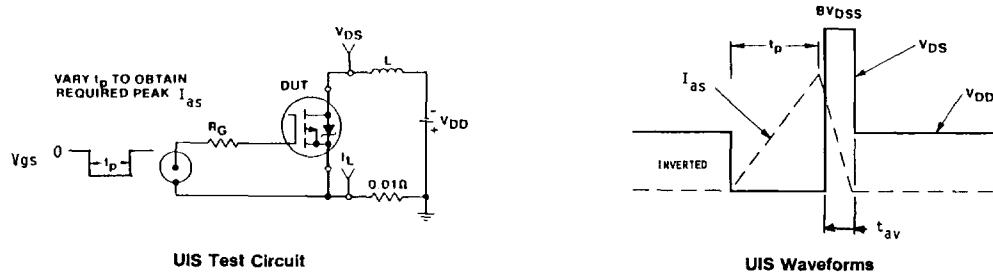


Figure 13 - Unclamped-inductive-switching test.