ISL43L841

Ultra Low ON-Resistance, Low-Voltage, Single Supply, Differential 4 to 1 Analog Multiplexer

FN6212
Rev 1.00
June 30, 2006

The Intersil ISL43L841 device contains precision, bidirectional, analog switches configured as a differential 4-channel multiplexer/demultiplexer. It is designed to operate from a single +1.65V to +4.5V supply. The device has an inhibit pin to simultaneously open all signal paths. With a supply voltage of 4.2V and logic high voltage of 2.85V at the logic inputs, the part draws only 20µA max of ICC current.

ON resistance is 0.47Ω with a +4.3V supply and 0.65Ω with a single +1.8V supply. Each switch can handle rail to rail analog signals. A channel can handle 300mA of continuous current. The part has low quiescent power consumption of 0.23µW max.

All digital inputs are 1.8V logic-compatible when using a single +3V supply.

The ISL43L841 is a differential 4 to 1 multiplexer device that is offered in a 16 Ld 3x3 TQFN package.

Table 1 summarizes the performance of this family.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	Diff 4:1 Mux
4.3V R_{ON}	0.47Ω
4.3V t_{ON}/t_{OFF}	22ns/12ns
3V R_{ON}	0.52Ω
3V t_{ON}/t_{OFF}	25ns/15ns
1.8V R_{ON}	0.65Ω
1.8V t_{ON}/t_{OFF}	40ns/17ns
PACKAGES	16 Ld 3x3 TQFN

Features

- Pb-Free Plus Anneal (RoHS Compliant)
- Pin Compatible Replacement for the MAX4782 and MAX4618
- ON Resistance (R_{ON})
  - V+ = +4.3V 0.47Ω
  - V+ = +3.0V 0.52Ω
  - V+ = +1.8V 0.65Ω
- R_{ON} Matching Between Channels. 0.12Ω
- R_{ON} Flatness Across Signal Range 0.056Ω
- Single Supply Operation. . . . . +1.65V to +4.5V
- Low Power Consumption (PD). . . . . <0.23µW
- Low ICC Current when VinH is not at the V+ Rail
- Fast Switching Action (V_S = +3V)
  - t_{ON} 25ns
  - t_{OFF} 15ns
- Guaranteed Break-Before-Make
- High Current Handling Capacity (300mA Continuous)
- Available in 16 Ld 3x3 TQFN
- 1.8V CMOS-Logic Compatible (+3V Supply)

Applications

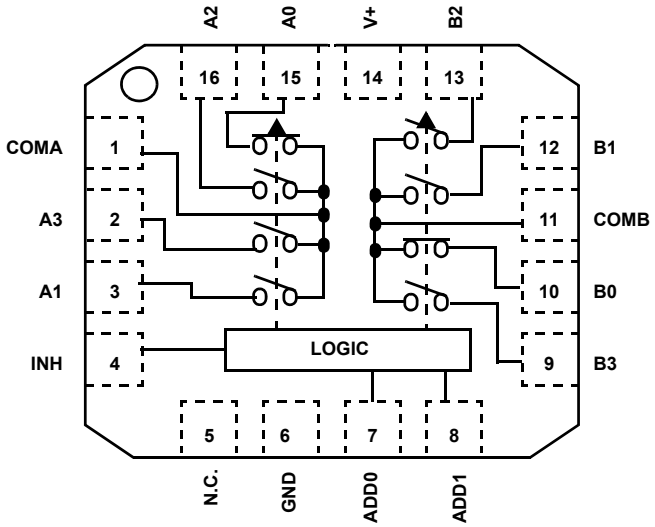
- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops
- Portable Test and Measurement
- Medical Equipment
- Audio and Video Switching

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

Pinout (Note 1)

ISL43L841 (3x3 TQFN)
TOP VIEW



NOTE:

1. Switches Shown for Logic “0” Inputs.

Truth Table

ISL43L841			
INH	**ADD0**	**ADD1**	**SWITCH ON**
1	X	X	NONE
0	0	0	A0, B0
0	0	1	A1, B1
0	1	0	A2, B2
0	1	1	A3, B3

NOTE: Logic “0” ≤0.5V. Logic “1” ≥1.4V, with a 3V supply. X = Don’t Care.

Pin Descriptions

PIN	FUNCTION
V+	System Power Supply Input (1.65V to 4.5V)
N.C.	N0 Connect. Not internally connected.
GND	Ground Connection
INH	Inhibit Input Pin. Connect to GND for Normal Operation. Connect to V+ to turn all switches off.
COMA	Analog Switch Channel A Output
COMB	Analog Switch Channel B Output
A0-A3	Analog Switch Channel A Input
B0-B3	Analog Switch Channel B Input
ADDx	Address Input Pin

Ordering Information

PART NO.	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL43L841IRZ (Note)	L81Z	-40 to 85	16 Ld 3x3 TQFN (Pb-Free)	L16.3x3A
ISL43L841IRZ-T (Note)	L81Z	-40 to 85	16 Ld 3x3 TQFN Tape and Reel (Pb-Free)	L16.3x3A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

V+ to GND . . . . . -0.3 to 4.7V
Input Voltages
INH, Ax, Bx, ADDx (Note 2) . . . . . -0.3 to (V+) + 0.3V
Output Voltages
COMx (Note 2) . . . . . -0.3 to (V+) + 0.3V
Continuous Current NO or COM . . . . . ±300mA
Peak Current NO or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±500mA
ESD Rating
HBM . . . . . >4kV

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
16 Ld 3x3 TQFN Package 75
Maximum Junction Temperature (Plastic Package). . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. Signals on Ax, Bx, COMx, ADDx, or INH exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.
3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

Electrical Specifications - 4.3V Supply

Test Conditions: V_{SUPPLY} = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.4V (Notes 4, 8), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 3.9V, I_{COM} = 100mA, $V_{AX\ or}$ V_{BX} = 0V to V+, (See Figure 5)	25	-	0.48	-	Ω
		Full	-	0.56	-	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 3.9V, I_{COM} = 100mA, $V_{AX\ or}$ V_{BX} = Voltage at max R_{ON}, (Note 6)	25	-	0.12	-	Ω
		Full	-	0.13	-	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 3.9V, I_{COM} = 100mA, $V_{AX\ or}$ V_{BX} = 0V t0 V+, (Note 7)	25	-	0.056	-	Ω
		Full	-	0.06	-	Ω
Ax or Bx OFF Leakage Current, $I_{Ax(OFF)}$ or $I_{Bx(OFF)}$	V+ = 4.5V, V_{COM} = 0.3V, 3V, $V_{AX\ or}$ V_{BX} = 3V, 0.3V	25	-50	1	50	nA
		Full	-150	-	150	nA
COM ON Leakage Current, $I_{COM(ON)}$	V+ = 4.5V, V_{COM} = $V_{AX\ or}$ V_{BX} = 0.3V, 3V	25	-50	0.6	50	nA
		Full	-150	-	150	nA
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	1.5	1.07	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	0.86	0.4	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = +4.5V, V_{INH} = V_{ADD} = 0V or V+ (Note 10)	Full	-0.5	-	0.5	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 3.9V, $V_{Ax\ or}$ V_{Bx} = 3.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	24	34	ns
		Full	-	-	38	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 3.9V, $V_{Ax\ or}$ V_{Bx} = 3.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	14	24	ns
		Full	-	-	28	ns
Address Transition Time, t_{TRANS}	V+ = 3.9V, $V_{AX\ or}$ V_{BX} = 3.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	21	31	ns
		Full	-	-	34	ns
Break-Before-Make Time, t_{BBM}	V+ = 4.5V, $V_{AX\ or}$ V_{BX} = 3.0V, R_L = 50Ω, C_L = 35pF, (See Figure 3, Note 10)	25	-	4	-	ns
		Full	1	-	-	ns

Electrical Specifications - 4.3V Supply

Test Conditions: V_{SUPPLY} = +3.9V to +4.5V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.4V (Notes 4, 8), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
Input OFF Capacitance, C_{OFF}	f = 1MHz, $V_{AX\ or}$ V_{BX} = V_{COM} = 0V, (See Figure 7)	25	-	62	-	pF
COM OFF Capacitance, C_{OFF}	f = 1MHz, $V_{AX\ or}$ V_{BX} = V_{COM} = 0V, (See Figure 7)	25	-	218	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, $V_{AX\ or}$ V_{BX} = V_{COM} = 0V, (See Figure 7)	25	-	232	-	pF
OFF Isolation	R_L = 50Ω, C_L = 35pF, f = 100kHz, (See Figures 4 and 6)	25	-	65	-	dB
Crosstalk, Note 9		25	-	-100	-	dB
Total Harmonic Distortion (THD)	f = 20Hz to 20kHz, 0.5Vp-p, R_L = 32Ω	25	-	0.02	-	%
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.65	-	4.5	V
Positive Supply Current, I+	V+ = 4.5V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	25	-	0.02	0.05	µA
		Full	-	-	0.9	µA
Positive Supply Current, I+	V+ = 4.2V, V_{ADDx} = 2.85V	25	-	10	20	µA

NOTES:

4. V_{IN} = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. R_{ON} matching between channels is calculated by subtracting the channel with the highest max R_{ON} value from the channel with lowest max R_{ON} value.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. Parts are 100% tested at +25°C. Limits across the full temperature range are guaranteed by design and correlation.
9. Between any two switches.
10. Guaranteed but not tested.

Electrical Specifications - 3V Supply

Test Conditions: V_{SUPPLY} = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.4V (Notes 4, 8) Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 2.7V, I_{COM} = 100mA, $V_{AX\ or}$ V_{BX} = 0V to V+, See Figure 5	25	-	0.53	0.75	Ω
		Full	-	-	0.8	Ω
R_{ON} Matching Between Channels, DR_{ON}	V+ = 2.7V, I_{COM} = 100mA, $V_{AX\ or}$ V_{BX} = Voltage at max R_{ON}, (Note 6)	25	-	0.12	0.2	Ω
		Full	-	-	0.2	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 2.7V, I_{COM} = 100mA, $V_{AX\ or}$ V_{BX} = 0V t0 V+, (Note 7)	25	-	0.056	0.15	Ω
		Full	-	-	0.15	Ω
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	1.4	0.8	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	0.67	0.4	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = 3.6V, V_{INH} = V_{ADD} = 0V or V+ (Note 10)	Full	-0.5	-	0.5	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 2.7V, $V_{Ax\ or}$ V_{Bx} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	27	37	ns
		Full	-	-	41	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 2.7V, $V_{Ax\ or}$ V_{Bx} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	16	26	ns
		Full	-	-	30	ns

Electrical Specifications - 3V Supply

Test Conditions: V_{SUPPLY} = +2.7V to +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.4V (Notes 4, 8) Unless Otherwise Specified **(Continued)**

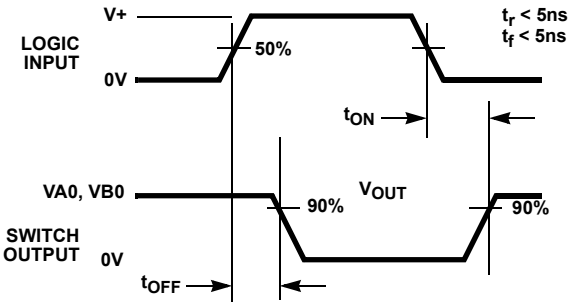
PARAMETER	TEST CONDITIONS	TEMP (°C)	(NOTE 5) MIN	TYP	(NOTE 5) MAX	UNITS
Address Transition Time, t_{TRANS}	V+ = 2.7V, V_{AX} or V_{BX} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	24	34	ns
		Full	-	-	38	ns
Break-Before-Make Time, t_{BBM}	V+ = 3.3V, V_{AX} or V_{BX} = 1.5V, R_L = 50Ω, C_L = 35pF, (See Figure 3, Note 10)	25	-	4	-	ns
		Full	1	-	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0W, (See Figure 2)	25	-	-65	-	pC
Input OFF Capacitance, C_{OFF}	f = 1MHz, V_{AX} or V_{BX} = V_{COM} = 0V, (See Figure 7)	25	-	62	-	pF
COM OFF Capacitance, C_{OFF}	f = 1MHz, V_{AX} or V_{BX} = V_{COM} = 0V, (See Figure 7)	25	-	218	-	pF
COM ON Capacitance, $C_{COM(ON)}$	f = 1MHz, V_{AX} or V_{BX} = V_{COM} = 0V, (See Figure 7)	25	-	232	-	pF
OFF Isolation	R_L = 50Ω, C_L = 35pF, f = 100kHz, (See Figures 4 and 6)	25	-	65	-	dB
Crosstalk, (Note 9)		25	-	-100	-	dB
Total Harmonic Distortion (THD)	f = 20Hz to 20kHz, 0.5Vp-p, RL = 32Ω	25	-	0.02	-	%
POWER SUPPLY CHARACTERISTICS						
Power Supply Range		Full	1.65	-	4.5	V
Positive Supply Current, I+	V+ = 3.6V, V_{INH}, V_{ADD} = 0V or V+, Switch On or Off	25	-	-	0.05	µA
		Full	-	-	0.9	µA

Electrical Specifications - 1.8V Supply

Test Conditions: V+ = +1.8V, GND = 0V, V_{INH} = 1V, V_{INL} = 0.4V (Notes 4, 8), Unless Otherwise Specified

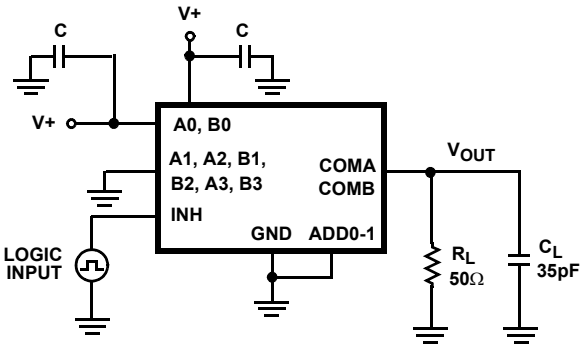
PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (NOTE 5)	TYP	MAX (NOTE 5)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Signal Range, V_{ANALOG}		Full	0	-	V+	V
ON Resistance, R_{ON}	V+ = 1.8V, I_{COM} = 10.0mA, V_{AX} or V_{BX} = 1.0V, (See Figure 5)	25	-	0.65	0.85	Ω
		Full	-	-	0.9	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V+ = 1.8V, I_{COM} = 10.0mA, V_{AX} or V_{BX} = 1.0V, (See Figure 5)	25	-	0.12	-	Ω
		Full	-	0.12	-	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V+ = 1.8V, I_{COM} = 10.0mA, V_{AX} or V_{BX} = 0V, 0.9V, 1.6V, (See Figure 5)	25	-	0.14	-	Ω
		Full	-	0.14	-	Ω
DIGITAL INPUT CHARACTERISTICS						
Input Voltage High, V_{INH}, V_{ADDH}		Full	1	-	-	V
Input Voltage Low, V_{INL}, V_{ADDL}		Full	-	-	0.4	V
Input Current, I_{INH}, I_{INL}, I_{ADDH}, I_{ADDL}	V+ = 1.8V, V_{INH}, V_{ADD} = 0V or V+, (Note 10)	Full	-0.5	-	0.5	µA
DYNAMIC CHARACTERISTICS						
Inhibit Turn-ON Time, t_{ON}	V+ = 1.8V, V_{Ax} or V_{Bx} = 1.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	40	50	ns
		Full	-	-	55	ns
Inhibit Turn-OFF Time, t_{OFF}	V+ = 1.8V, V_{Ax} or V_{Bx} = 1.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	17	27	ns
		Full	-	-	31	ns
Address Transition Time, t_{TRANS}	V+ = 1.8V, V_{AX} or V_{BX} = 1.0V, R_L = 50Ω, C_L = 35pF, (See Figure 1, Note 10)	25	-	32	42	ns
		Full	-	-	46	ns
Break-Before-Make Time, t_{BBM}	V+ = 1.8V, V_{AX} or V_{BX} = 1.0V, R_L = 50Ω, C_L = 35pF, (See Figure 3, Note 10)	25	-	9	-	ns
Charge Injection, Q	C_L = 1.0nF, V_G = 0V, R_G = 0Ω, (See Figure 2)	25	-	-39	-	pC

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

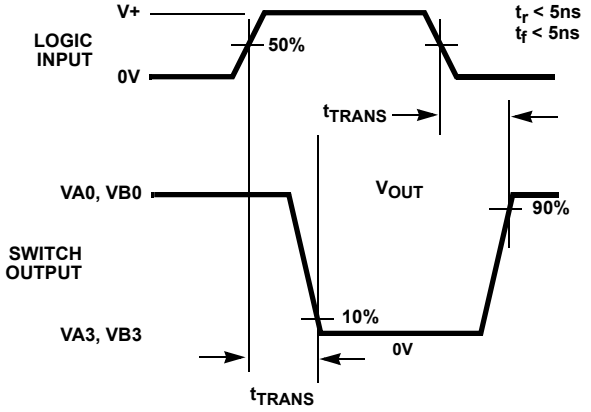
FIGURE 1A. INHIBIT t_{ON}/t_{OFF} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

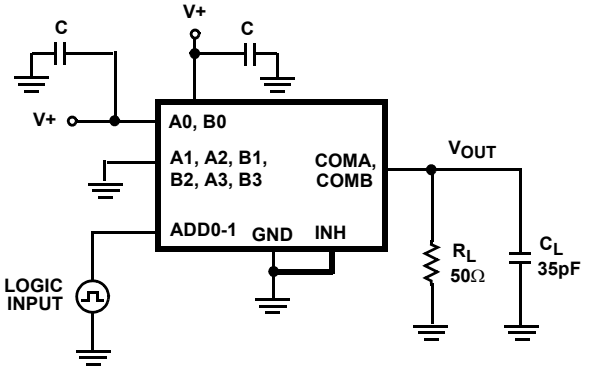
$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. INHIBIT t_{ON}/t_{OFF} TEST CIRCUIT



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS t_{TRANS} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1D. ADDRESS t_{TRANS} TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

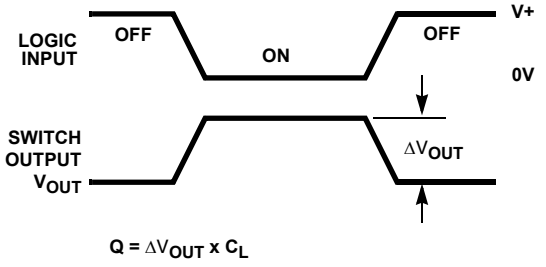
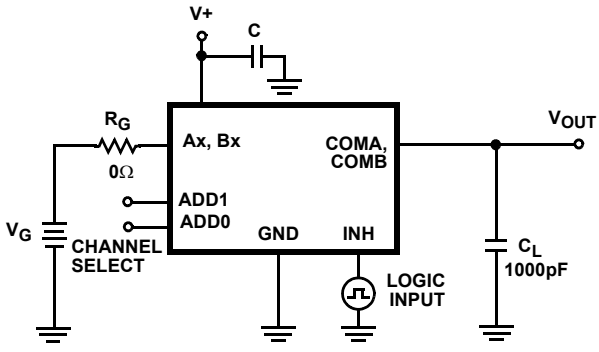


FIGURE 2A. Q MEASUREMENT POINTS



Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

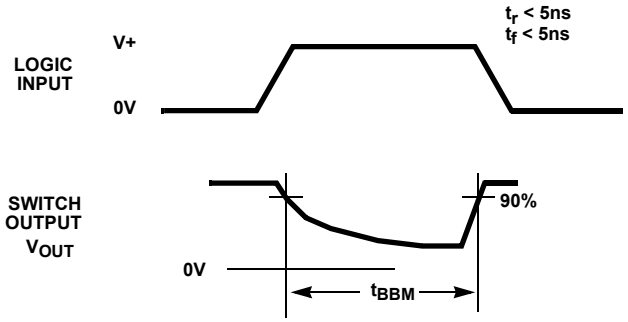
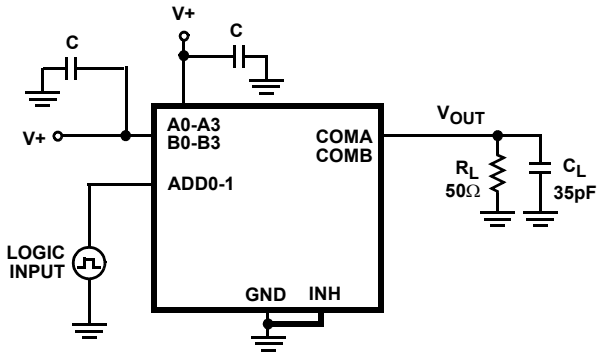


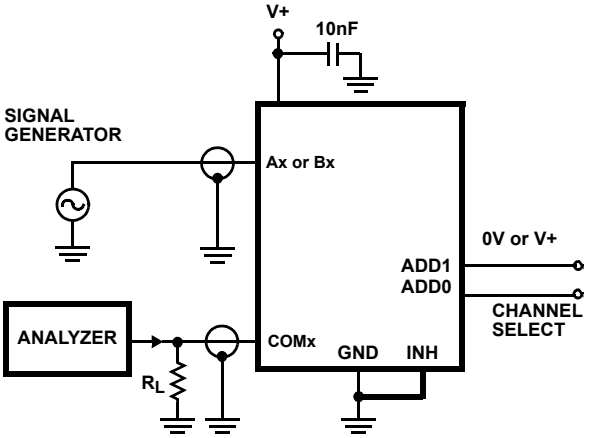
FIGURE 3A. t_{BBM} MEASUREMENT POINTS



Repeat test for other switches. C_L includes fixture and stray capacitance.

FIGURE 3B. t_{BBM} TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME



Off-Isolation is measured between COM and "Off" NO terminal on each switch.
Signal direction through switch is reversed and worst case values are recorded.

FIGURE 4. OFF ISOLATION TEST CIRCUIT

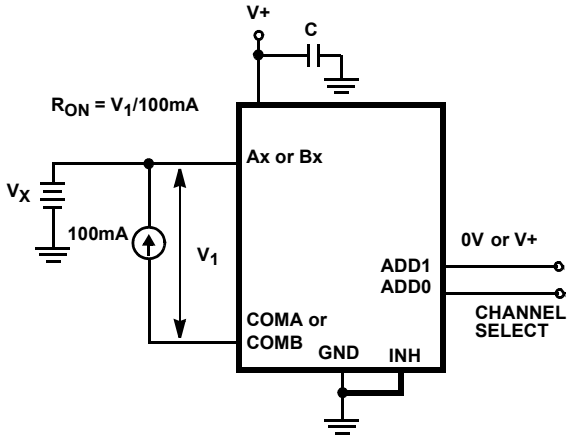
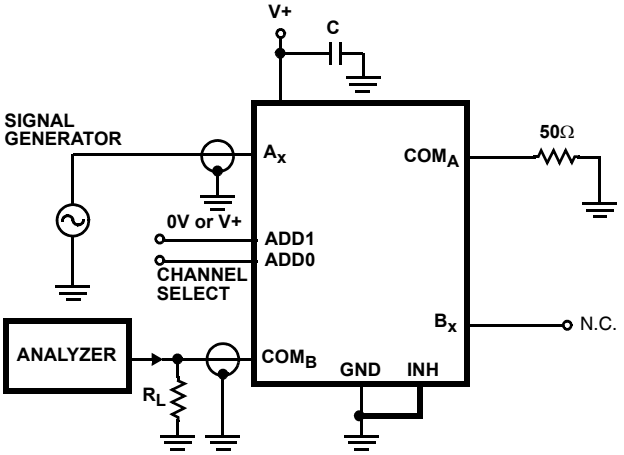


FIGURE 5. R_{ON} TEST CIRCUIT



Crosstalk is measured between adjacent channels with one channel ON and the other channel OFF.
Signal direction through switch is reversed and worst case values are recorded.

FIGURE 6. CROSSTALK TEST CIRCUIT

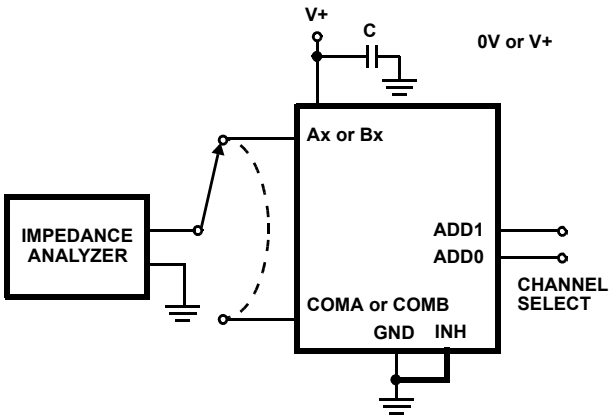


FIGURE 7. CAPACITANCE TEST CIRCUIT

Detailed Description

The ISL43L841 analog multiplexer offers precise switching capability from a single 1.65V to 4.5V supply with low on-resistance (0.47Ω) and high speed operation (t_{ON} = 24ns, t_{OFF} = 14ns). The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (1.65V), low power consumption (0.23µW), low leakage currents (50nA max). High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND.

If these conditions cannot be guaranteed, then precautions must be implemented to prohibit the current and voltage at the logic pins and signal pins from exceeding the maximum ratings of the switch. The following two methods can be used to provided additional protection to limit the current in the event that the voltage at a signal pin or logic pin goes below ground or above the V+ rail.

Logic inputs can be protected by adding a 1kΩ resistor in series with the logic input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the submicroamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low R_{ON} switch. Connecting schottky diodes to the signal pins as shown in Figure 8 will shunt the fault current to the supply or to ground thereby protecting the switch. These schottky diodes must be sized to handle the expected fault current.

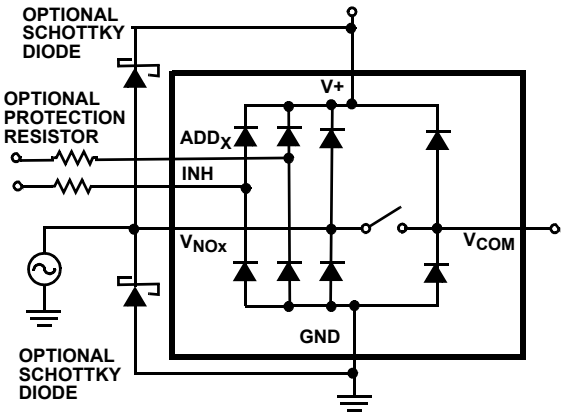


FIGURE 8. OVERVOLTAGE PROTECTION

Power-Supply Considerations

The ISL43L841 construction is typical of most CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL43L841 4.7V maximum supply voltage provides plenty of room for the 10% tolerance of 4.3V supply, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.65V but the part will operate with a supply below 1.65V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the electrical specification tables and *Typical Performance Curves* for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switch V+ and GND signals to drive the analog switch gate terminals.

This device cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

Logic-Level Thresholds

These devices are 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.5V to 4.5V (see Figure 15). At 2.5V the V_{INL} level is about 0.52V. This is still above the 1.8V CMOS guaranteed minimum level of 0.4V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL43L841 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 2.85V logic (0V to 2.85V) while operating with a 4.2V supply, the device draws only 10µA of current when both address inputs are high (see Figure 13 for V_{LOGIC} = 2.85V).

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 10MHz with a -3dB bandwidth of 70MHz (see Figure 19). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off Isolation is the resistance to this feed through, while Crosstalk indicates the amount of feed through from one switch to another. Figure 20 details the high Off Isolation and Crosstalk rejection provided by this family. At 100kHz, Off Isolation is about 65dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection

due to the voltage divider action of the switch OFF impedance and the load impedance.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified

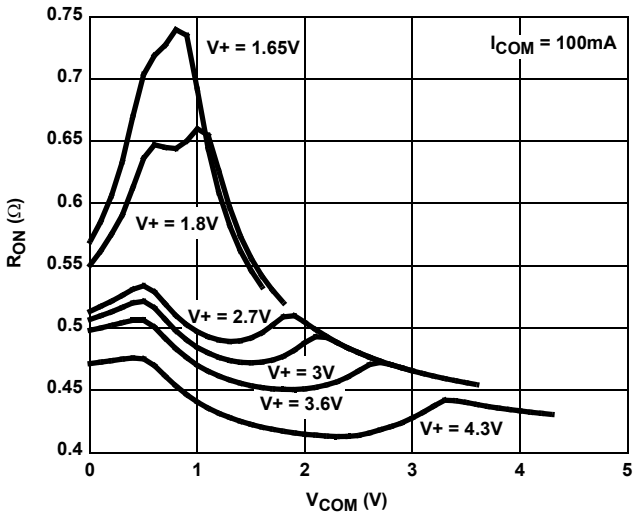


FIGURE 9. ON RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE

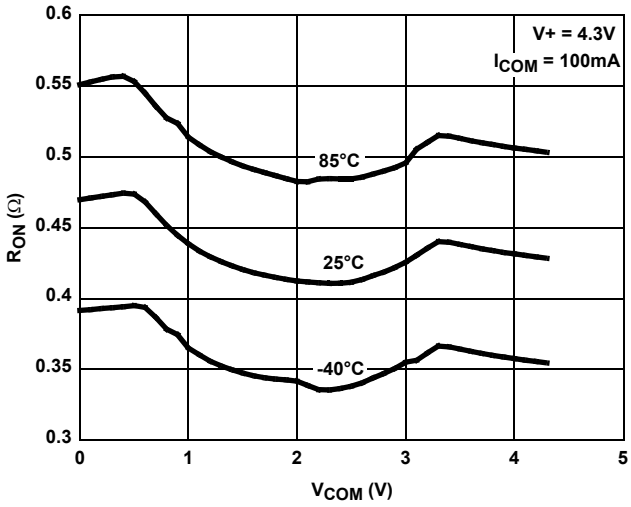


FIGURE 10. ON RESISTANCE vs SWITCH VOLTAGE

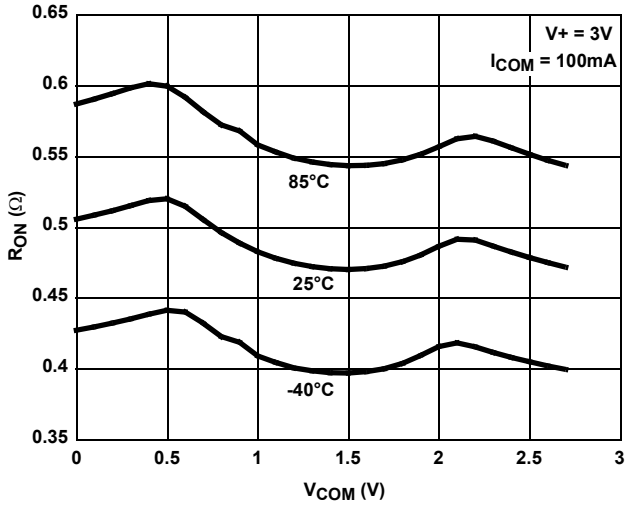


FIGURE 11. ON RESISTANCE vs SWITCH VOLTAGE

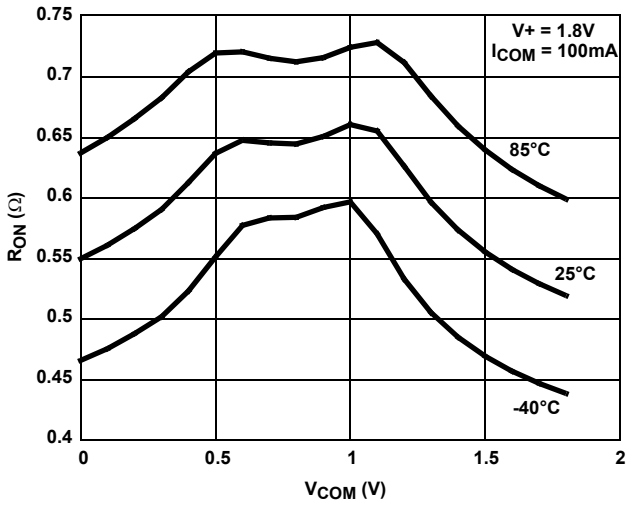


FIGURE 12. ON RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

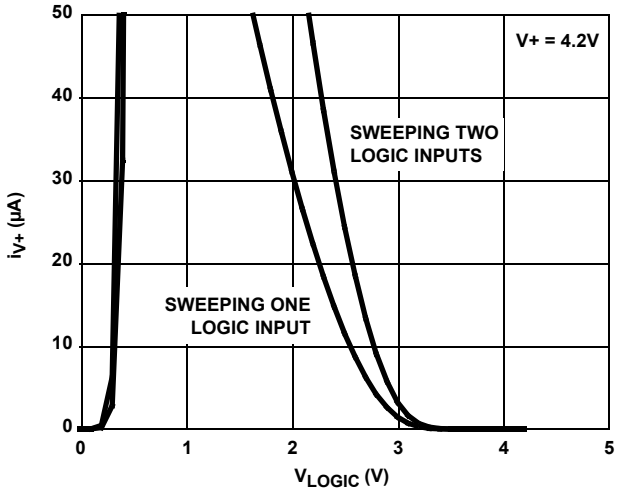


FIGURE 13. I+ CURRENT vs LOGIC VOLTAGE

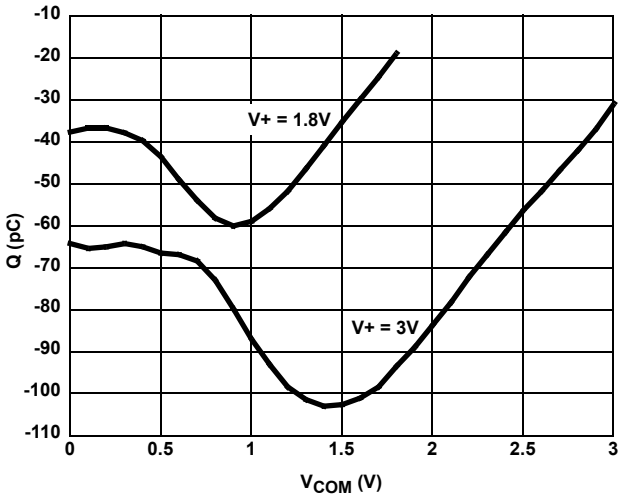


FIGURE 14. CHARGE INJECTION vs SWITCH VOLTAGE

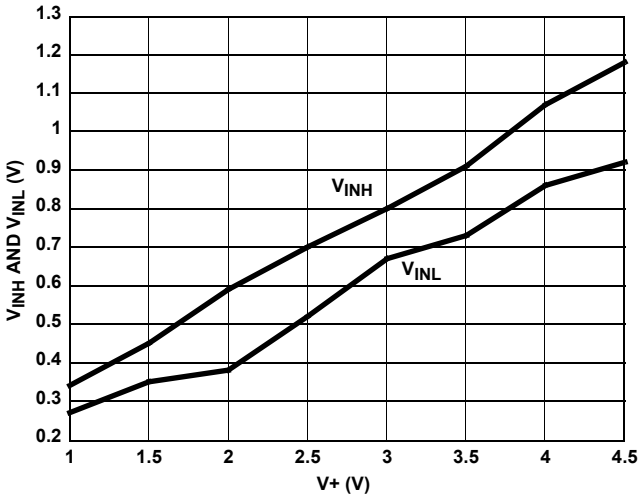


FIGURE 15. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

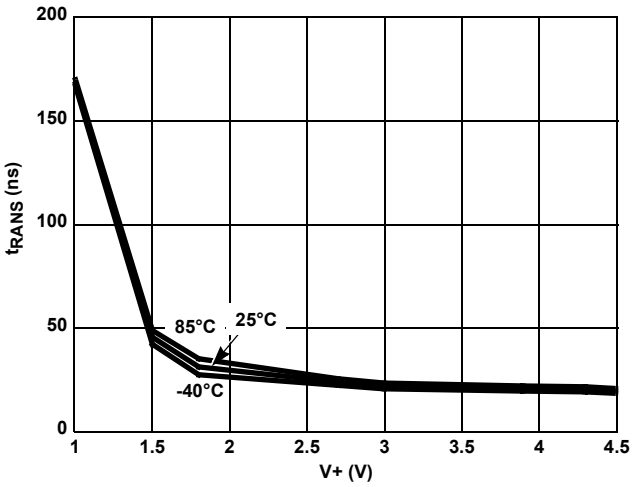


FIGURE 16. ADDRESS TRANS TIME vs SUPPLY VOLTAGE

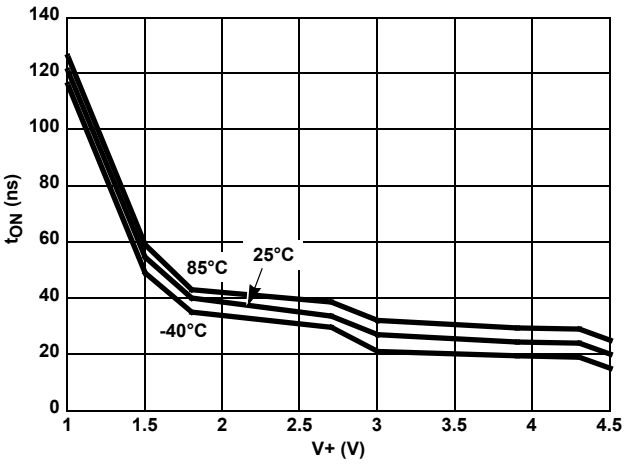


FIGURE 17. INHIBIT TURN - ON TIME vs SUPPLY VOLTAGE

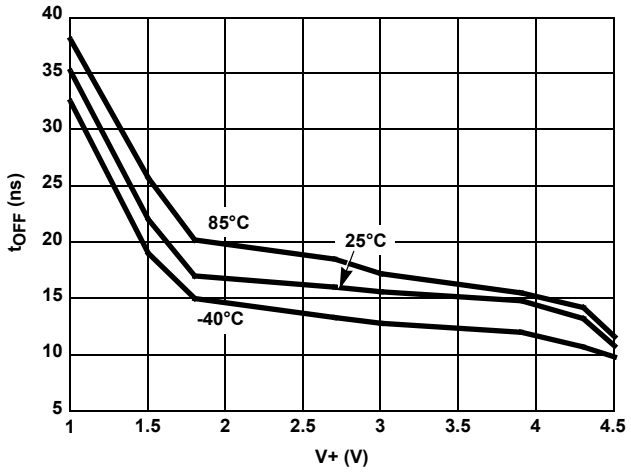


FIGURE 18. INHIBIT TURN - OFF TIME vs SUPPLY VOLTAGE

Typical Performance Curves T_A = 25°C, Unless Otherwise Specified **(Continued)**

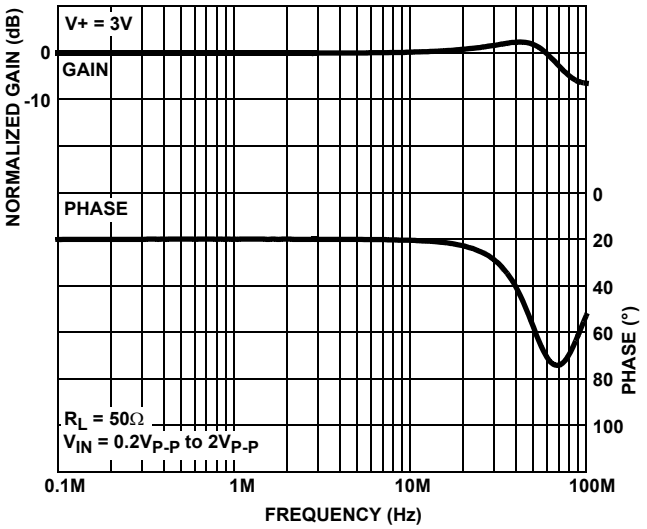


FIGURE 19. FREQUENCY RESPONSE

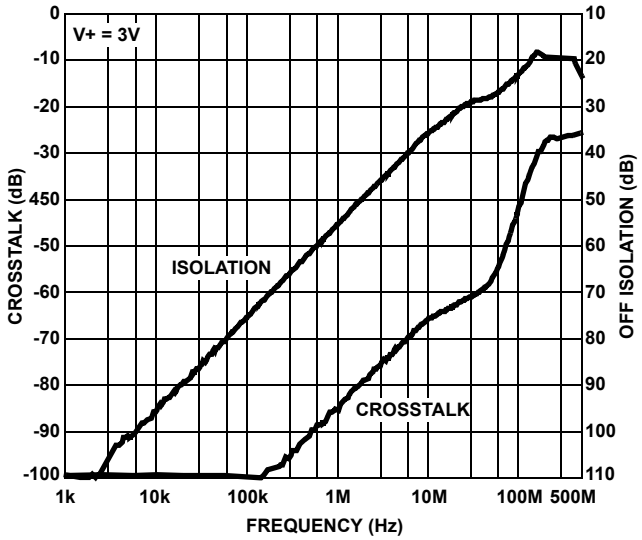


FIGURE 20. CROSSTALK AND OFF ISOLATION

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND (QFN Paddle Connection: To Ground or Float)

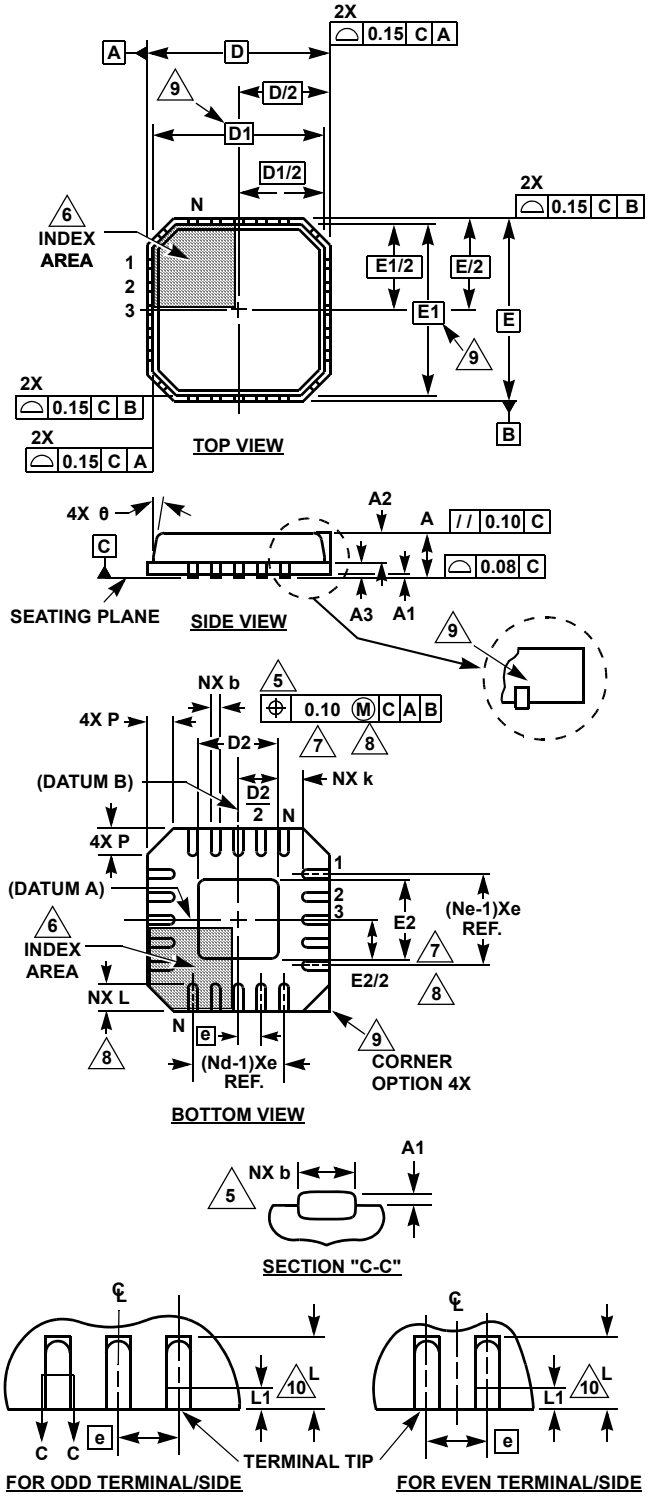
TRANSISTOR COUNT:

228

PROCESS:

Si Gate CMOS

Thin Quad Flat No-Lead Plastic Package (TQFN)
Thin Micro Lead Frame Plastic Package (TMLFP)



L16.3x3A

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A2	-	-	0.80	9
A3		0.20 REF		9
b	0.18	0.23	0.30	5, 8
D		3.00 BSC		-
D1		2.75 BSC		9
D2	1.35	1.50	1.65	7, 8, 10
E		3.00 BSC		-
E1		2.75 BSC		9
E2	1.35	1.50	1.65	7, 8, 10
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 0 6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220WEED-2 Issue C, except for the E2 and D2 MAX dimension.