ANALOG DEVICES

EVAL-ADuM4137EBZ User Guide
UG-1438

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Evaluating the ADuM4137 *i*Coupler®, High Voltage Isolated IGBT Gate Driver with Fault Detection

FEATURES

- 6 A peak drive output capability
- Output power device resistance: <1 Ω
- Test infrastructure for
  - SPI communication
  - Miller clamp
  - Desaturation detection
  - Two overcurrent protection pins
  - Two temperature sensor pins
  - Fault reporting
  - Two dummy loads

EVALUATION KIT CONTENTS

- EVAL-ADuM4137EBZ board

EQUIPMENT NEEDED

- Two variable power supplies up to 25 V and up to 1 A
- USB-SDP-CABLEZ required for SPI communication
- Signal generator

SUPPORTED *i*COUPLER MODELS

- ADuM4137

DOCUMENTS NEEDED

- ADuM4137 data sheet

SOFTWARE NEEDED

- ADuM4137 evaluation software

GENERAL DESCRIPTION

The EVAL-ADuM4137EBZ board demonstrates the advanced features of the ADuM4137 while maintaining flexibility in a testing environment. The EVAL-ADuM4137EBZ board layout delivers a circuit that is easy to manipulate via jumper pins. A more optimized layout is possible and increases the performance of the system.

The EVAL-ADuM4137EBZ board works with the USB-SDP-CABLEZ programming cable to access the secondary side electronically erasable programmable read only memory (EEPROM) and includes the option to drive the serial peripheral interface (SPI) bus with any other SPI compatible system. The USB-SDP-CABLEZ operates with a 3.3 V logic supply, while the ADuM4137 has an internal 5 V regulator. A resistor divider on the MISO line is included in the R21 and R22 resistors to allow interfacing.

This guide demonstrates how to use the ADuM4137 evaluation software for accessing the user trim bits and explains how to simulate EEPROM settings and program bits into nonvolatile memory.

For full details on the ADuM4137, see the ADuM4137 data sheet, which should be consulted in conjunction with this user guide when using this evaluation board.

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REVISION HISTORY

2/2019—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

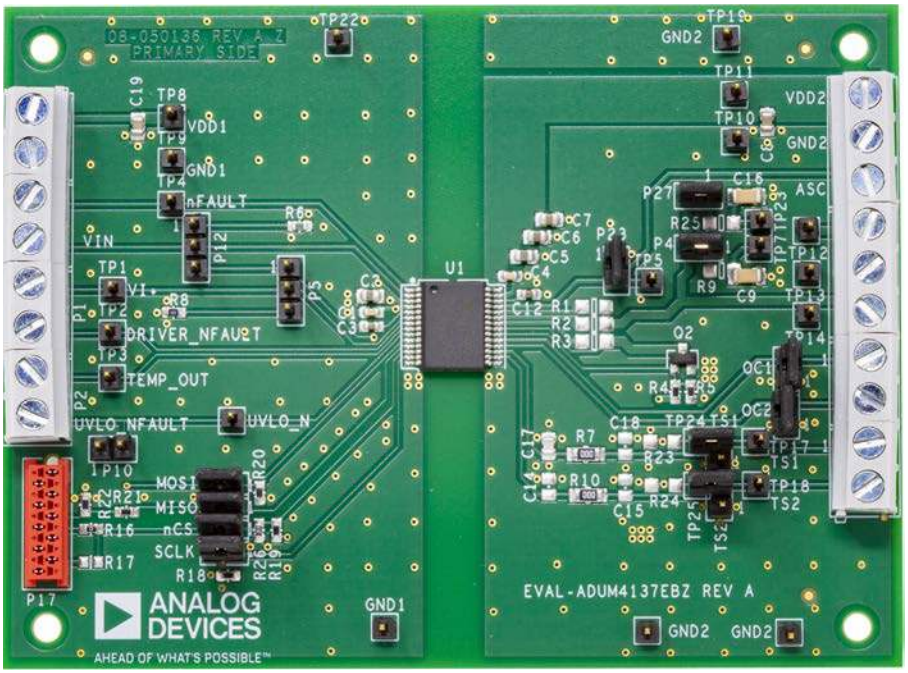

Figure 1.

CONFIGURING THE BOARD

The EVAL-ADuM4137EBZ board requires some modifications to enable the evaluation of the VI+ pin to gate operation. The board requires the following component settings:

- R1: turn on resistor, 2 Ω suggested
- R2: turn off resistor, 1 Ω suggested
- R3: soft off resistor, 1 kΩ suggested
- R9, R25: load resistors, 1 Ω suggested (optional)
- R23, R24 : temperature sense simulation resistors, 2 kΩ suggested (optional)

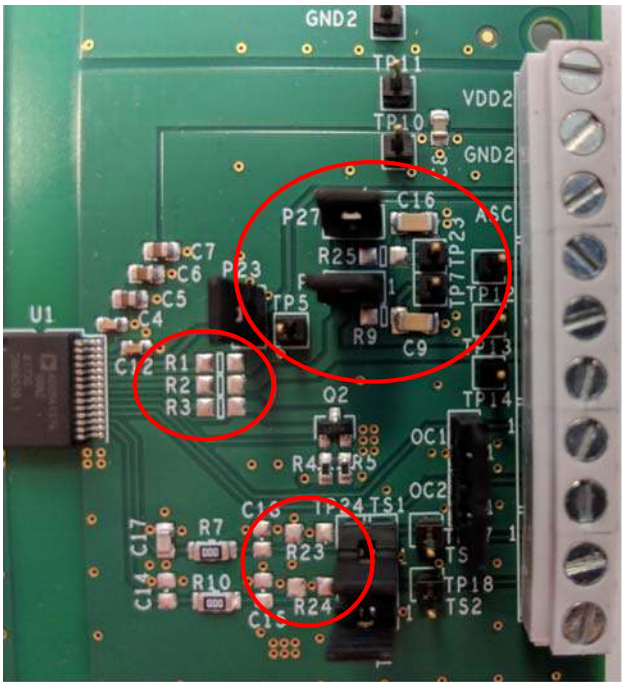

Figure 2. Stock Configuration Without Suggested Components

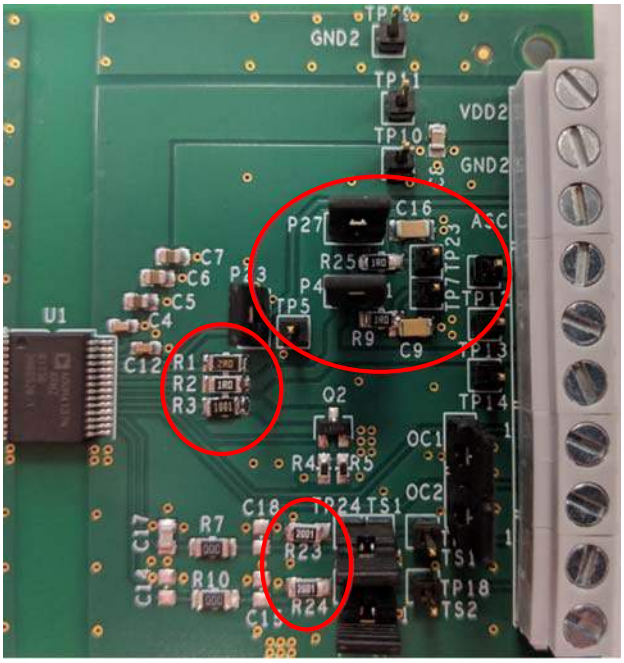

Figure 3. EVAL-ADuM4137EBZ Board with Suggested Components Placed

SIMULATED LOAD

In the stock configuration, two parallel resistor, capacitor (RC) loads, a 1 Ω (suggested) resistor (R9 or R25) in series with a 100 nF capacitor (C9 or C16), can be jumped in via Jumper P4 and/or Jumper P27.

Removing the P4 and P27 jumpers removes the RC load. Screw terminals are provided on the EVAL-ADuM4137EBZ board as an alternate method to connect other loads to the ADuM4137. Terminal TP7 and Terminal TP23 provide convenient test points that show the simulated internal gate connection within an insulated gate bipolar transistor (IGBT) module. The IGBT module has integrated series gate resistor pads, R9 and R25. By jumping the P4 or P27 jumpers, a single RC load can remain.

POWER CONNECTIONS

The ADuM4137 is an isolated gate driver, and there are two different isolation regions on the device. The left side of the IC (Pin 1 to Pin 14) is referred to as the primary side. The right side of the IC (Pin 15 to Pin 28) is referred to as the secondary side. The primary side is powered by the VDD1 pin and the GND1 pin. The primary side controls the input logic, SPI communications, and fault reporting. Voltages between 4.5 V and 25 V are recommended for the VDD1 pin to the GND1 pin. The secondary side voltage controls the output side of the ADuM4137. The voltage from the VDD2 pin to the GND2 pin controls the voltage swing seen at the driven power device. The VDD2 pin to GND2 pin voltages are recommended to be between 6 V and 25 V, with 15 V being a normal target for IGBTs.

The ADuM4137 operates whether the primary and secondary power supplies share a common ground or not. DC current limits of approximately 1 A are also recommended for up to 20 kHz operation, although lower current limits are acceptable.

INPUT AND OUTPUT CONNECTIONS

Drive the VI+ pin with any 5 V logic or 3.3 V logic, push pull complementary metal-oxide semiconductor (CMOS) connection or with an adequate open-drain configuration if the correct pull-up resistor is used. When a jumper is in P5 from Pin 2 to Pin 3 when the VI+ pin is driven with a 50 Ω load capable source, the 50 Ω load is connected. Register R8 is a 0603 surface mount device (SMD) resistor that allows 50 Ω termination.

P12 provides jumper access to the VI− pin. Placing a jumper in P12 from Pin 1 to Pin 2 terminates the VI− pin with a 50 Ω load. Placing a jumper in P12 from Pin 2 to Pin 3 pulls the VI− pin to VDD1. If there is no jumper in P12, the VI− pin is high impedance, and the provided screw terminal goes directly to the VI− pin.

When a 50 Ω termination is not used, do not drive the VI+ pin by a high-Z signal. When the VI+ pin is not driven, bring it to a safe state by jumping Pin 2 and Pin 3 of Jumper P5, which shorts the VI+ pin to the GND1 pin through the 50 Ω resistor. When no 50 Ω termination is used, drive the VI+ pin high by jumping Pin 1 and Pin 2 of Jumper P5.

USING SPI

The EVAL-ADuM4137EBZ evaluation board interfaces easily with the USB-SDP-CABLEZ cable. When using the SPI bus, place jumpers on the MOSI, MISO, NCS, and SCLK jumper pins. Connect the USB-SDP-CABLEZ to Jumper P17. The EVAL-ADuM4137EBZ evaluation board has an indexing hole to ensure proper polarity. P10 is provided to allow the placing of a jumper to ground UVLO_nFault. To communicate to the ADuM4137 via the SPI, UVLO_nFault must be grounded.

Test any other SPI system on the EVAL-ADuM4137EBZ board by connecting cables to the right side of the MOSI, MISO, NCS, and SCLK jumpers. The pins of the EVAL-ADuM4137EBZ board are labeled on the silkscreen.

When programming, it is recommended to have Pin 2 and Pin 3 of Jumper P5 shorted to prevent the VI+ pin from affecting the transfer of the gate drive signal. This configuration shorts the VI+ pin to the GND1 pin.

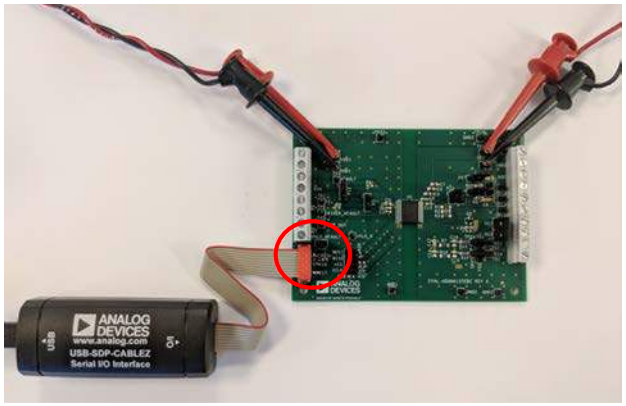

Figure 4. EVAL-ADuM4137EBZ Board with USB-SDP-CABLEZ Connected

STOCK CONFIGURATION FAULT OVERIDES

The EVAL-ADuM4137EBZ board comes configured with fault mode overrides that normally do not exist in the application to present a simplified test platform. Remove these overrides to evaluate the fault modes or leave the overrides on the EVAL-ADuM4137EBZ board to disable the fault condition and focus on other parts of the IC.

ASC Override

Jumping P23 shorts the ASC pin to the GND2 pin, which blocks the ASC from occurring. Remove the jumper on P23 to allow the ASC to be driven high by an external voltage source. When evaluating the ASC pin, remove the default jumper on P23 to change the ASC pin voltage.

Over Current Fault Overrides

The OC1 and OC2 jumper pins provide a simple method for tying the overcurrent pins to the GND2 pin. This method removes the possibility of an overcurrent fault stopping the output drive. When testing overcurrent capabilities of the ADuM4137, remove the default jumpers on the OC1 and OC2 jumper pins.

Temperature Sense Fault Override

Without remote temperature sensing resistors in place, the TS1 and TS2 pins float high, which produces a low temperature operation mode, as shown in Figure 5. To create a middle range voltage on the temperature sense pins, resistors are provided connected to the TP24 and TP25 pins. Jumping from TP24 to Pin 2 of the TS1 jumper pins simulates a midrange temperature simulation on TS1. Jumping from TP25 to Pin 2 of the TS2 jumper pins simulates a midrange temperature on TS2, as shown in Figure 6. To simulate a high temperature reading on the TSx pins, jump the TS1 jumper pins and/or the TS2 jumper pins to ground the TS1 and/or TS2 pins, resulting in a high temperature reading at the ADuM4137 remote temperature sensing pins, as shown in Figure 7.

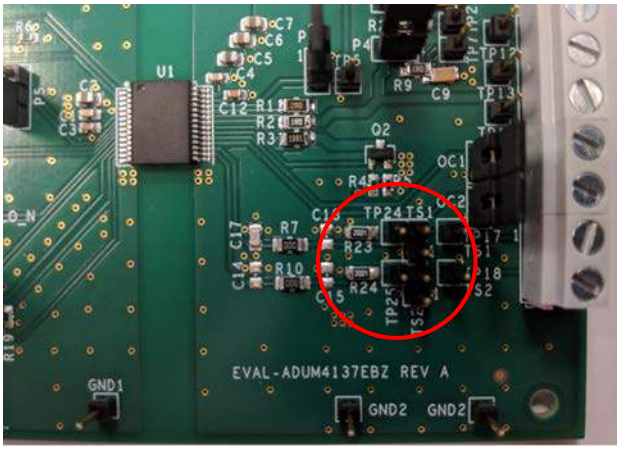

Figure 5. TS1 and TS2 Pins Floating High with Low Temperature Simulation

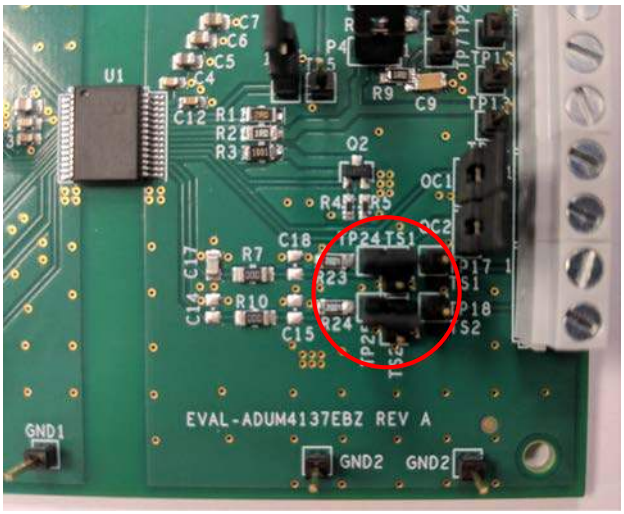

Figure 6. Midrange Temperature Sense Jumper Configuration

Figure 7. TS1 and TS2 Pins Jumped Low with High Temperature Simulation

EXAMPLE PROPAGATION DELAY TESTING

Perform an example propagation delay testing from a stock configuration. Figure 8 shows one possible configuration. The VI+ pin is driven via a 5 V, push pull CMOS driver referenced to the GND1 pin. The VDD1 pin is fed with 12 V referenced to the GND1 pin. The VDD2 pin is fed with 15 V referenced to the GND2 pin. The E screw terminal is the emitter connection of the secondary side, which is also the GND2 pin. For this configuration, remove the USB-SDP-CABLEZ, as well as the MOSI, MISO, NCS, and SCLK jumper pins. When an SPI transmission occurs when the VI+ pin is brought high, the output is blocked. It is possible to perform the test with the USB-SDP-CABLEZ connected to the ADuM4137.

Measuring TP7 and/or TP23 test points simulates what an IGBT with a 1 Ω (suggested) internal series gate resistance sees at the gate.

Do not allow the VI+ pin to be driven by a high-Z signal, which happens on some function generator models when the output off button is pressed. When the function generator being used has a high-Z when turned off, leave Pin 2 to Pin 3 of Jumper P5 jumpered by placing a 50 Ω terminating resistor, R8, between the VI+ pin and the GND1 pin.

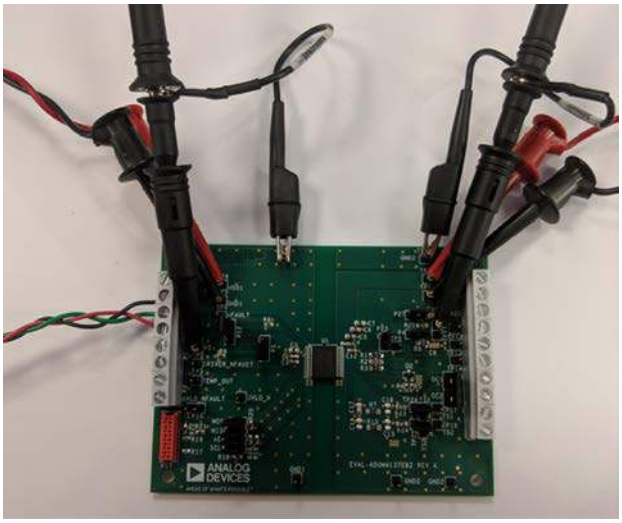

Figure 8. Example Propagation Delay Test Setup

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURE

To use the USB-SDP-CABLEZ for SPI communication, a LabVIEW® executable is available. The LabVIEW executable requires installed USB-SDP-CABLEZ drivers and a LabVIEW run-time engine compatible with LabVIEW 2011.

Take the following steps to install the drivers and the LabVIEW software:

1. Install **SDPdrivers.exe**, available here.
2. Install LabVIEW Run-Time Engine 2011 or later (available from National Instruments).
3. Double click **ADuM4137_eval_progam_01.exe** to run the evaluation program.

USING THE SOFTWARE FOR TESTING

STOP

Click **STOP** in the upper right corner of the window to halt the LabVIEW® program. Alternate methods of stopping the program are to close the window or to force quit the program. All of these options set the NCS pin to an unknown state. Therefore, remove the USB-SDP-CABLEZ connection from the EVAL-ADuM4137EBZ board before shutting the program down.

Read Addr:00

Click **Read Addr:00** to see what the ADuM4137 has in the EEPROM at Register Address 00 (user bits). Clicking **Read Addr:00** sends two read commands because of the way the SPI setup operates. The second read command pushes the data loaded by the first read command to the MISO pin. The result of the second read appears in the **Addr:00 Output** box.

Read Addr:01

Click **Read Addr:01** to see what the ADuM4137 has in the EEPROM at Register Address 01 (configure bits). Clicking **Read Addr:01** sends two read commands because of the way the SPI setup operates. The second read command pushes the data loaded by the first read command to the MISO pin. The result of the second read appears in the **Addr:01 Output** box.

Read Addr:10

Click **Read Addr:10** to see what the ADuM4137 has in the EEPROM at Register Address 10 (control bits). Clicking **Read Addr:10** sends two read commands because of the way the SPI setup operates. The second read command pushes the data loaded by the first read command to the MISO pin. The result of the second read appears in the **Addr:10 Output** box.

Write/Read Addr:00

Click **Write/Read Addr:00** to perform a single write comprised of the bit pattern set by the user in the **OFFSET_2** box, the **GAIN_2** field, the **OFFSET_1** box, and the **GAIN_1** box. After the single write is performed, a single read is performed that allows the user to verify that the sequence is sent. The result of this read is sent to the **Addr:00 Output** box. When the SIM_TRIM bit at Register Address 10 is set to 1, the write affects the operation of the ADuM4137 with the new settings written by the user. The SIM_TRIM bit is set to 0 until the device is powered down, or until new settings are written.

Write/Read Addr:01

Click **Write/Read Addr:01** to perform a single write comprised of the bit pattern set by the user in the **OT_Fault_OP** box, the **OT_Fault_Sel** box, the **OC_TIME_OP** box, **OC_2Lev_OP** box, the **Low_T_OP** box, the **OC_Blank_OP** box, the **tBLANK** box, the **ECC_OFF_OP** box, the **T_Ramp_OP** box, and the **PWM_OSC** box. After the single write is performed, a single read is performed that allows the user to verify that the sequence is sent. The result of this read is sent to the **Addr:01 Output** box. When the SIM_TRIM bit at Register Address 10 is set to 1, the write affects the operation of the ADuM4137 with the new settings written by the user. The SIM_TRIM bit is set to 0 until the device is powered down, or until new settings are written.

Write/Read Addr:10

Click **Write/Read Addr:10** to perform a single write comprised of the bit pattern set by the user in the **Prog_Busy** box and the **Sim_Trim** box. After the single write is performed, a single read is performed that allows the user to verify that the sequence is sent. The result of this read is sent to the **Addr:10 Output** box. When the SIM_TRIM and PROG_BUSY bits are both set to 1, values written to the ADuM4137 using **Write/Read Addr:00** and **Write/Read Addr:01** are written to EEPROM and are loaded on the next power up. Verify these with an address read after a power up.

sclkFrequency

This field is used to change the operating frequency of the SPI clocking. The field is set in Hz. The default is 200 kHz maximum value.

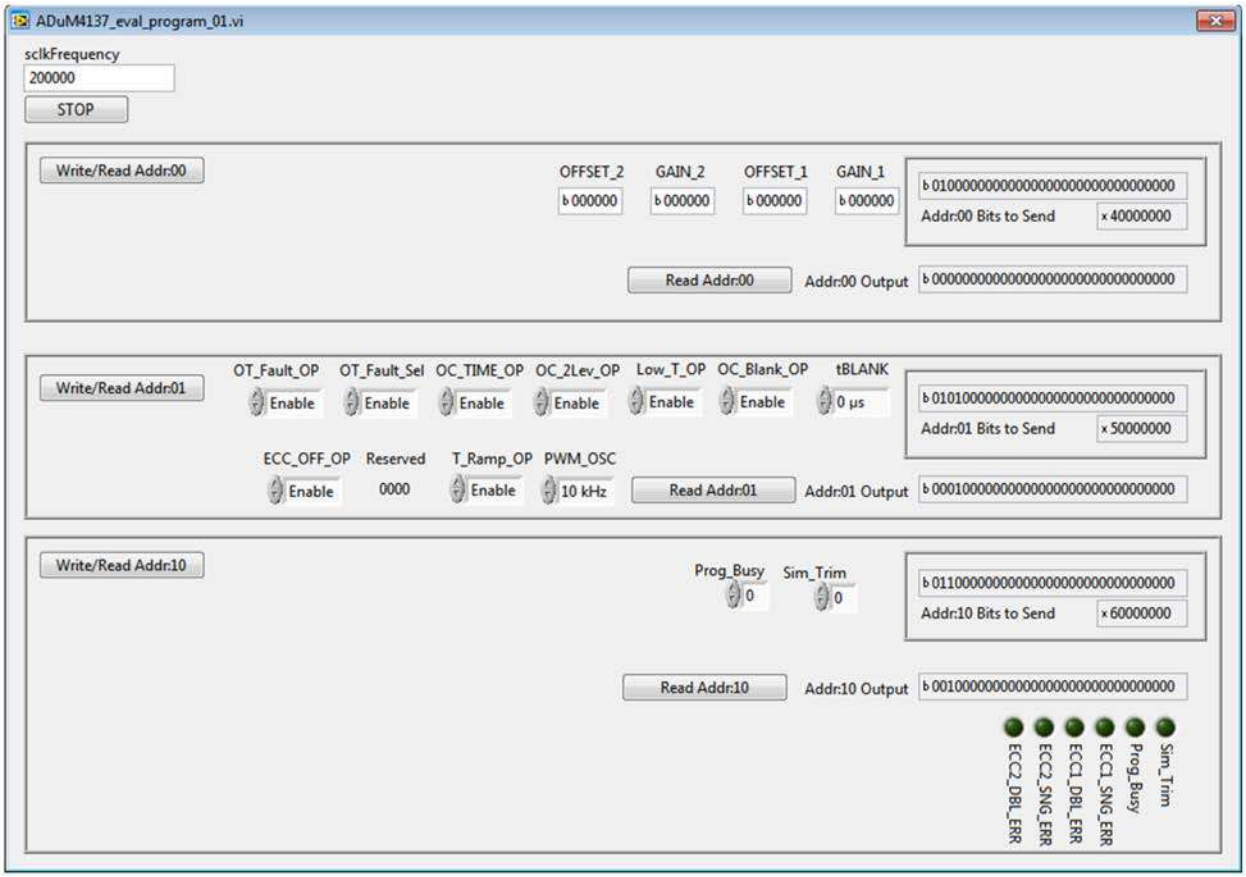

Figure 9. Evaluation Software Screenshot

EVALUATION SOFTWARE EXAMPLE OPERATION

WHEN ADUM4137 IS NOT COMMUNICATING

When the ADuM4137 is not powered, and the USB-SDP-CABLEZ is plugged into the EVAL-ADuM4137EBZ board, all read commands usually report 0. By reading all registers, it is possible to see if the ADuM4137 is communicating properly as the address bits display on a read command. With default settings, the FLYBACK_V setting is 111 (see Figure 10).

EXAMPLE READ COMMANDS

To perform a read command, power up the ADuM4137 with the VDD1 to GND1 pins between 4.5 V and 25 V, and the VDD2 to GND2 pins between 12 V and 25 V. Click the read button of the desired address to be read. If the ADuM4137 EEPROM has never been programmed, expect all 0s to be returned except the address. Figure 11 shows **Read Addr:00**, **Read Addr:01**, and **Read Addr:10** clicked on an ADuM4137 that has never been programmed.

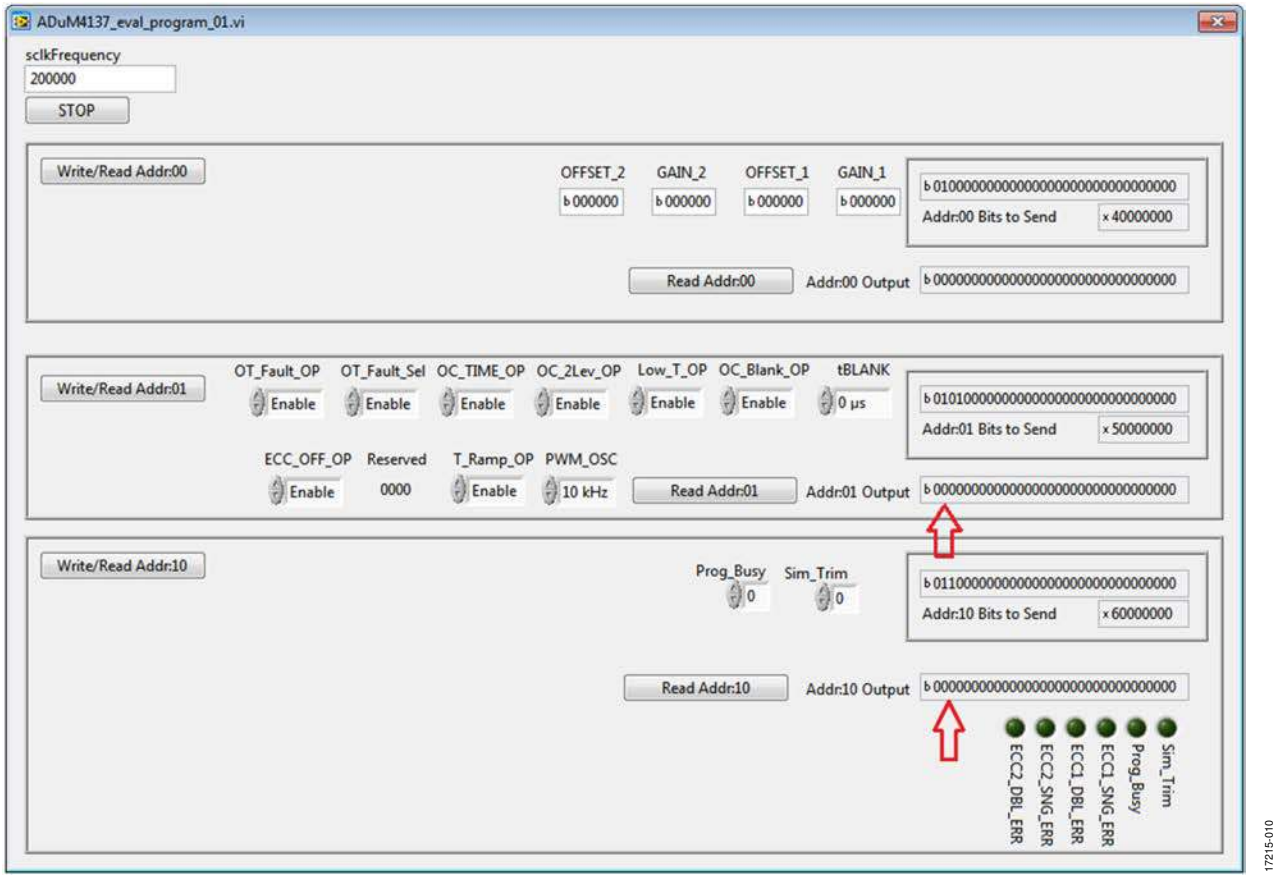

Figure 10. All Zeros Show Communication Not Occurring

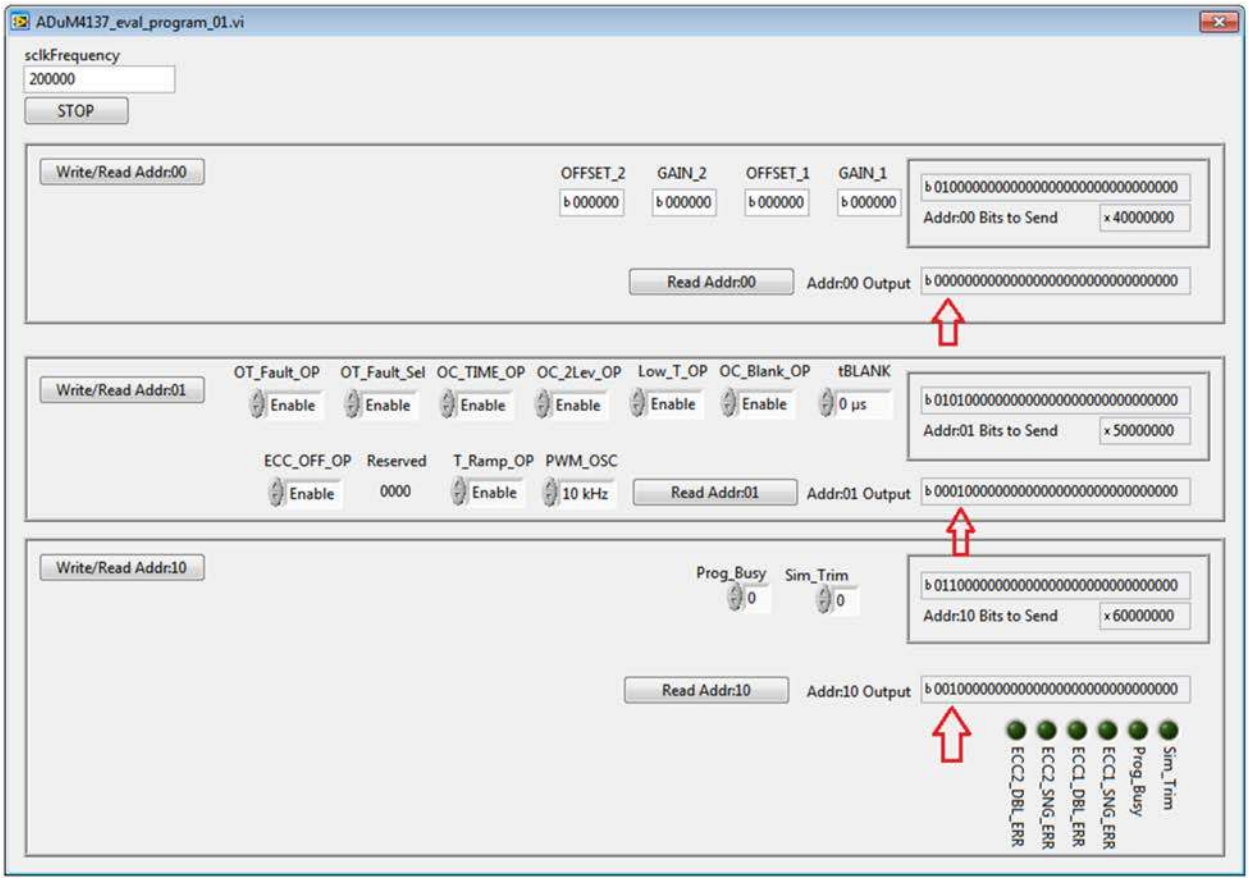

Figure 11. Address Bits Read Back

EXAMPLE EEPROM WRITE

Writing Data to the EEPROM

To write data to the EEPROM, take the following steps:

1. Set the SIM_TRIM bit by typing 1 in the **Sim_Trim** box, and click **Write/Read Addr:10**. This setting results in the green **Sim_Trim** indicator lighting up (see Figure 12). When the SIM_TRIM bit is set to 1, the write commands to Register Address 00 or Register Address 01 affect the operation of the ADuM4137.
2. Set the desired bits in Register Address 00 and Register Address 01. In this example, Bit 0 of the **GAIN_1** box is set to 1.
3. Click **Write/Read Addr:00**. This command allows the **Addr:00 Output** box to show that the value was written to the register. At this time, the GAIN_1 EEPROM register is not yet programmed. Note that the **Sim_Trim** box value still reads 1 (see Figure 13).

Writing Address 00 Data to the EEPROM

To write Address 00 data to the EEPROM, take the following steps:

1. Set the **Prog_Busy** field to 1 and then click **Write/Read Addr:10** (see Figure 14). The **Write/Read Addr:10** button performs a write, and then performs a read. The **Prog_Busy** green indicator lights up because the read command occurs quickly after the write, and the PROG_BUSY bit in the ADuM4137 is 1 while the device is being programmed.
2. After this programming, click **Read Addr:10**. Once the PROG_BUSY bit changes to 0, the EEPROM is programmed. The programming takes approximately 10 µs. Therefore, a user generally cannot click the read button fast enough to see 1 in the **Prog_Busy** box the second time, but an automated program can (see Figure 15).

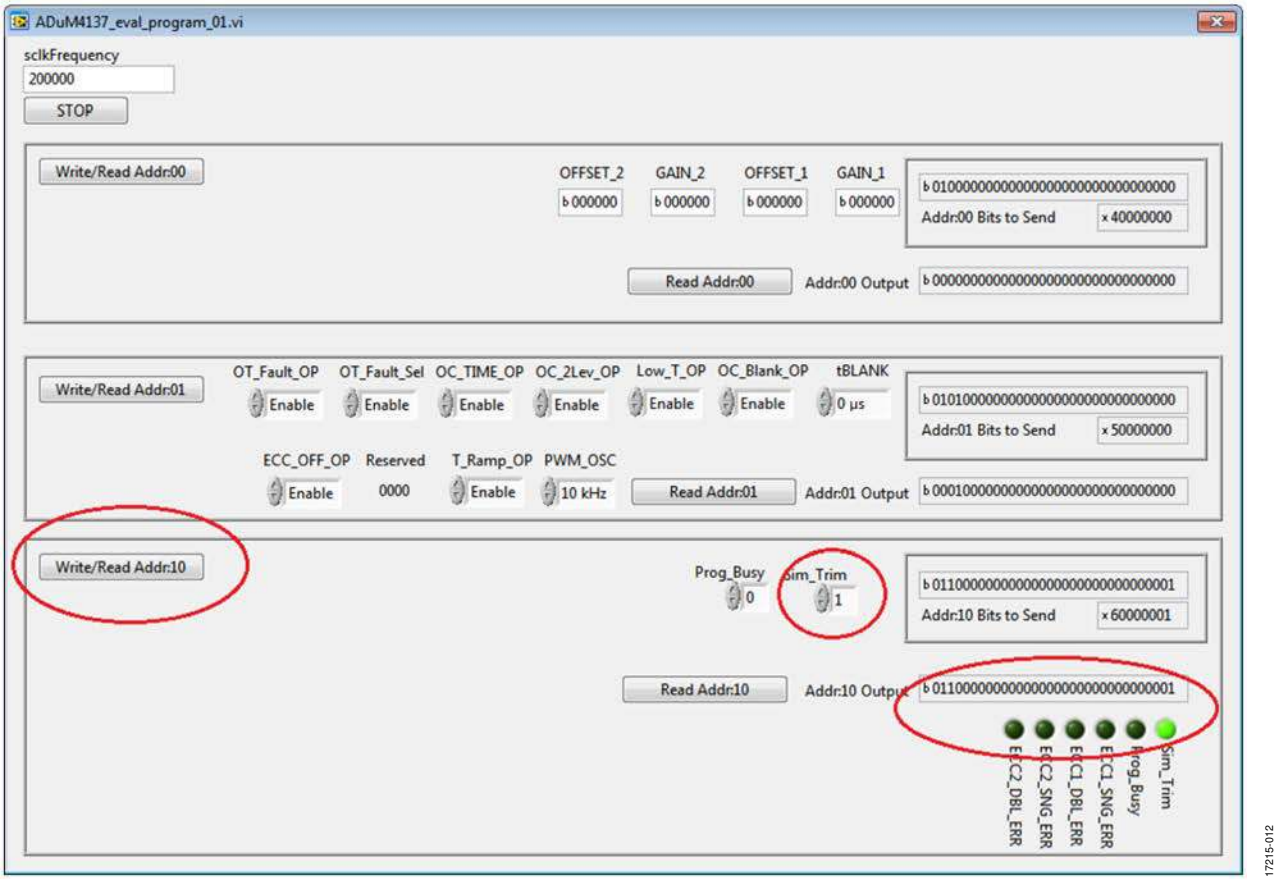

Figure 12. Setting the SIM_TRIM Bit

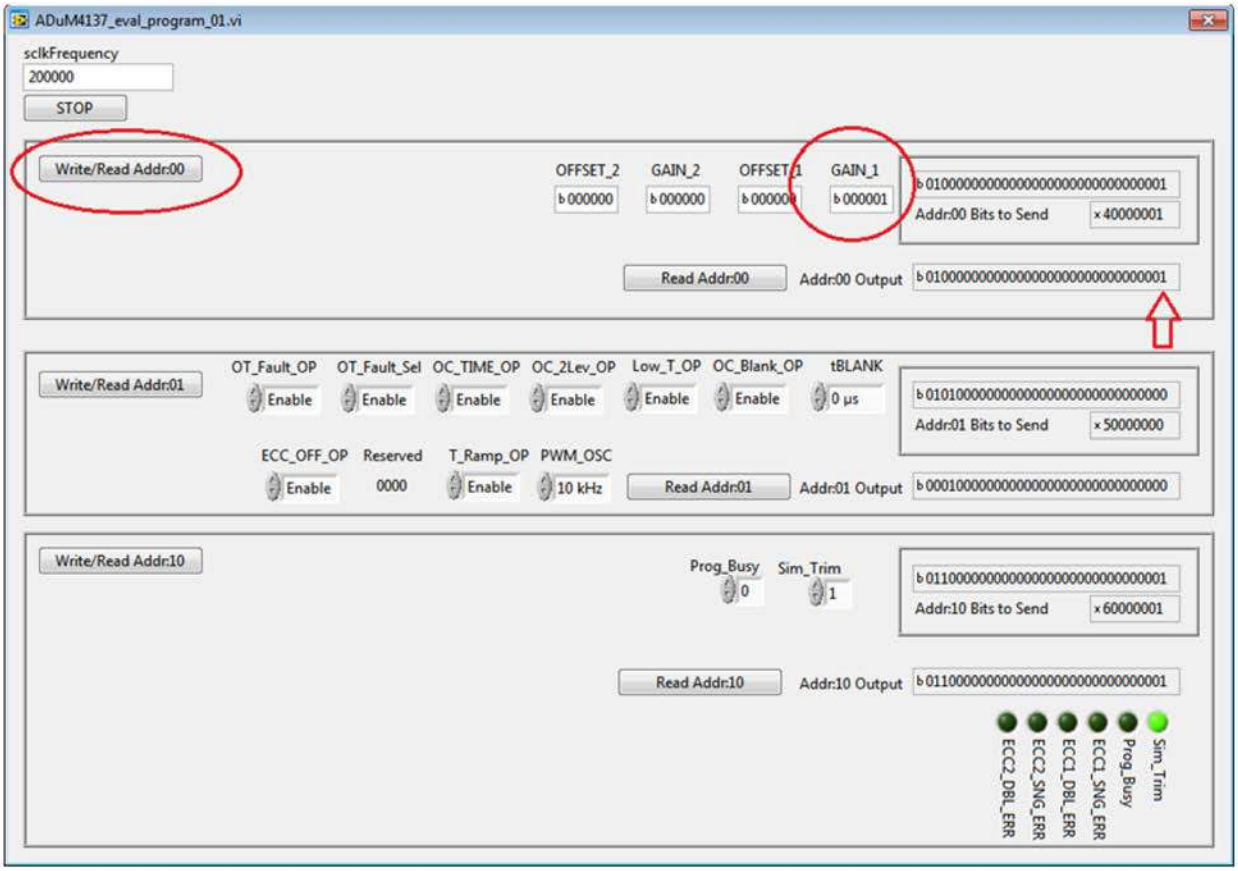

Figure 13. Writing Example Register Edit

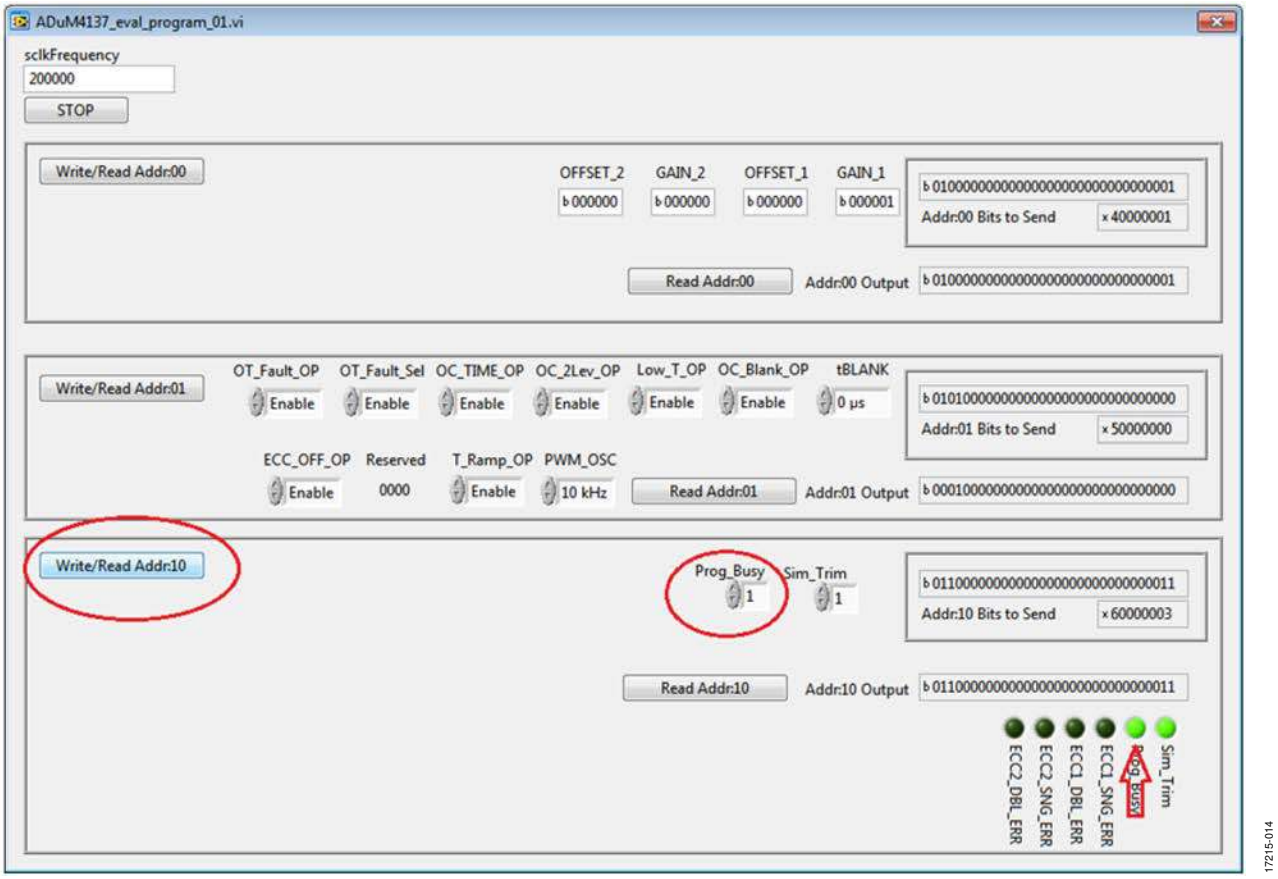

Figure 14. Programming the EEPROM

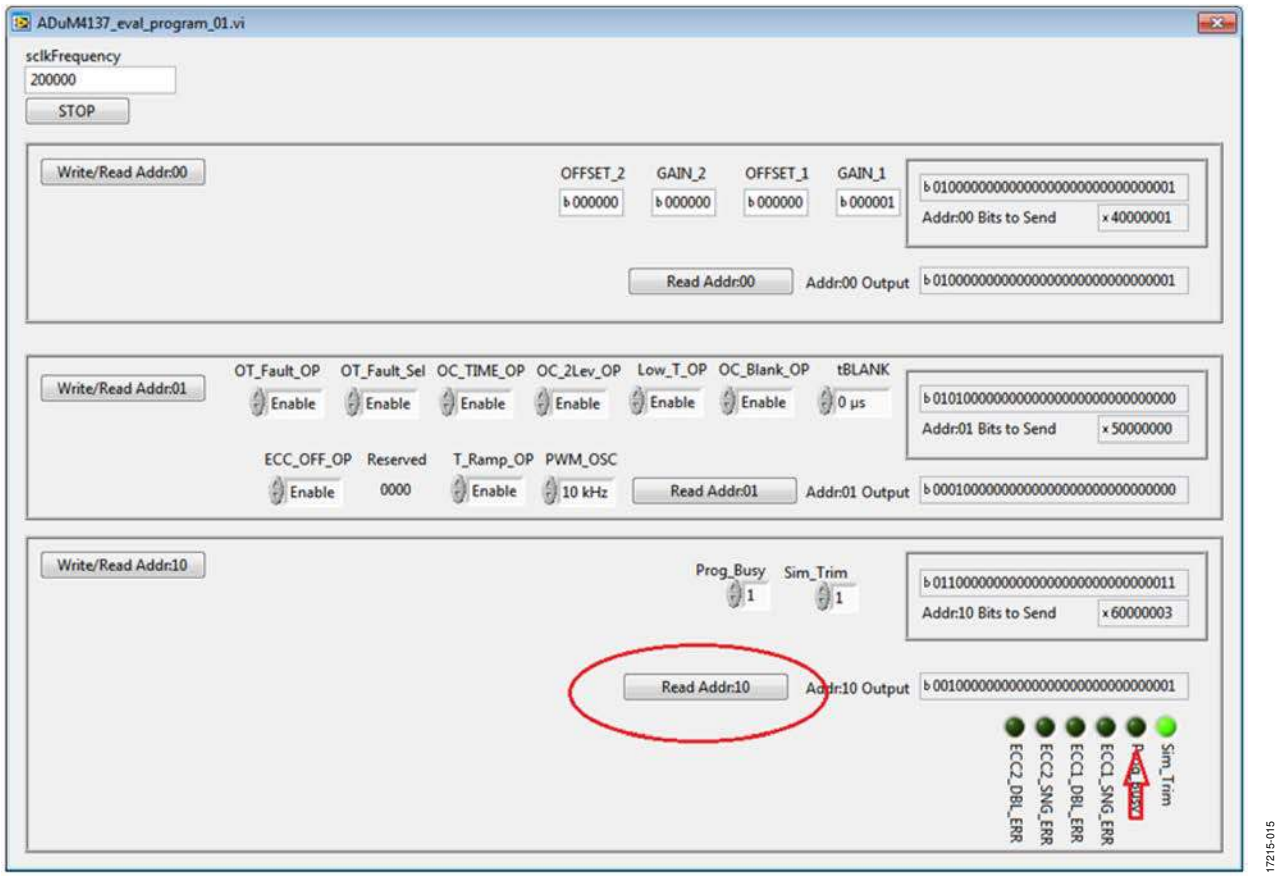

Figure 15. ADuM4137 Showing Programming Complete

After the **Prog_Busy** box reads 0, the EEPROM programming is complete. Power down the ADuM4137 and click **Read Addr:00** to verify the programming. Expect to receive all 0s back because the ADuM4137 is unpowered. This read allows the next read to be easier to see. It is not necessary to click the other read buttons. Figure 16 shows all read buttons clicked while the ADuM4137 is off.

Power up the ADuM4137 and click all read buttons. Bit 0 of GAIN_1 survives the power-up, indicating that the EEPROM is programmed. Perform the same steps with the **GAIN_1** box set to 0 to return the EEPROM to the original programmed state (see Figure 17).

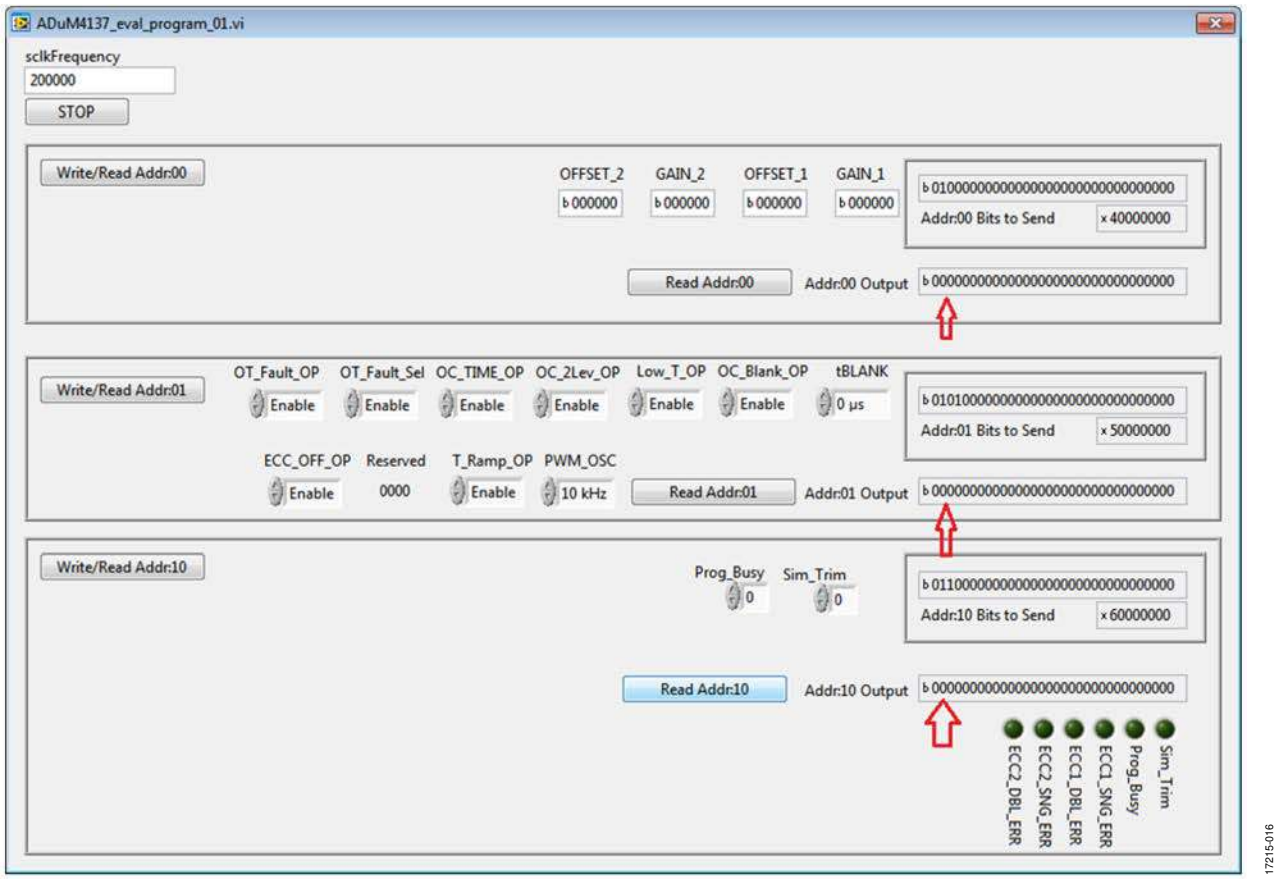

Figure 16. Unpowered Reads

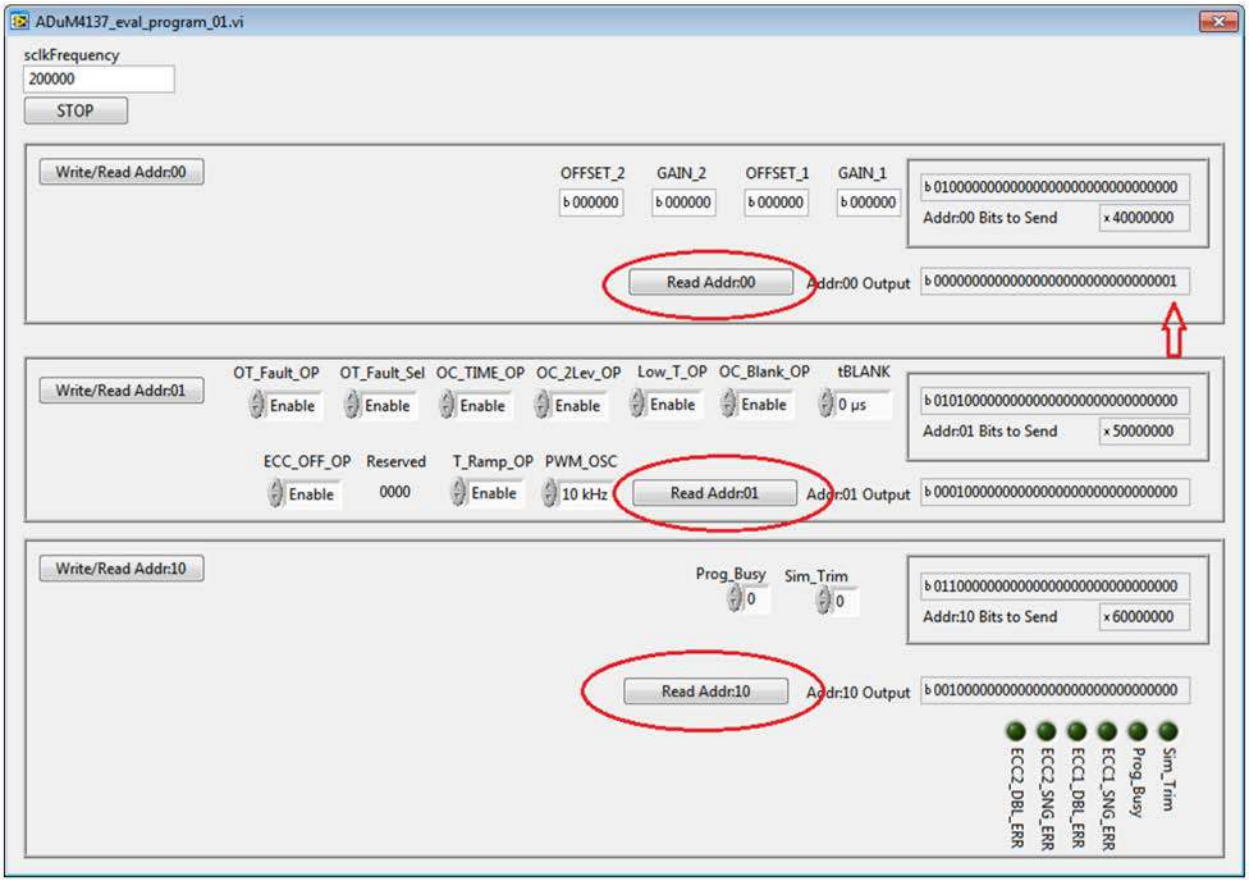

Figure 17. EEPROM Successfully Written

EVALUATION BOARD SCHEMATIC

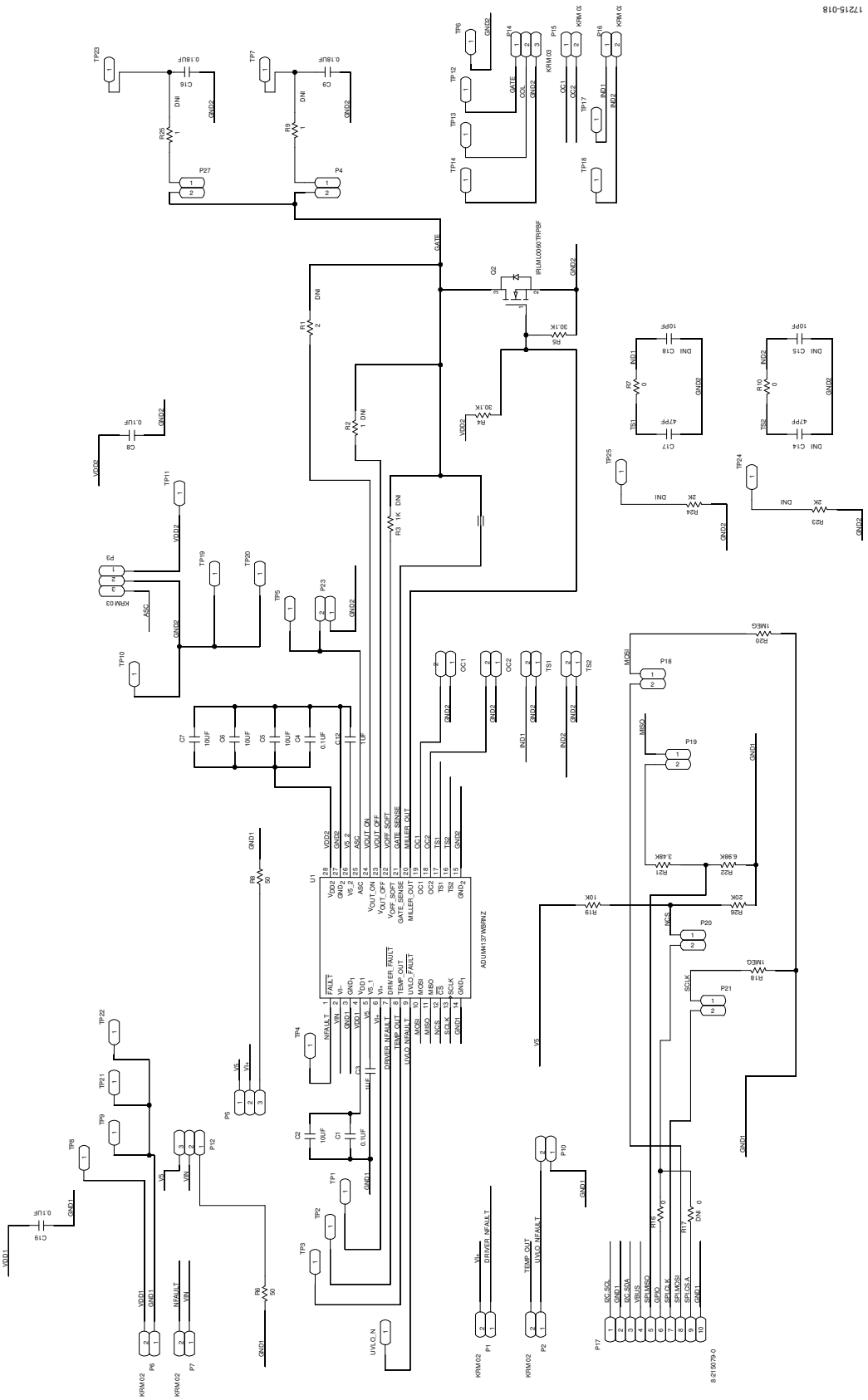

Figure 18. EVAL-ADuM4137EBZ Circuit Schematic

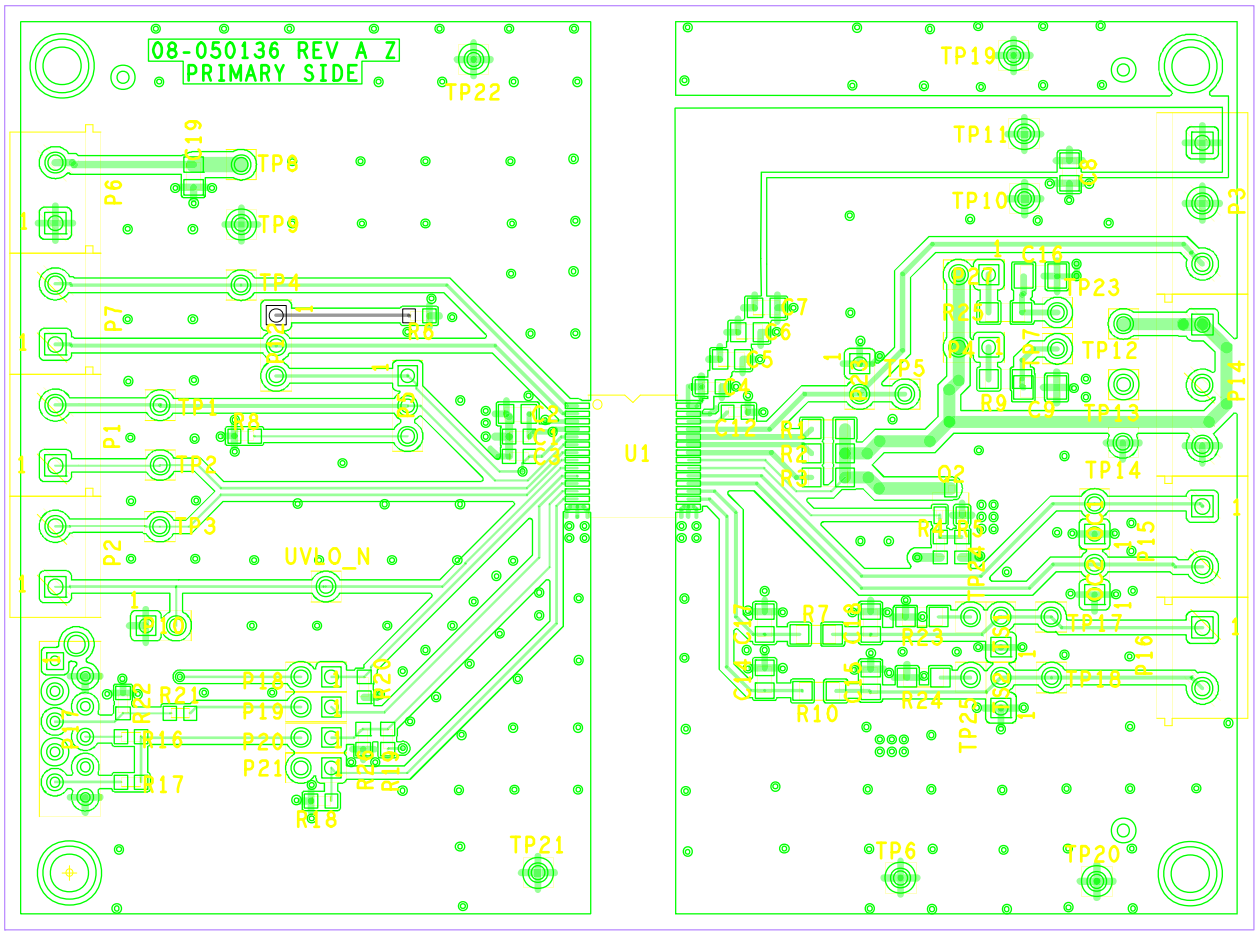

Figure 19. Evaluation Board Layout Top Layer

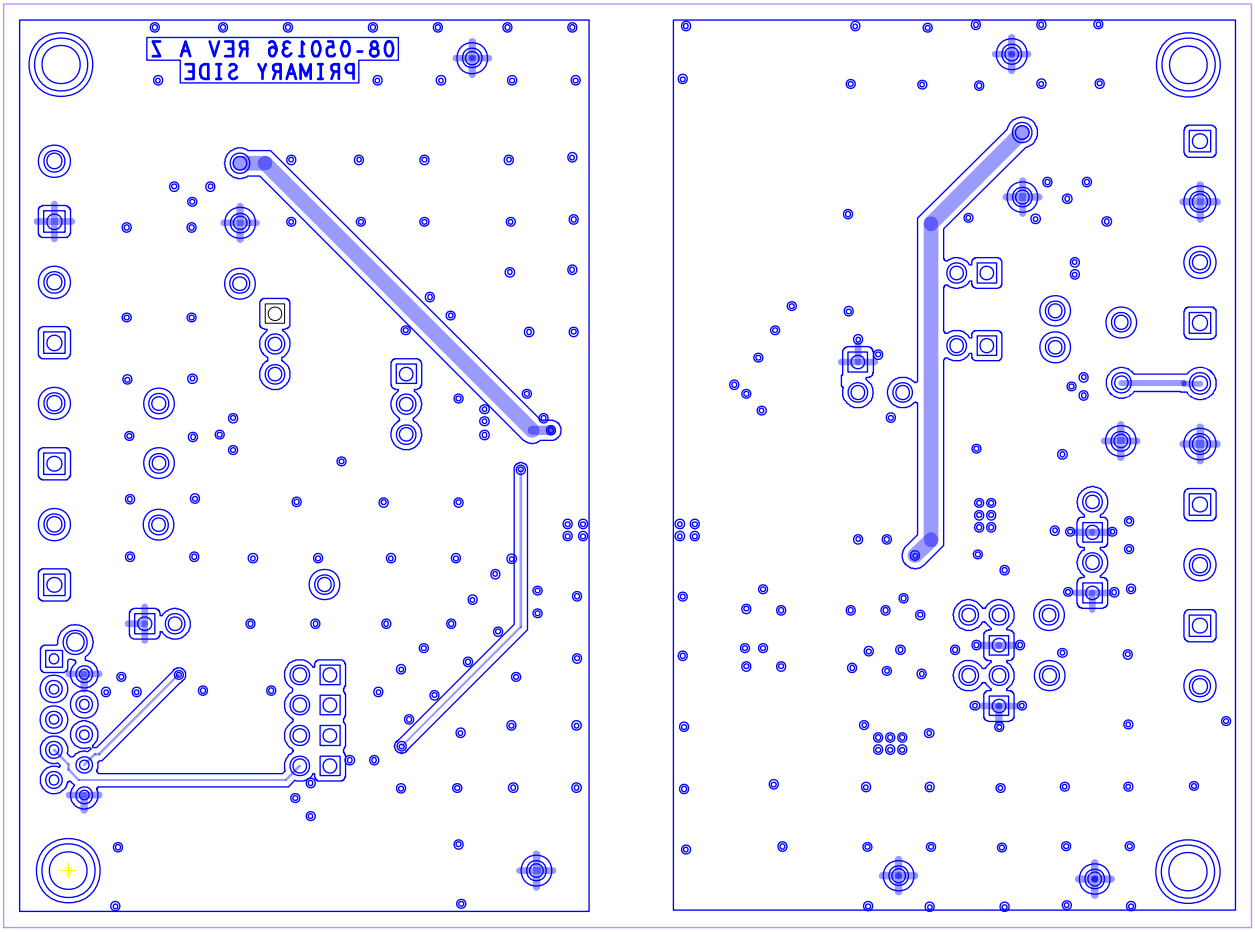

Figure 20. Evaluation Board Layout Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 1. Bill of Materials

Reference Designator	Description	Part Number	Manufacturer
U1	ADuM4137 isolated gate driver	ADuM4137WBRNZ	Analog Devices, Inc.
C1, C4	0.1 µF, X7R, ceramic capacitors, 50 V, 0603	06035C104J4Z2A	AVX Corporation
C3, C12	1 µF, X7R, ceramic capacitors, 10 V, 0603	C0603C105K8RACTU	Kemet
C9, C16	180 nF, X7R, ceramic capacitors, 50 V, 1206	12065C184JAT2A	AVX Corporation
C17	47 pF, NP0, ceramic capacitor, 100 V, 0805	08051A470JAT2A	AVX Corporation
C8, C19	0.1 µF, X7R, ceramic capacitors, 50 V, 0805	C0805C104J5RACTU	Kemet
C2, C5 to C7	10 µF, X5R, ceramic capacitors, 25 V, 0805	GRM21BR61E106KA73L	Murata
P17	10-pin system demonstration platform (SDP)	8-215079-0	TE Connectivity, LTD
P17 (Alternate)	WR-MM female connector	690367181072	Wurth Electronics
Q2	HEXFET power MOSFET, 60 V, SOT23	IRLML0060TRPBF	Infineon Technologies
R7, R10	0 Ω resistors, 1206	ERJ-8GEY0R00V	Panasonic
R16	0 Ω resistor, 0603	ERJ-3GEY0R00V	Panasonic
R18, R20	1 MΩ resistors, 0603	ERJ-3EKF1004V	Panasonic
R19	10 kΩ resistor, 0603	ERJ-3EKF1002V	Panasonic
R21	3.48 kΩ resistor, 0603	ERJ-3EKF3481V	Panasonic
R22	6.98 kΩ resistor, 0603	ERJ-3EKF6981V	Panasonic
R26	20 kΩ resistor, 0603	ERJ-3GEYJ203V	Panasonic
R4, R5	30.1 kΩ resistors, 0603	ERJ-3EKF3012V	Panasonic
R6	50 Ω resistor, 0603	FC0603E50R0BST1	Vishay Intertechnology, Inc.
R8	50 Ω resistor, 0603	CRCW060350R0FKEA	Vishay Intertechnology, Inc.
C14, C15, C18, R9, R17, R23 to R25	Not installed	Not applicable	Not applicable
R1	Not installed (2 Ω, 1206 recommended)	Not applicable	Not applicable
R2	Not installed (1 Ω, 1206 recommended)	Not applicable	Not applicable
R3	Not installed (1 kΩ, 1206 recommended)	Not applicable	Not applicable
OC1, OC2, P4, P10, P18 to P21, P23, P27, TS1, TS2	2 position male headers, 2.54 mm spacing	TSW-102-07-G-S	Samtec, Inc
P1, P2, P6, P7, P15, P16	2 position terminal blocks, 5 mm spacing	KRM 02	Lumberg
P5, P12	3 position male headers, 2.54 mm spacing	TSW-103-23-F-S	Samtec, Inc
P3, P14	3 position terminal block, 5 mm spacing	KRM 03	Lumberg
11 (Supplied)	2-pin shunt jumper	NPC02SXON-RC	Sullins

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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