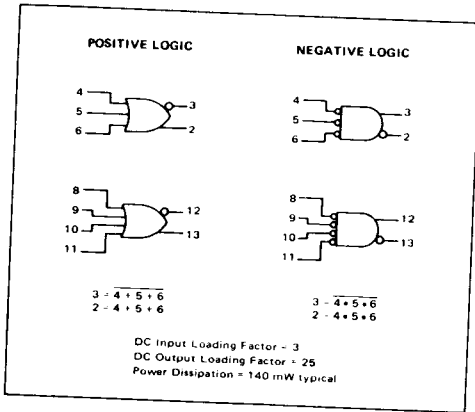


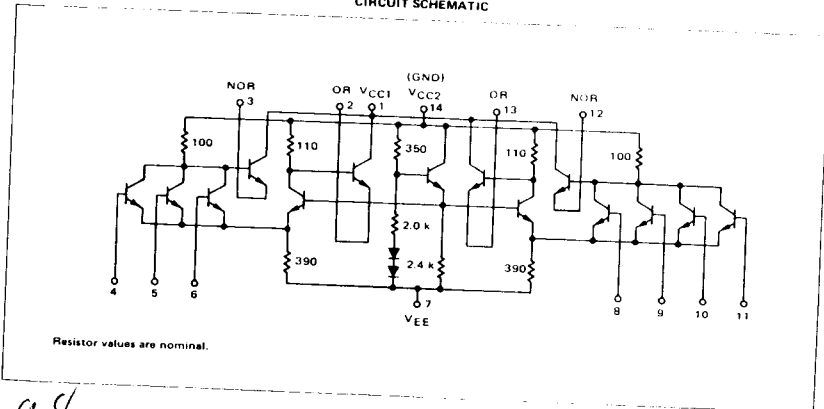
MC1026
MC1226

Provides simultaneous OR/NOR or AND/NAND output functions. It contains an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

This circuit is designed to operate in high-speed digital computer applications as a 50-ohm transmission line driver, as a clock driver, or as a high speed gate.



CIRCUIT SCHEMATIC



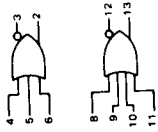
MC1026, MC1226 (continued)

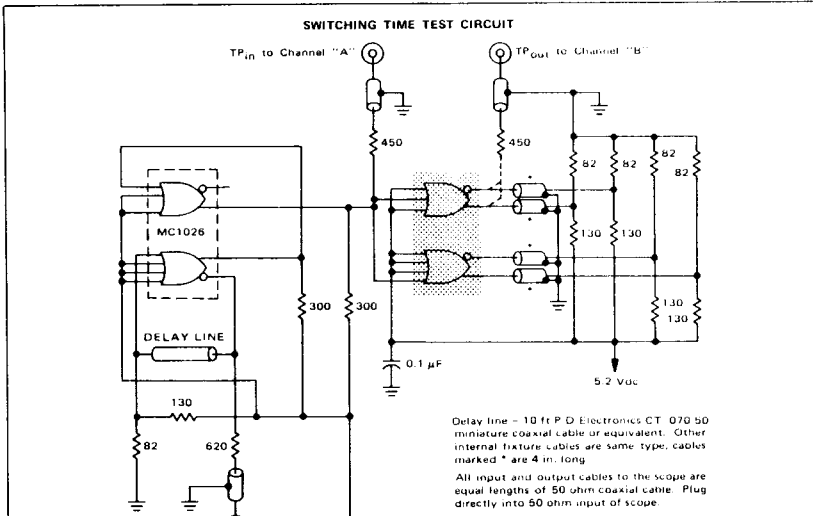
ELECTRICAL CHARACTERISTICS

Test is shown for only one gate. The other gates is tested in a similar manner.

Characteristic	Pin Under Test	MC1226 Test Limits						MC1026 Test Limits						TEST VOLTAGE / CURRENT APPLIED TO PINS LISTED BELOW:												V_{CC} (Gnd)											
		-55°C		+25°C		+125°C		0°C		+25°C		+75°C		V_R	V_{IH}	V_{OL}	V_{IH}	V_{OH}	V_{OL}	V_{IH}	V_{OH}	V_{OL}	V_{IH}	V_{OH}	V_{OL}		V_{IH}	V_{OH}	V_{OL}								
Power Supply Drain Current	I _E																																				
Input Current	I _{in}																																				
Input Leakage Current	I _L																																				
"NOR" Logical "1" Output Voltage	V _{OH1}																																				
"NOR" Logical "0" Output Voltage	V _{OL}																																				
"OR" Logical "1" Output Voltage	V _{OH2}																																				
"OR" Logical "0" Output Voltage	V _{OL}																																				
Switching Times**																																					
Propagation Delay (Fan-Out=2)†	t _{pd3+}																																				
	t _{pd3+}																																				
	t _{pd2+}																																				
	t _{pd2+}																																				
Rise Time (Fan-Out=2)	t _{r3+}																																				
Fall Time (Fan-Out=2)	t _{f3+}																																				
	t _{f3+}																																				
	t _{f3+}																																				

† V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).
 ** Switching times apply from no load (0 mA) to full load (-2.5 mA).
 †† V_{OH} limits apply from no load (0 mA) to full load (-2.5 mA).
 ††† Paddown is Thevenin equivalent of 50 ohms to -2.0 V.





APPLICATIONS INFORMATION

The MC1026/MC1226 has been designed with high frequency capabilities and low output impedance for use as a high speed clock driver and for driving transmission lines in excess of 50 MHz. Characteristics are similar to those of the MC1023 clock driver, including 2.0 ns propagation delay time and 5.0 ohm output impedance. The major differences between the MC1026 and the MC1023 are:

(1) The V_{CC} supply to the output emitter followers and the V_{CC} supply to the current switches (and V_{BB} network) have been separated (shown as V_{CC1} and V_{CC2} in the circuit schematic). This separation permits the outputs of one gate to drive impedances as low as 50 ohms without observable crosstalk in the other gate due to common impedances. Because of this additional V_{CC} supply pin, one of the gates has only three inputs.

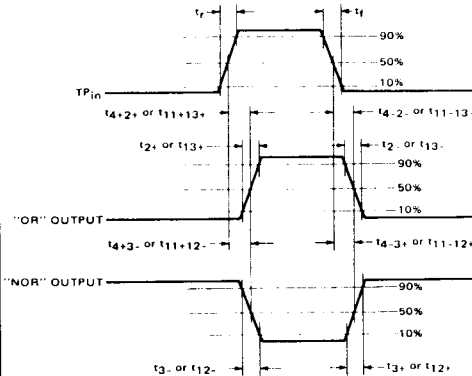
(2) The internal output emitter follower pulldown resistors have been eliminated to reduce internal power consumption, allowing operation to $+125^{\circ}C$ in present packages and permitting wired ORing of multiple outputs with use of a single external pulldown resistor.

The MC1026/MC1226 may be used for driving a 50 ohm coaxial cable as shown in Figure 1. The leads of the terminating resistors (the equivalent of 50 ohms to -2.0 volts) and the printed circuit leads from the BNC connectors to the input and output of the line driver must be kept as short as possible to reduce mismatch reflections. The V_{CC1} and V_{CC2} leads should be connected to ground at the pins.

Figures 2 and 3 show the waveforms for the circuit of Figure 1 at 50 MHz. Note that the output at "B" is slightly attenuated (with an inherent increase in rise and fall times) when compared with output "A".

Figure 4 shows the typical switching times at $25^{\circ}C$ and 20 MHz using the circuit shown in Figure 1.

PROPAGATION DELAY



MC1026, MC1226 (continued)

APPLICATIONS INFORMATION (continued)

FIGURE 1 - LINE DRIVER TEST CIRCUIT

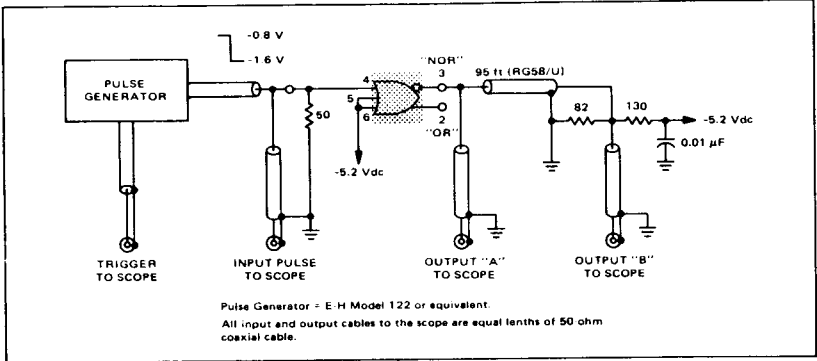


FIGURE 2 - "OR" OUTPUT WAVEFORMS

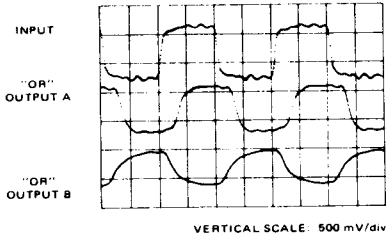


FIGURE 3 - "NOR" OUTPUT WAVEFORMS

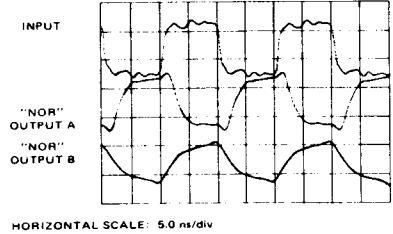


FIGURE 4 - TYPICAL SWITCHING TIMES
(Test Circuit Figure 1, $T_A = 25^\circ\text{C}$, $f = 20\text{ MHz}$)

OUTPUT A		OUTPUT B	
TEST	TIME (ns)	TEST	TIME (ns)
"OR" OUTPUT			
t_{pd++} (50% to 50%)	2.6	t_r (10% to 80%)	3.8
t_{pd-} (50% to 50%)	2.7	t_r (10% to 90%)	5.4
t_r (10% to 90%)	2.6	t_f (80% to 10%)	3.4
t_f (90% to 10%)	2.0	t_f (90% to 10%)	5.4
"NOR" OUTPUT			
t_{pd-} (50% to 50%)	2.6	t_r (10% to 80%)	3.8
t_{pd+} (50% to 50%)	2.5	t_r (10% to 90%)	5.4
t_r (10% to 90%)	2.4	t_f (80% to 10%)	3.7
t_f (90% to 10%)	2.7	t_f (90% to 10%)	5.7