CY8CPROTO-062S3-4343W

PSoC 62S3 Wi-Fi BT Prototyping Kit Guide

Doc. # 002-28070 Rev. *A

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone (USA): 800.858.1810
Phone (Intnl): +1.408.943.2600
www.cypress.com

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Contents

Safety and Regulatory Compliance Information

The CY8CPROTO-062S3-4343W PSoC® 62S3 Wi-Fi BT Prototyping Kit is intended for development purposes only. Users are advised to test and evaluate this kit in an RF development environment.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required authorizations are first obtained. Contact support@cypress.com for details.

The CY8CPROTO-062S3-4343W, as shipped from the factory, has been verified to meet with the requirements of CE as a Class A product.

PSoC 62S3 Wi-Fi BT Prototyping Boards contain electrostatic discharge (ESD)- sensitive devices. Electrostatic charges readily accumulate on the human body and any equipment, which can cause a discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused PSoC 62S3 Wi-Fi BT Prototyping Boards in the protective shipping package.

End-of-Life/Product Recycling

The end-of-life cycle for this kit is five years from the date of manufacture mentioned on the back of the box. Contact your nearest recycler to discard the kit.

General Safety Instructions

ESD Protection

ESD can damage boards and associated components. Cypress recommends that you perform procedures only at an ESD workstation. If an ESD workstation is unavailable, use appropriate ESD protection by wearing an anti-static wrist strap attached to a grounded metal object.

Handling Boards

CY8CPROTO-062S3-4343W PSoC 62S3 Wi-Fi BT Prototyping Kit is sensitive to ESD. Hold the board only by its edges. After removing the board from its box, place it on a grounded, static-free surface. Use a conductive foam pad, if available. Do not slide the board over any surface.

Regulatory Compliance Information

The CY8CPROTO-062S3-4343W PSoC 62S3 Wi-Fi BT Prototyping Kit contains devices that transmit and receive radio signals in accordance with the spectrum regulations for the 2.4-GHz unlicensed frequency range.

Cypress Semiconductor Corporation has obtained regulatory approvals for this kit to be used in specific countries. These countries include the United States (FCC Part 15), Canada (IC RSS210), and Japan (JRF/TELEC). Additional regional regulatory agency approval may be required to operate these throughout the world.

This kit, as shipped from the factory, has been tested and found to comply with the limits and requirements for the following compliances:

- As a Class B digital device, pursuant to part 15 of the FCC Rules.
- As a Class B digital apparatus, compliant with Canadian ICES-003.

CAUTION:

Only antennas with a peak gain of less than or equal to 1.4 dBi may be used with this device.

The manufacturer is not responsible for any radio or television interference caused by unauthorized modifications to this equipment. Such modifications could void the user's authority to operate the equipment.

Regulatory Statements and Product Labeling

United States (FCC)

The CY8CPROTO-062S3-4343W contains LBEE5KL1DX modular transmitter that complies with Part 15 of the Federal Communications Commission (FCC) Rules. The FCC ID for this device is **VPYLB1DX**.

Operation is subject to the following two conditions:

- This device may not cause harmful interference
- This device must accept any interference received, including interference that may cause undesired operation.

CAUTION: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. The antennas for this transmitter must be installed to provide a separation distance of 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

Canada (IC)

This device complies with the Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

- This device may not cause interference.
- This device must accept any interference, including interference that may cause undesired operation of the device.

This equipment complies with radio frequency exposure limits set forth by Industry Canada for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the device and the user or bystanders.

CAUTION: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Contains IC: **772C-LB1DX**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Cet équipement est conforme aux limites d'exposition aux radiofréquences définies par Industrie Canada pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre le dispositif et l'utilisateur ou des tiers.

Contains IC: **772C-LB1DX**

Japan (TELEC)

This product has built-in specified radio equipment which authorized “Japan Radio Certification” (certification number: 001-P00840) based on type approval system.

1. Introduction

Thank you for your interest in the CY8CPROTO-062S3-4343W PSoC 62S3 Wi-Fi BT Prototyping Kit (hereafter called PSoC 62S3 Wi-Fi BT Kit). The PSoC 62S3 Wi-Fi BT Kit enables you to evaluate and develop your applications using the PSoC 62 Series MCU (hereafter called “PSoC 6 MCU”) and CYW4343W WICED Wi-Fi/BT combo device.

PSoC 6 MCU is Cypress’ latest, ultra-low-power PSoC specifically designed for wearables and IoT products. PSoC 6 MCU is a true programmable embedded system-on-chip, integrating a 150-MHz ARM® Cortex®-M4 as the primary application processor, a 100-MHz ARM Cortex®-M0+ that supports low-power operations, up to 2 MB Flash and 1 MB SRAM, Secure Digital Host Controller (SDHC) supporting SD/SDIO/eMMC interfaces, CapSense® touch-sensing, and programmable analog and digital peripherals that allow higher flexibility, in-field tuning of the design, and faster time-to-market.

The PSoC 6 MCU on this kit has 512 KB of Flash and 256 KB of SRAM.

The PSoC 62S3 Wi-Fi BT Kit carries a PSoC 6 MCU and a CYW4343W based Wi-Fi and Bluetooth combination module. In addition, the board features an onboard programmer/debugger (KitProg3), a 512-MB Quad SPI NOR flash, a Micro-B connector for USB device interface, a 5-segment CapSense slider, two CapSense buttons, a user LED, and one push button. The board supports operating voltages from 1.8 V to 3.3 V for PSoC 6 MCU.

You can use ModusToolbox™ to develop and debug your PSoC 6 MCU projects. ModusToolbox software is a set of tools that enable you to integrate Cypress devices into your existing development methodology. Application development using PSoC 62S3 Wi-Fi BT Kit is also supported in other development environments such as Mbed OS.

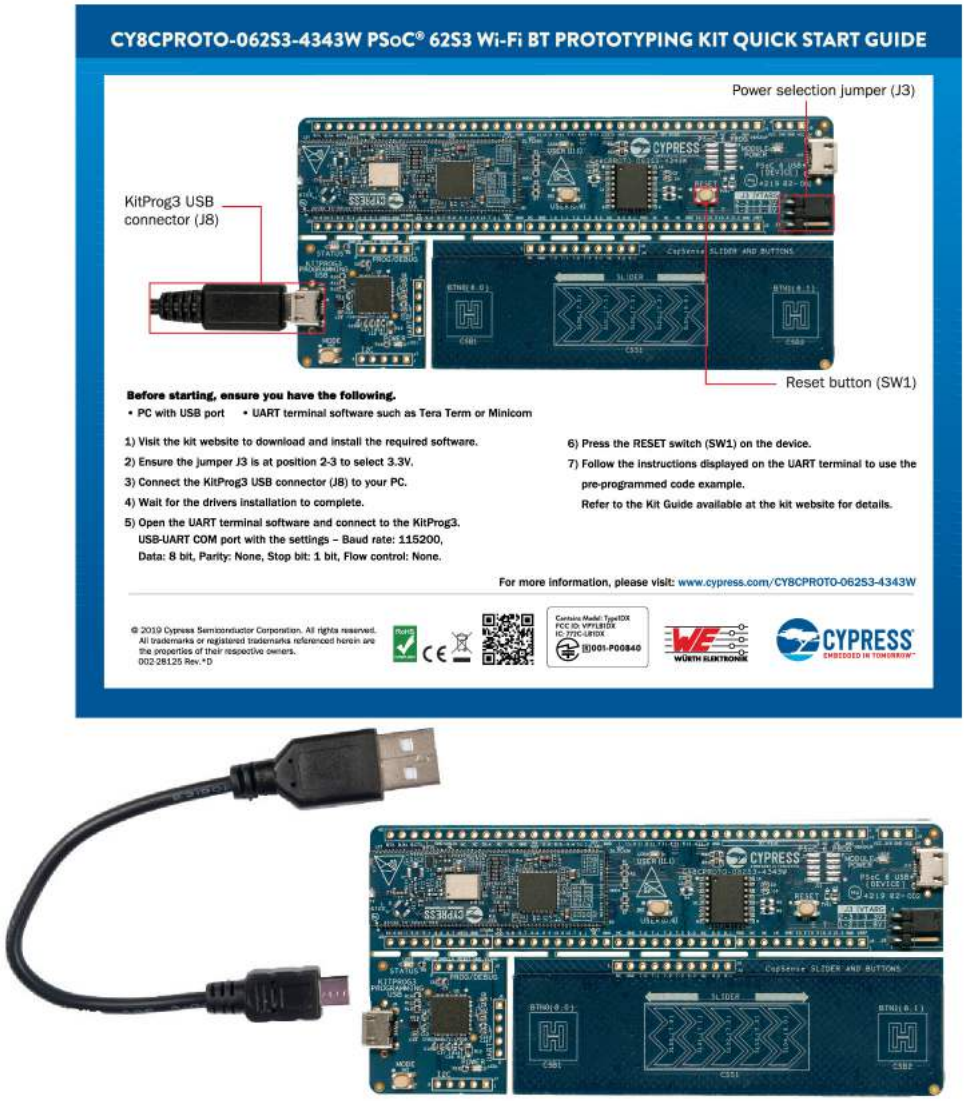
If you are new to PSoC 6 MCU and ModusToolbox IDE, refer to the application note AN221774 - Getting Started with PSoC 6 MCU to help you familiarize with the PSoC 6 MCU and help you create your own design using the ModusToolbox IDE.

1.1 Kit Contents

The PSoC 62S3 Wi-Fi BT Prototyping Kit package has the following contents, as shown in Figure 1-1.

- PSoC 62S3 Wi-Fi BT Prototyping Board
- USB Type-A to Micro-B cable
- Quick Start Guide

Figure 1-1. Kit Contents



Inspect the contents of the kit; if you find any part missing, contact your nearest Cypress sales office for help: www.cypress.com/support.

1.2 Getting Started

This guide will help you to get acquainted with the PSoC 62S3 Wi-Fi BT Kit:

- The Kit Operation chapter on page 16 describes the major features of the PSoC 62S3 Wi-Fi BT Kit and functionalities such as programming, debugging, and the USB-UART and USB-I^{2}C bridges.
- The Hardware chapter on page 25 provides a detailed hardware description, methods to use the onboard NOR Flash, kit schematics, and the bill of materials (BOM).
- Application development using PSoC 62S3 Wi-Fi BT Kit is supported in various development ecosystems such as ModusToolbox, and Mbed OS. For the latest software support for this development kit including the different development ecosystems, refer to the kit webpage.
  - ModusToolbox is a free development ecosystem that includes the ModusToolbox IDE and the PSoC 6 SDK. Using ModusToolbox IDE, you can enable and configure device resources, middleware libraries; and program and debug the device. You can download the software from the ModusToolbox home page. See the ModusToolbox Installation Guide for additional information.
  - Mbed OS: Visit Cypress' Mbed OS page on instructions to develop applications on Cypress's target board on the Mbed OS ecosystem.
- There are a wide range of code examples to evaluate the PSoC 62S3 Wi-Fi BT Kit. These examples help you familiarize yourself with the PSoC 6 MCU and create your own design. These examples are available in various development ecosystems such as ModusToolbox IDE, Mbed OS, etc. Visit Cypress's code example page to access examples for the following development ecosystems:
  - ModusToolbox based examples
  - Mbed OS based examples

1.3 Board Details

The PSoC 62S3 Wi-Fi BT Prototyping Kit that has the following features:

- CY8CMOD-062S3-4343W that contains
  - PSoC 6 MCU with SDHC
  - Murata Type 1DX ultra-small 2.4-GHz WLAN and Bluetooth module based on CYW4343W
- 512-Mbit external Quad SPI NOR Flash that provides a fast, expandable memory for data and code
- KitProg3 onboard SWD programmer/debugger, USB-UART and USB-I2C bridge functionality
- CapSense touch-sensing slider (5 elements) and two buttons, based on self-capacitance (CSD)
- A Micro-B connector for PSoC 6 MCU USB device interface
- 1.8 V and 3.3 V operation of PSoC 6 MCU is supported
- One user LED, one user button, and a reset button for PSoC 6 MCU
- One Mode selection button and one Status LED for KitProg3

Refer to Figure 2-4 for more details of the kit features.

Figure 1-2 shows the pinout of the PSoC 62S3 Wi-Fi BT Kit.

Figure 1-2. Prototyping Kit Pinout

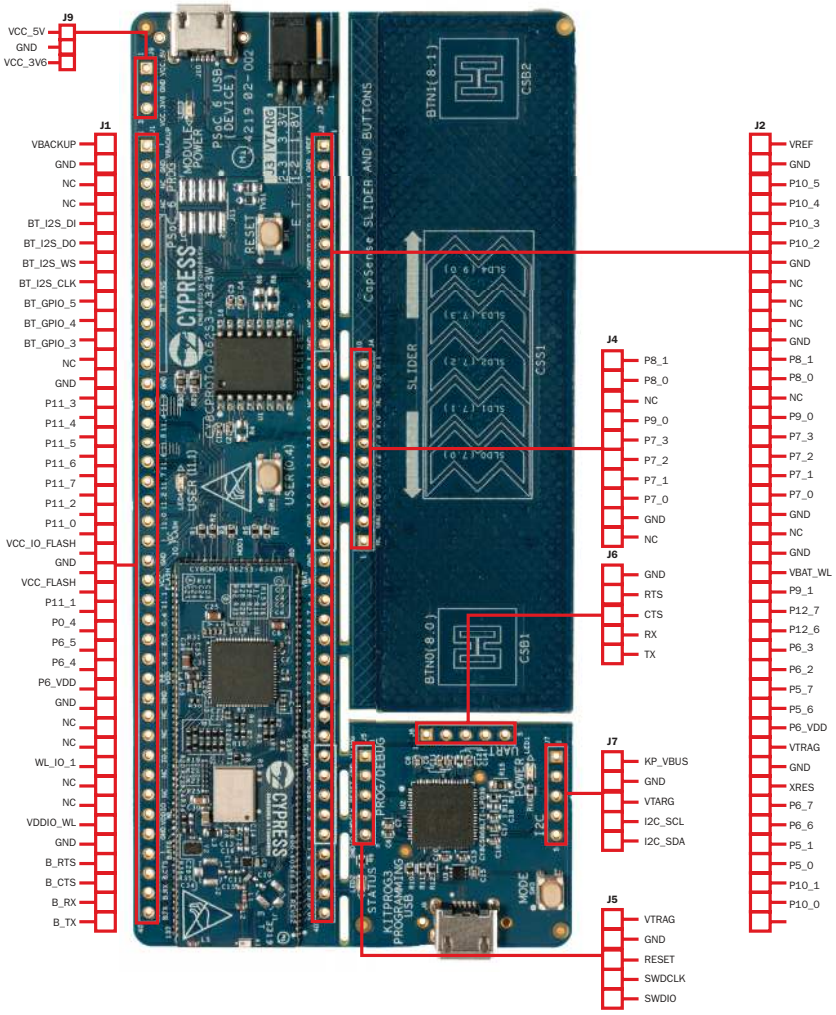


Table 1-1. Pioneer Board Pinout

Pin	Primary On-board Function	Secondary On-board Function	Connection details
PSoC 6 MCU Pins			
XRES	Hardware Reset	–	Remove R49 to disconnect it from KitProg3 RESET.
P0[4]	User Button with Hibernate wakeup capability	–	Configured as Active LOW switch
P5[0]	GPIO	–	–
P5[1]	GPIO	–	–
P5[6]	GPIO	–	–
P5[7]	GPIO	–	–
P6[4]	I2C SCL	–	Remove R21 to disconnect from KitProg3 I2C_SCL
P6[5]	I2C SDA	–	Remove R30 to disconnect from KitProg3 I2C_SDA
P6[6]	SWDIO	GPIO	–
P6[7]	SWDCLK	GPIO	–
P8[0]	CapSense Button0	GPIO	Connected to CapSense by default. Remove R84 to disconnect CapSense.
P8[1]	CapSense Button1	GPIO	Connected to CapSense by default. Remove R77 to disconnect CapSense.
P7[0]	CapSense Silder0	GPIO	Connected to CapSense by default. Remove R82 to disconnect CapSense.
P7[1]	CapSense Silder1	GPIO	Connected to CapSense by default. Remove R81 to disconnect CapSense.
P7[2]	CapSense Silder2	GPIO	Connected to CapSense by default. Remove R80 to disconnect CapSense.
P7[3]	CapSense Silder3	GPIO	Connected to CapSense by default. Remove R79 to disconnect CapSense.
P9[0]	CapSense Silder4	GPIO	Connected to CapSense by default. Remove R78 to disconnect CapSense.
P9[1]	GPIO	–	–
P7[7]	CMOD	–	–
P10[0]	UART RX	GPIO	Connected to KitProg3 UART TX pin. Remove R53 to disconnect from KitProg3.
P10[1]	UART TX	GPIO	Connected to KitProg3 UART RX pin. Remove R64 to disconnect from KitProg3.
P10[2]	GPIO	UART RTS	Populate R29 to connect to KitProg3 UART CTS.

Table 1-1. Pioneer Board Pinout *(continued)*

Pin	Primary On-board Function	Secondary On-board Function	Connection details
P10[3]	GPIO	UART CTS	Populate R33 to connect to KitProg3 UART RTS.
P10[4]	GPIO	–	–
P10[5]	GPIO	–	–
P11[0]	GPIO	–	–
P11[1]	Red User LED	–	–
P11[2]	QSPI FLASH CS	GPIO	–
P11[3]	QSPI Flash IO3	GPIO	Remove R2 to isolate from external memory and use as a GPIO
P11[4]	QSPI Flash IO2	GPIO	Remove R7 to isolate from external memory and use as a GPIO
P11[5]	QSPI Flash IO1	GPIO	Remove R1 to isolate from external memory and use as a GPIO
P11[6]	QSPI Flash IO0	GPIO	Remove R3 to isolate from external memory and use as a GPIO
P11[7]	QSPI FLASH CLK	GPIO	Remove R5 to isolate from external memory and use as a GPIO
P12[6]	GPIO	–	–
P12[7]	GPIO	–	–
USB_DP	USB-FS device interface	–	–
USB_DM	USB-FS device interface	–	–
CYW4343 Pins			
BT_UART_TXD	UART interface with Host MCU (PSoC 6 MCU)	–	Connected to UART RX pin (P3.0) of PSoC 6 MCU by default. To connect to KitProg3, remove R64 and populate R63
BT_UART_RXD	UART interface with Host MCU (PSoC 6 MCU)	–	Connected to UART TX pin (P3.1) of PSoC 6 MCU by default. To connect to KitProg3, remove R53 and populate R52
BT_UART_CTS	UART interface with Host MCU (PSoC 6 MCU)	–	Connected to UART RTS pin (P9.2) of PSoC 6 MCU by default. To connect to KitProg3, remove R33 (if loaded) and populate R26
BT_UART_RTS	UART interface with Host MCU (PSoC 6 MCU)	–	Connected to UART CTS pin (P9.3) of PSoC 6 MCU by default. To connect to KitProg3, remove R29 (if loaded) and populate R24
BT_I2S_WS	I2S Word Select	–	–
BT_I2S_CLK	I2S Clock	–	–
BT_I2S_DI	I2S Data Input	–	–

Table 1-1. Pioneer Board Pinout *(continued)*

Pin	Primary On-board Function	Secondary On-board Function	Connection details
BT_I2S_DO	I2S Data Output	–	–
BT_GPIO_2	NC	–	BT_GPIO_2 pin is not routed on to the castellated pads on CY8CMOD-062S3-4343W carrier module. Hence this pin is NC on the kit.
BT_GPIO_3	Bluetooth GPIO	–	–
BT_GPIO_4	Bluetooth GPIO	–	–
BT_GPIO_5	Bluetooth GPIO	–	–
WL_IO_1	GPIO	–	–

1.4 Additional Learning Resources

Cypress provides a wealth of data at www.cypress.com/psoc6 to help you to select the right PSoC device for your design and to help you to quickly and effectively integrate the device into your design.

1.5 Technical Support

For assistance, visit Cypress Support or contact customer support at +1(800) 541-4736 Ext. 3 (in the USA) or +1 (408) 943-2600 Ext. 3 (International).

You can also use the following support resources if you need quick assistance:

- Self-help (Technical Documents)
- Local Sales Office Locations

1.6 Documentation Conventions

Table 1-2. Document Conventions for Guides

Convention	Usage
`Courier New`	Displays file locations, user entered text, and source code: `C:\...cd\icc\`
Italics	Displays file names and reference documentation: Read about the *sourcefile.hex* file in the *PSoC Creator User Guide*.
[**Bracketed, Bold**]	Displays keyboard commands in procedures: [**Enter**] or [**Ctrl**] [**C**]
File > Open	Represents menu paths: File > Open > New Project
Bold	Displays commands, menu paths, and icon names in procedures: Click the **File** icon and then click **Open**.
Times New Roman	Displays an equation: 2 + 2 = 4
Text in gray boxes	Describes cautions or unique functionality of the product.

1.7 Acronyms

Table 1-3. Acronyms Used in this Document

Acronym	Definition
ADC	Analog-to-Digital Converter
BLE	Bluetooth Low Energy
BOM	Bill of Materials
CMOD	Modulator Capacitor
CPU	Central Processing Unit
CSD	CapSense Sigma Delta
DC	Direct Current
Del-Sig	Delta-Sigma
DMA	Direct Memory Access
ECO	External Crystal Oscillator
ESD	Electrostatic Discharge
GPIO	General-Purpose Input/Output
HID	Human Interface Device
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IC	Integrated Circuit
IDE	Integrated Development Environment
IoT	Internet of Things
LED	Light-emitting Diode
LPO	Low Power Oscillator
OOB	Out Of Box
PC	Personal Computer
PSoC	Programmable System-on-Chip
PWM	Pulse Width Modulation
QSPI	Quad Serial Peripheral Interface
SAR	Successive Approximation Register
SDHC	Secure Digital Host Controller
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SMIF	Serial Memory Interface
SPI	Serial Peripheral Interface
SRAM	Serial Random Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
WCO	Watch Crystal Oscillator

2. Kit Operation

This chapter introduces you to various features of the PSoC 62S3 Wi-Fi BT Prototyping Board, including the theory of operation and the onboard programming and debugging functionality, KitProg3 USB-UART and USB-I2C bridges.

2.1 Theory of Operation

The PSoC 62S3 Wi-Fi BT Prototyping Board is built around PSoC 6 MCU. Figure 2-1 shows the block diagram of the PSoC 6 MCU device used in the PSoC 62S3 Wi-Fi BT Prototyping Board. For details of device features, see the device datasheet.

Figure 2-1. PSoC 6 MCU Block Diagram

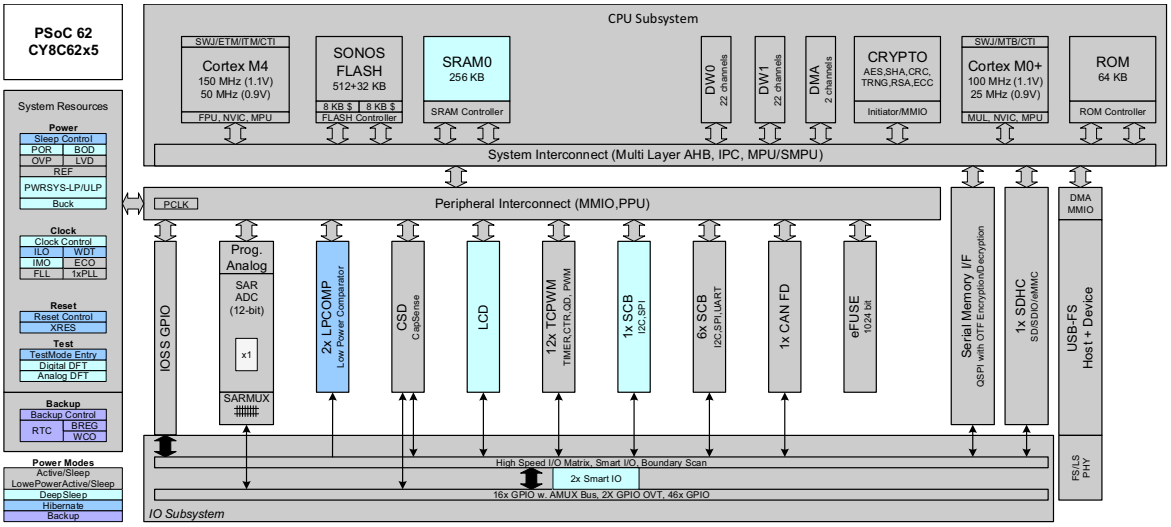


Figure 2-2. Block Diagram of Prototyping Kit

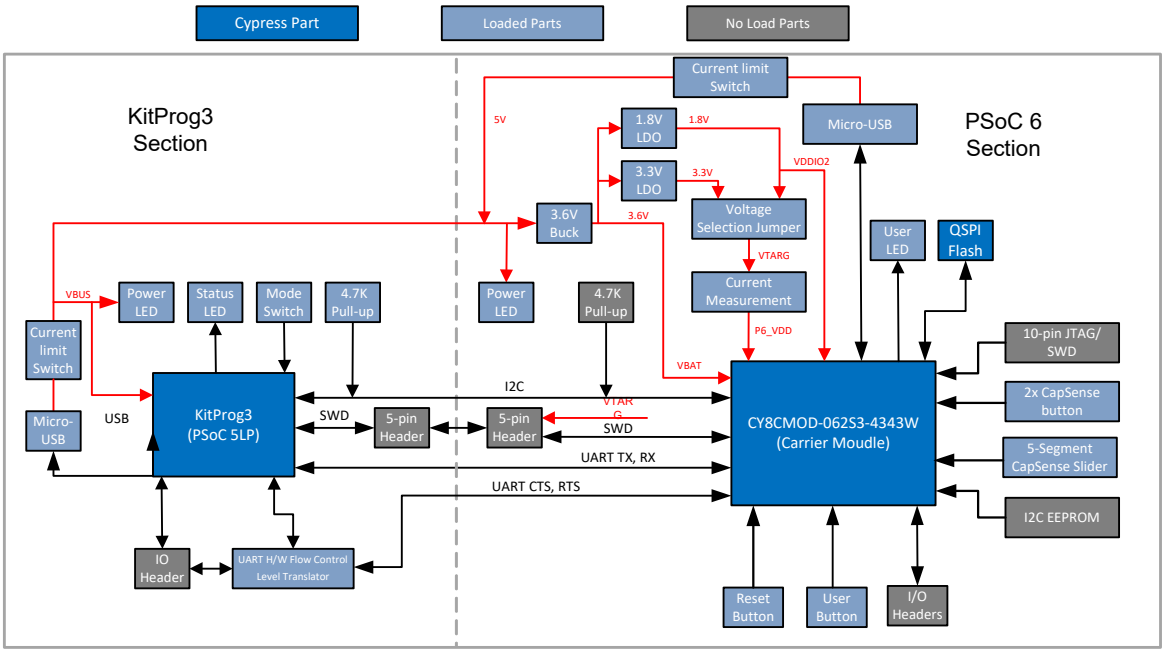


Figure 2-3. Block Diagram of CY8CMOD-062S3-4343W (Carrier Module)

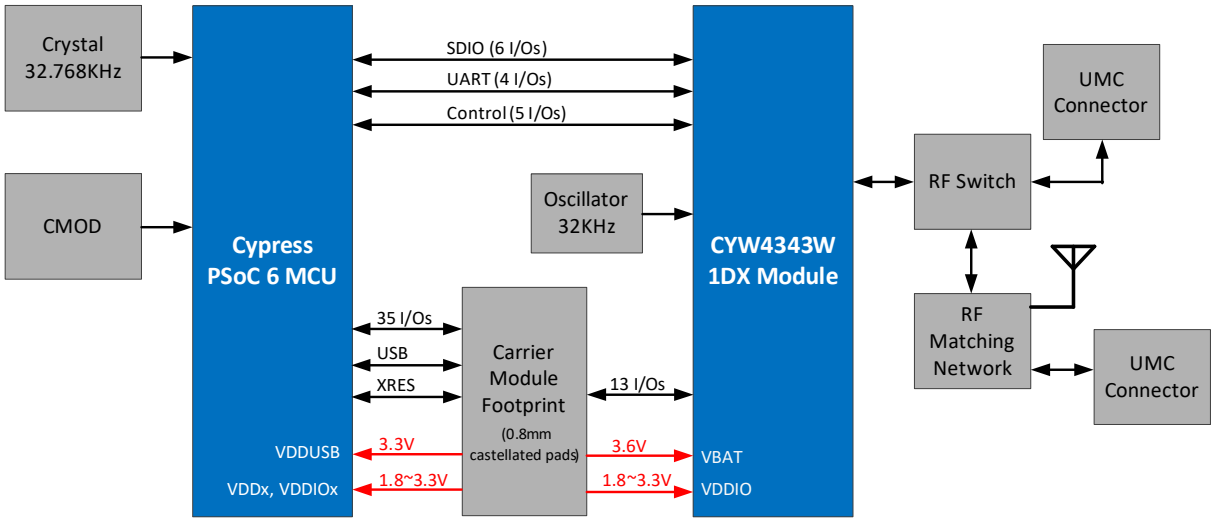
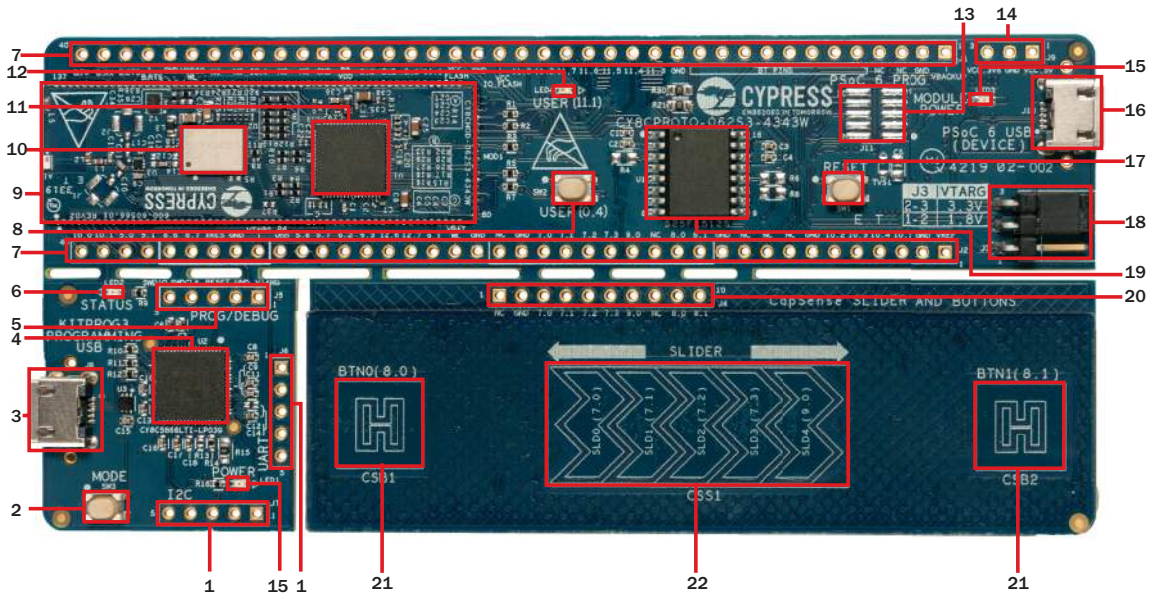


Figure 2-4. PSoC 62S3 Wi-Fi BT Prototyping Board - Top View



The PSoC 62S3 Wi-Fi BT Prototyping Board has the following peripherals:

1. **KitProg3 I/O headers (J6, J7):** These headers bring out the USB-UART and USB-I2C interface pins of the KitProg3 respectively. If the KitProg3 section is broken away, it is also necessary to connect VTARG and GND as this is used to voltage level translation.
2. **KitProg3 programming mode selection button (SW3):** This button can be used to switch between various modes of operation of KitProg3 (CMSIS-DAP BULK, CMSIS-DAP HID or DAPLink modes). For more details, see the KitProg3 User Guide.
3. **KitProg3 USB connector (J8):** The USB cable provided along with the PSoC 62S3 Wi-Fi BT Kit connects between this USB connector and the PC to use the KitProg3 onboard programmer and debugger and powers the board.
4. **KitProg3 (PSoC 5LP) programmer and debugger (CY8C5868LTI-LP039, U2):** The PSoC 5LP device (CY8C5868LTI-LP039) serving as KitProg3, is a multi-functional system, which includes a SWD programmer, debugger, USB-I2C bridge and USB-UART bridge. For more details, see the KitProg3 User Guide.
5. **KitProg3 5-pin programming header (J5):** This header brings out the SWD interface pins of the KitProg3. This is used to program and debug the PSoC 6 MCU. If KitProg3 section is broken away, it can be used to program any device over the 5-pin interface. Please note that VTARG is an input to KitProg3, and hence target must be powered externally. In the PSoC 62S3 Wi-Fi BT Kit, the on-board regulators on the PSoC 6 MCU section provide VTARG.
6. **KitProg3 status LED (LED2):** Amber LED indicates the status of KitProg3. For details on the KitProg3 status, see the KitProg3 User Guide.
7. **PSoC 6 MCU I/O headers (J1, J2):** These headers provide connectivity to PSoC 6 MCU GPIOs. Most of these I/Os are also connected to on-board peripherals.
8. **PSoC 6 MCU user button (SW2):** This button can be used to provide an input to PSoC 6 MCU. Note that by default the button connects the PSoC 6 MCU pin to ground when pressed, so you need to configure the PSoC 6 MCU pin as a digital input with resistive pull-up for detecting the button press. This button also provides a wake-up source from low-power modes of the device. In addition, this button can be used to activate the regulator control output from PSoC 6 MCU.

9. **Cypress PSoC 6 (512K) with CYW4343W Carrier Module (CY8CMOD-062S3-4343W, MOD1):** This kit is designed to highlight the features of the PSoC 6 MCU on the CY8CMOD-062S3-4343W. For details refer to Hardware chapter on page 25.
10. **CYW4343W based Murata 1DX Module:** The Type 1DX module is an ultra-small module that includes 2.4 GHz WLAN and Bluetooth functionality. Based on the Cypress CYW4343W, the module provides high-efficiency RF front end circuits. To ease Wi-Fi certification, the Type 1DX module complies with IEEE 802.11b/g/n and Bluetooth Version 4.2 plus EDR, Power Class (10 dBm max) + BLE.
11. **PSoC 6 MCU:** This kit is designed to highlight the features of the PSoC 6 MCU. For details on PSoC 6 MCU pin mapping, refer to Table 1-1 on page 12.
12. **PSoC 6 MCU user LED (LED4):** The red user LED can operate over the entire operating voltage range of PSoC 6 MCU. The LED is active LOW, so the pins must be driven to ground to turn ON the LED.
13. **PSoC 6 MCU program and debug header (J11):** This 10-pin header allows you to program and debug the PSoC 6 MCU using an external programmer such as MiniProg4. Please note that this is not loaded by default.
14. **External Power Supply VIN connector (J9):** This connector connects an external DC power supply input to the onboard regulators. The voltage input from the external supply should be between 3.6 V and 5 V. Note that this is not required when powering via one of the two Micro-USB connectors on the board.
15. **Power LEDs (LED1, LED3):** LED1 and LED3 are amber LEDs that indicate the status of power supplied to PSoC 5LP and PSoC 6 MCU respectively.
16. **PSoC 6 USB device connector (J10):** The USB cable provided with the PSoC 62S3 Wi-Fi BT Prototyping Kit can be connected between this USB connector and the PC to use the PSoC 6 MCU USB device applications.
17. **PSoC 6 MCU reset button (SW1):** This button is used to reset PSoC 6 MCU. This button connects the PSoC 6 MCU reset (XRES) pin to ground.
18. **System Power selection jumper (J3):** This switch is used to select the PSoC 6 MCU's supply voltage (P6_VDD) between 1.8 V and 3.3 V.
19. **Cypress 512-Mbit serial NOR flash memory (S25FL512S, U1):** The S25HL512T NOR flash of 512Mbit capacity is connected to the Quad SPI interface of the PSoC 6 MCU. The NOR device can be used for both data and code memory with execute-in-place (XIP) support and encryption.
20. **CapSense header (J4):** CapSense section is independent and can be broken away from the PSoC 6 MCU section.
21. **CapSense buttons (BTN0 and BTN1):** CapSense touch-sensing buttons, capable of self-capacitance (CSD) operation, let you evaluate Cypress' fourth-generation CapSense technology.
22. **CapSense slider (SLIDER):** CapSense touch-sensing slider capable of self-capacitance (CSD) operation. The slider and the buttons have a 1-mm acrylic overlay for smooth touch sensing.

See Hardware Functional Description on page 25 for details on various hardware blocks.

2.2 KitProg3: On-Board Programmer/Debugger

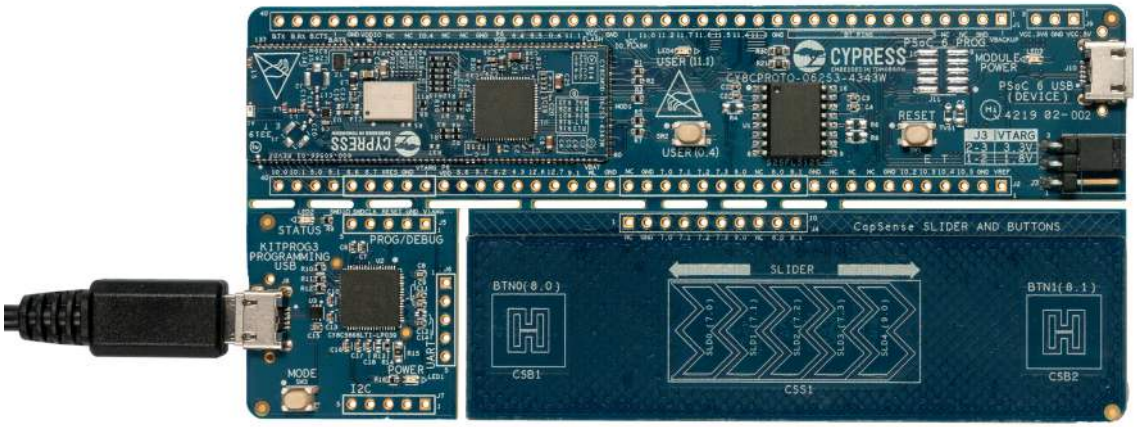
The PSoC 62S3 Wi-Fi BT Prototyping Board can be programmed and debugged using the onboard KitProg3. KitProg3 is an onboard programmer/debugger with USB-UART and USB-I2C. Mass Storage programming is supported in DAPLink mode. A Cypress PSoC 5LP device is used to implement KitProg3 functionality. For more details on the KitProg3 functionality, see the KitProg3 User Guide.

2.2.1 Programming and Debugging using ModusToolbox IDE

This section presents a quick overview of programming and debugging using ModusToolbox IDE. For detailed instructions, see **Help** > **ModusToolbox IDE Documentation** > **User Guide**.The steps below use the PSoC 6 MCU: Hello World example, which is the Out Of Box (OOB) project of this kit, to illustrate programming and debugging in ModusToolbox IDE.

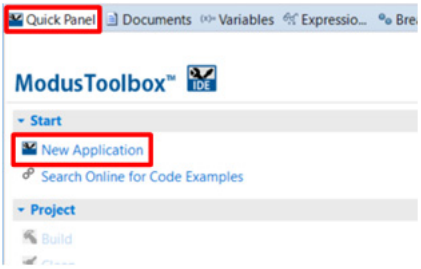
1. Connect the board to the PC using the USB cable, as shown in Figure 2-5. It enumerates as a USB Composite Device if you are connecting it to your PC for the first time. KitProg3 can operate either in CMSIS-DAP Bulk mode (default) or CMSIS-DAP HID mode or DAPLink mode. Programming is faster with the Bulk mode. The status LED (Amber) is always ON in Bulk mode, ramping at 1 Hz rate in HID mode, and ramping at 2 Hz rate in DAPLink mode. Press and release the Mode select button (SW3) to switch between these modes. If you do not see the desired LED status, see the KitProg3 User Guide for details on the KitProg3 status and troubleshooting instructions.

Figure 2-5. Connect USB Cable to USB Connector on the Board



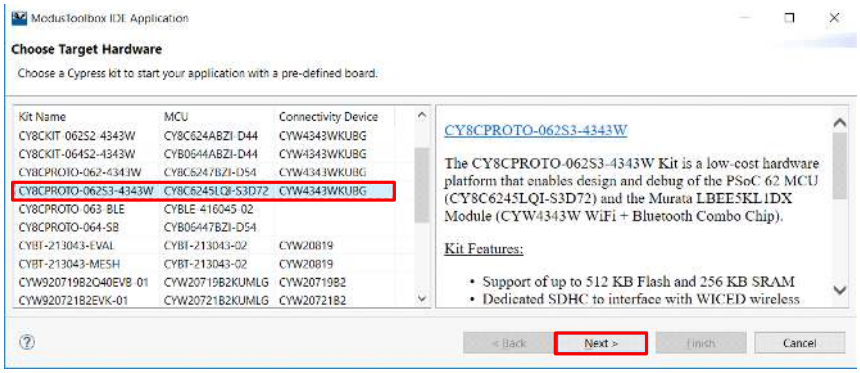
2. In the ModusToolbox IDE, import the desired code example (application) into a new workspace.
   a. Click on **New Application** from the **Quick Panel**.

Figure 2-6. Create New Application



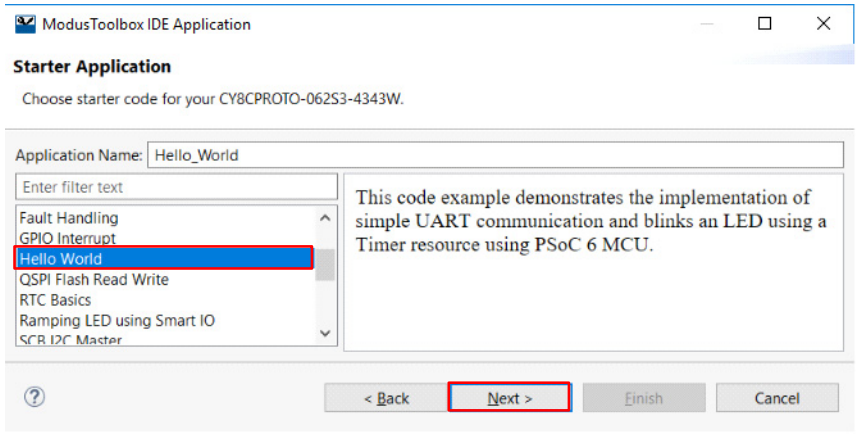
b. Select the CY8CPROTO-062S3-4343W in the **Choose Hardware Target** window and click **Next**, as shown in Figure 2-7.

Figure 2-7. New Application Creation: Choose Target Hardware



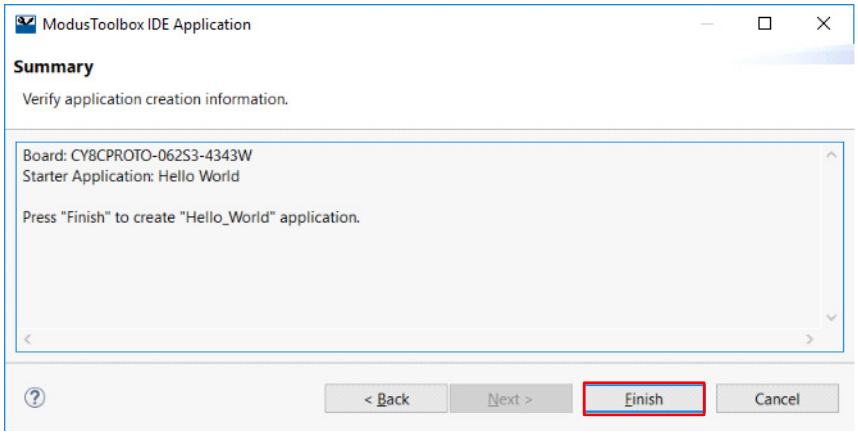
c. Select the desired application in the **Starter Application** window and click **Next**, as shown in Figure 2-8. If desired, you can change the application name in this window.

Figure 2-8. New Application Creation: Select Starter Application



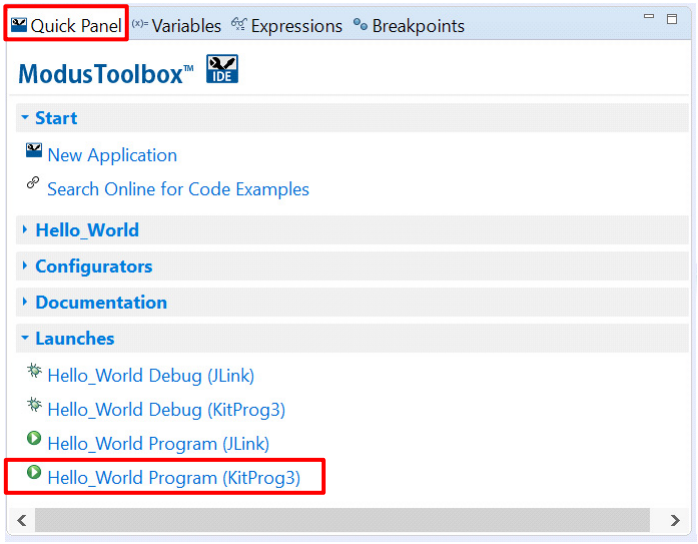
d. Click **Finish** in the **Summary** window, as shown in Figure 2-9.

Figure 2-9. New Application Creation: Summary



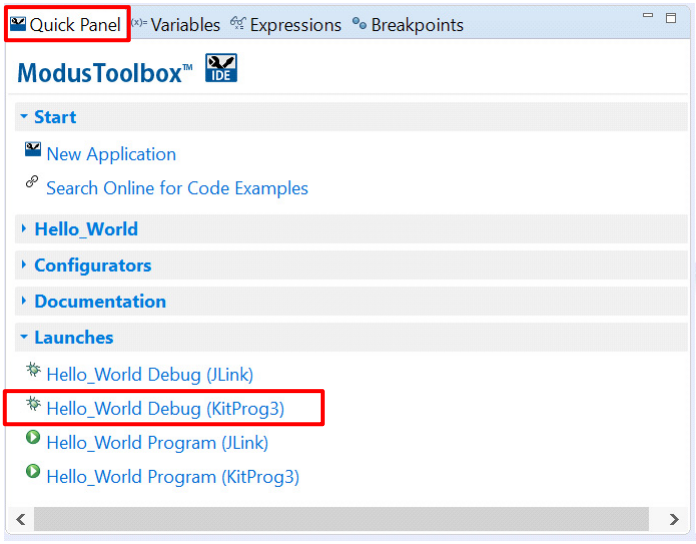
3. To build and program a PSoC 6 MCU application, in the Project Explorer, select **<App_Name>** project. In the Quick Panel, scroll to the Launches section and click the **<App_Name> Program (KitProg3)** configuration as shown in Figure 2-10.

Figure 2-10. Programming in ModusToolbox



4. ModusToolbox has an integrated debugger. To debug a PSoC 6 MCU application, in the Project Explorer, select **<App_Name>** project. In the Quick Panel, scroll to the Launches section and click the **<App_Name> Debug (KitProg3)** configuration as shown in Figure 2-11. Note that Debug operation would perform a build operation followed by program operation and finally the debug operation.

Figure 2-11. Debugging in ModusToolbox



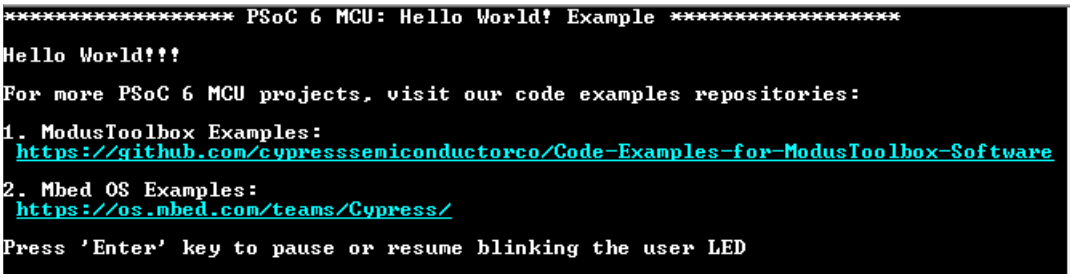
2.2.1.1 Using the OOB Example – PSoC 6 MCU: Hello World

The PSoC 62S3 Wi-Fi BT Prototyping Board is by default programmed with the code example: PSoC 6 MCU: Hello World. The steps below describe on how to use the example. For a detailed description of the project refer to the example's readme file in the GitHub repository.

Note: At any point of time, if you overwrite the OOB example, you can restore it back by programming the PSoC 6 MCU: Hello World application. Refer Programming and Debugging using ModusToolbox IDE on page 20 for programming the board.

1. Connect the board to your PC using the provided USB cable through the KitProg3 USB connector.
2. Open a terminal program and select the KitProg3 COM port. Set the serial port parameters to 8N1 and 115200 baud.
3. Press the reset button (**SW1**) on the board and confirm that "Hello World!!!" and other text is displayed on the UART terminal as shown in Figure 2-12.

Figure 2-12. Hello World in Terminal



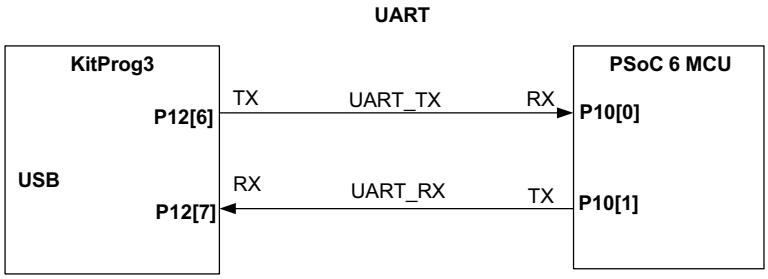
4. Confirm that the kit LED blinks at 1 Hz.
5. Press the Enter key. Confirm that the kit LED stops blinking. The terminal displays the message "LED blinking paused".
6. Press the Enter key again. Confirm that the kit LED resumes blinking at 1 Hz. The message displayed on the terminal is updated to "LED blinking resumed".

You can repeat Steps 5 and 6 indefinitely.

2.2.2 USB-UART Bridge

The KitProg3 on the PSoC 62S3 Wi-Fi BT Prototyping Board can act as a USB-UART bridge. The UART and flow-control lines between the PSoC 6 MCU and the KitProg3 are hard-wired on the board, as Figure 2-13 shows. For more details on the KitProg3 USB-UART functionality, see the KitProg3 User Guide.

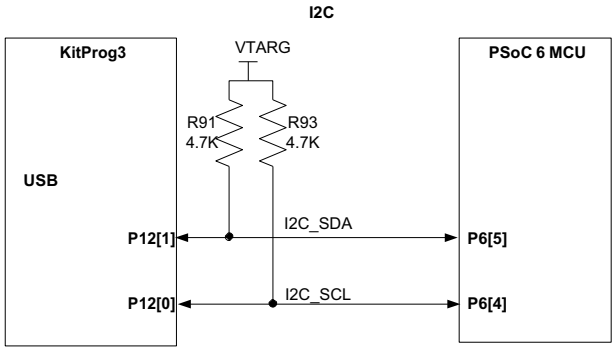
Figure 2-13. UART Connection between KitProg3 and PSoC 6 MCU



2.2.3 USB-I2C Bridge

The KitProg3 can function as a USB-I2C bridge and communicate with the Bridge Control Panel (BCP) software. The I2C lines on the PSoC 6 MCU are hard-wired on the board to the I2C lines of the KitProg3, with onboard pull-up resistors as Figure 2-14 shows. The USB-I2C supports I2C speeds of 50 kHz, 100 kHz, 400 kHz, and 1 MHz. For more details on the KitProg3 USB-I2C functionality, see the KitProg3 User Guide.

Figure 2-14. I2C Connection between KitProg3 and PSoC 6 MCU



3. Hardware

3.1 Schematics

Refer to the schematic files available in the kit webpage.

3.2 Hardware Functional Description

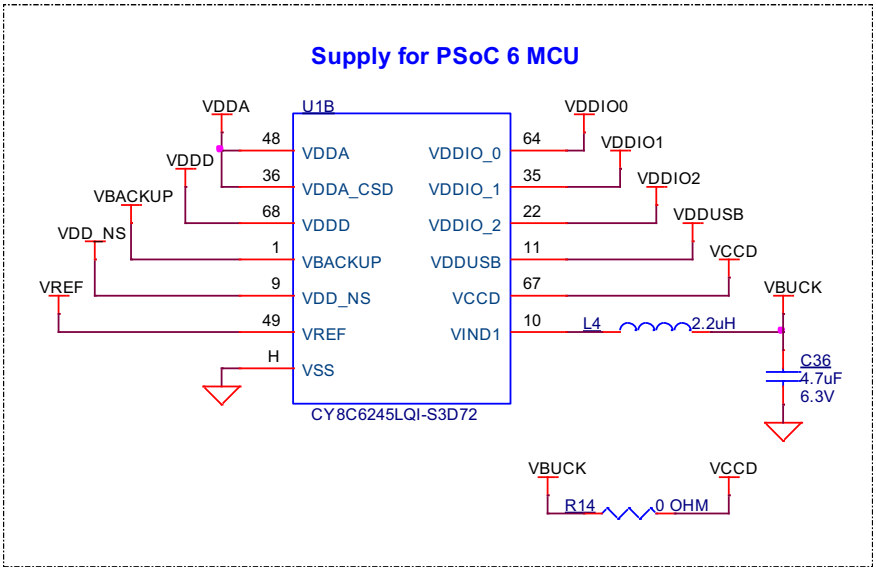
This section explains in detail the individual hardware blocks of the PSoC 62S3 Wi-Fi BT Prototyping Board.

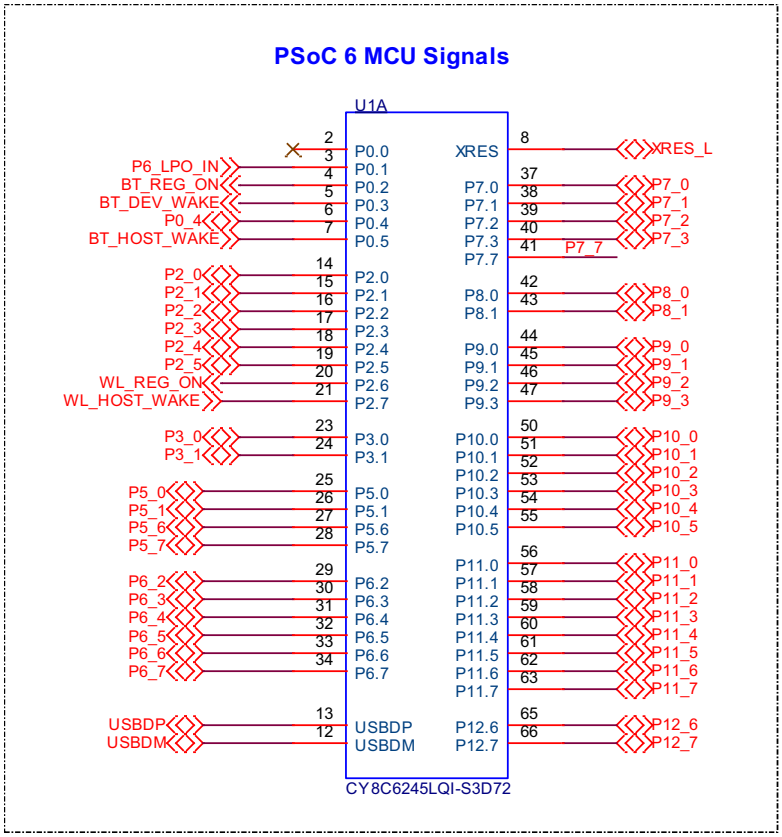
3.2.1 CY8CMOD-062S3-4343W (MOD1)

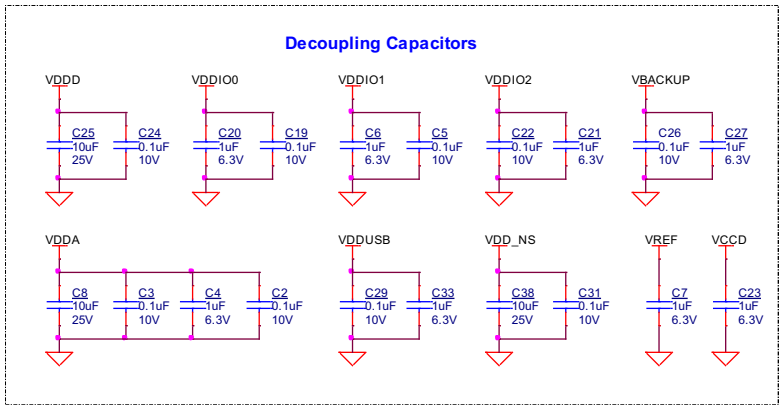
CY8CMOD-062S3-4343W is a castellated PCB module which consists mainly of PSoC 6 MCU and CYW4343W devices. The module also houses a 2.45GHz/5GHz dual band chip antenna, RF switch for antenna diversity, Low Power Oscillator (LPO) for CYW4343W and PSoC 6 MCU, modulation capacitor to support CapSense and other passive components required for the proper working of PSoC 6 MCU and CYW4343W. A Pre-certified Type 1DX module with CYW4343W from Murata, LBEE5KL1DX, is used for ease of development. CYW4343W supports only 2.45GHz band, but the antenna used is 2450AD14A5500 Dual Band 2.45GHz/5GHz Mini Chip Antenna from Johanson, to use the same antenna across different designs. The castellated PCB module has 137 castellated pads, which are used for different voltage rails and I/O signals of PSoC 6 MCU and CYW4343W.

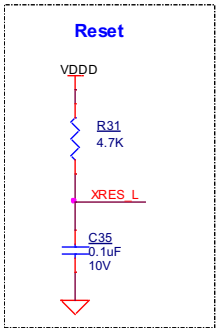
For more information, see the PSoC 6 MCU webpage, Type 1DX module webpage, PSoC 6 MCU datasheet and CYW4343W datasheet.

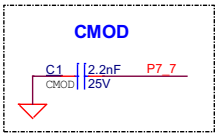
Figure 3-1. Schematics of CY8CMOD-062S3-4343W

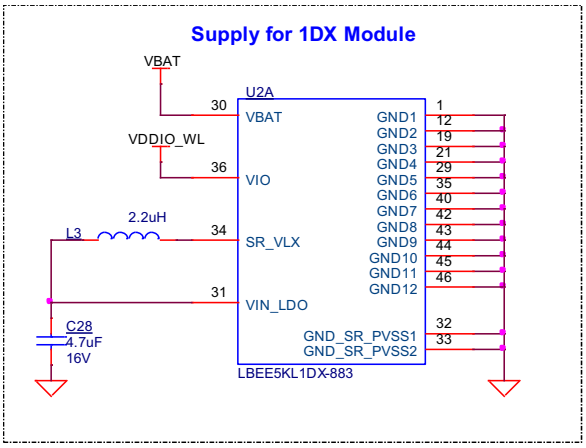


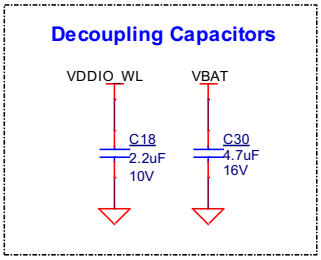

PSoC 6 MCU Signals
U1A
P6_LPO_IN
BT_REG_ON
BT_DEV_WAKE
P0_4
BT_HOST_WAKE
P2_0
P2_1
P2_2
P2_3
P2_4
P2_5
WL_REG_ON
WL_HOST_WAKE
P3_0
P3_1
P5_0
P5_1
P5_6
P5_7
P6_2
P6_3
P6_4
P6_5
P6_6
P6_7
USBDP
USBDM
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P2.0
P2.1
P2.2
P2.3
P2.4
P2.5
P2.6
P2.7
P3.0
P3.1
P5.0
P5.1
P5.6
P5.7
P6.2
P6.3
P6.4
P6.5
P6.6
P6.7
USBDP
USBDM
XRES
P7.0
P7.1
P7.2
P7.3
P7.7
P8.0
P8.1
P9.0
P9.1
P9.2
P9.3
P10.0
P10.1
P10.2
P10.3
P10.4
P10.5
P11.0
P11.1
P11.2
P11.3
P11.4
P11.5
P11.6
P11.7
P12.6
P12.7
XRES_L
P7_0
P7_1
P7_2
P7_3
P7_7
P8_0
P8_1
P9_0
P9_1
P9_2
P9_3
P10_0
P10_1
P10_2
P10_3
P10_4
P10_5
P11_0
P11_1
P11_2
P11_3
P11_4
P11_5
P11_6
P11_7
P12_6
P12_7
CY8C6245LQI-S3D72

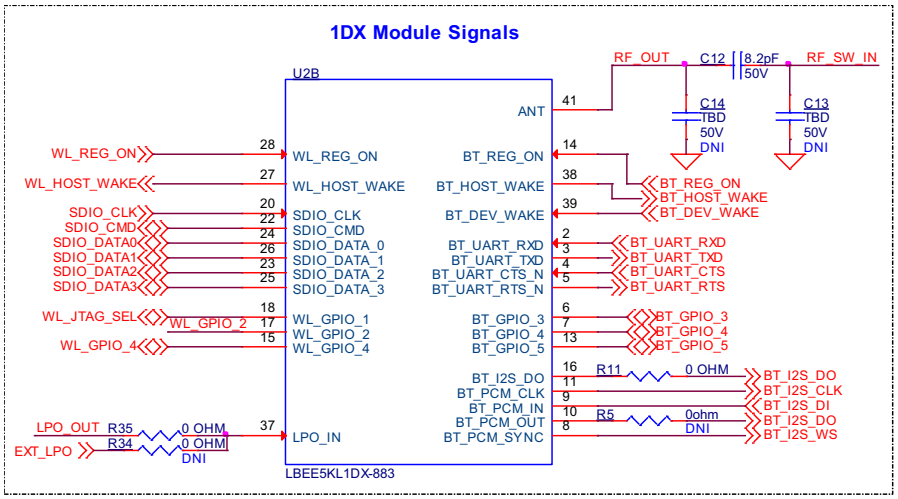

Decoupling Capacitors
VDDD
C25 10uF 25V
C24 0.1uF 10V
VDDIO0
C20 1uF 6.3V
C19 0.1uF 10V
VDDIO1
C6 1uF 6.3V
C5 0.1uF 10V
VDDIO2
C22 0.1uF 10V
C21 1uF 6.3V
VBACKUP
C26 0.1uF 10V
C27 1uF 6.3V
VDDA
C8 10uF 25V
C3 0.1uF 10V
C4 1uF 6.3V
C2 0.1uF 10V
VDDUSB
C29 0.1uF 10V
C33 1uF 6.3V
VDD_NS
C38 10uF 25V
C31 0.1uF 10V
VREF
C7 1uF 6.3V
VCCD
C23 1uF 6.3V

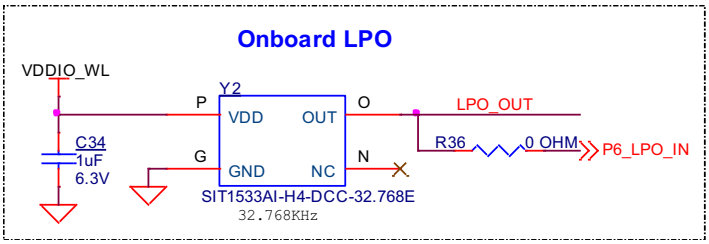

Reset
VDDD
R31
4.7K
XRES_L
C35
0.1uF
10V

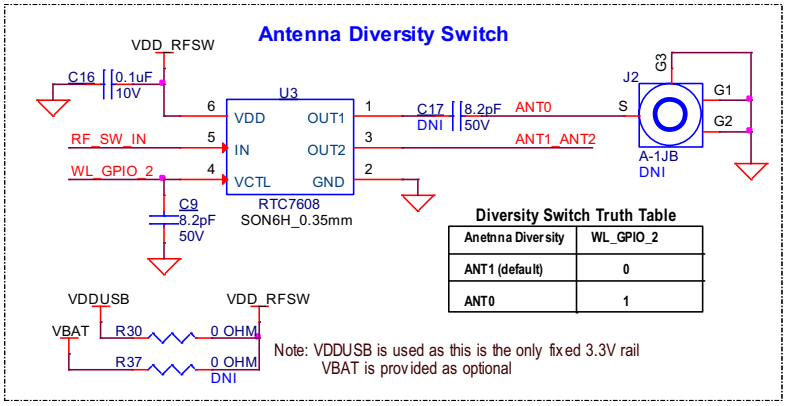

CMOD
C1
2.2nF
25V
CMOD
P7_7

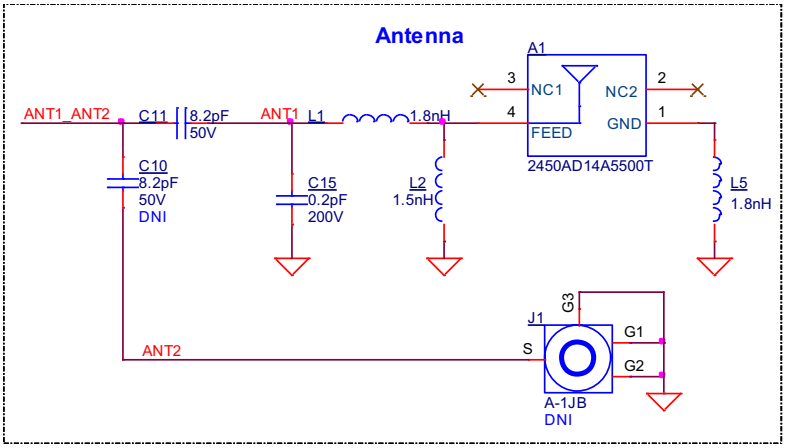

Supply for 1DX Module
VBAT
U2A
30
VBAT
VDDIO_WL
36
VIO
2.2uH
L3
34
SR_VLX
31
VIN_LDO
C28
4.7uF
16V
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
1
12
19
21
29
35
40
42
43
44
45
46
32
33
GND_SR_PVSS1
GND_SR_PVSS2
LBEE5KL1DX-883


Decoupling Capacitors
VDDIO_WL
VBAT
C18
2.2uF
10V
C30
4.7uF
16V

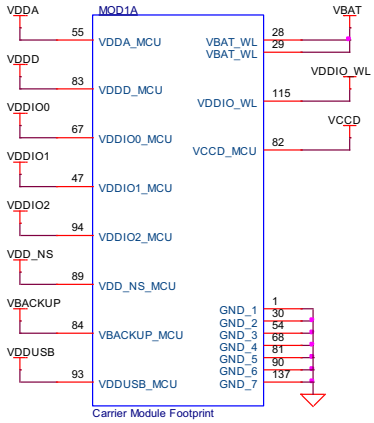

1DX Module Signals
U2B
RF_OUT
C12
8.2pF
50V
RF_SW_IN
ANT
41
C14
TBD
50V
DNI
C13
TBD
50V
DNI
WL_REG_ON
28
WL_REG_ON
BT_REG_ON
14
WL_HOST_WAKE
27
WL_HOST_WAKE
BT_HOST_WAKE
38
BT_REG_ON
BT_HOST_WAKE
BT_DEV_WAKE
39
BT_DEV_WAKE
SDIO_CLK
SDIO_CMD
SDIO_DATA0
SDIO_DATA1
SDIO_DATA2
SDIO_DATA3
20
22
24
26
23
25
SDIO_CLK
SDIO_CMD
SDIO_DATA_0
SDIO_DATA_1
SDIO_DATA_2
SDIO_DATA_3
BT_UART_RXD
BT_UART_TXD
BT_UART_CTS_N
BT_UART_RTS_N
2
3
4
5
BT_UART_RXD
BT_UART_TXD
BT_UART_CTS
BT_UART_RTS
WL_JTAG_SEL
WL_GPIO_2
WL_GPIO_4
18
17
15
WL_GPIO_1
WL_GPIO_2
WL_GPIO_4
BT_GPIO_3
BT_GPIO_4
BT_GPIO_5
6
7
13
BT_GPIO_3
BT_GPIO_4
BT_GPIO_5
R11
0 OHM
16
11
9
10
8
BT_I2S_DO
BT_PCM_CLK
BT_PCM_IN
BT_PCM_OUT
BT_PCM_SYNC
R5
0ohm
DNI
BT_I2S_DO
BT_I2S_CLK
BT_I2S_DI
BT_I2S_DO
BT_I2S_WS
LPO_OUT
R35
0 OHM
EXT_LPO
R34
0 OHM
DNI
37
LPO_IN
LBEE5KL1DX-883

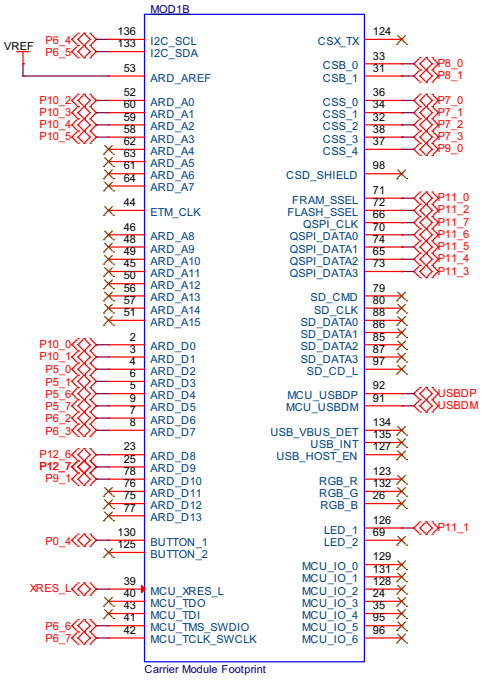

Onboard LPO
VDDIO_WL
Y2
P
VDD
OUT
O
LPO_OUT
R36
0 OHM
P6_LPO_IN
C34
1uF
6.3V
G
GND
NC
N
SIT1533AI-H4-DCC-32.768E
32.768KHz

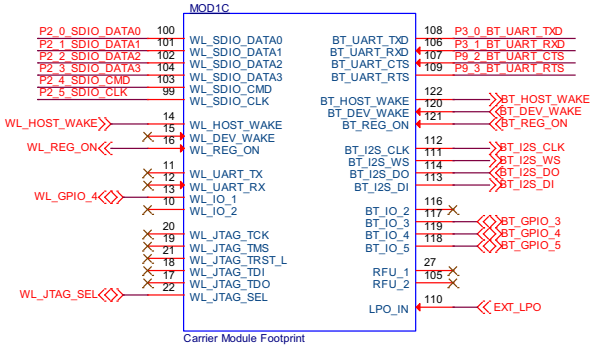

Antenna Diversity Switch
VDD_RFSW
C16
0.1uF
10V
U3
6
VDD
OUT1
1
C17
DNI
8.2pF
50V
ANT0
J2
S
G3
G1
G2
RF_SW_IN
5
IN
OUT2
3
ANT1_ANT2
A-1JB
DNI
WL_GPIO_2
4
VCTL
GND
2
C9
8.2pF
50V
RTC7608
SON6H_0.35mm
Diversity Switch Truth Table
Anetnna Diversity
WL_GPIO_2
ANT1 (default)
0
ANT0
1
VDDUSB
VDD_RFSW
VBAT
R30
0 OHM
R37
0 OHM
DNI
Note: VDDUSB is used as this is the only fixed 3.3V rail
VBAT is provided as optional

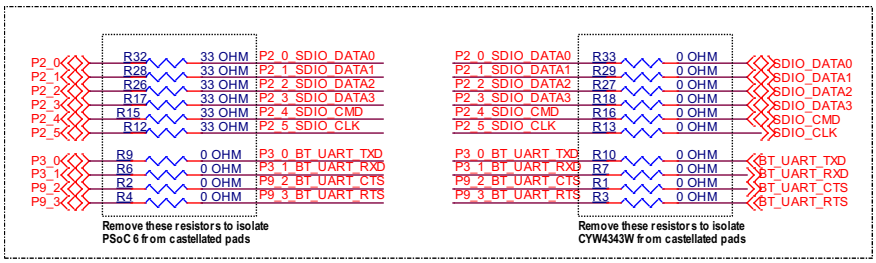


Carrier Module Footprint







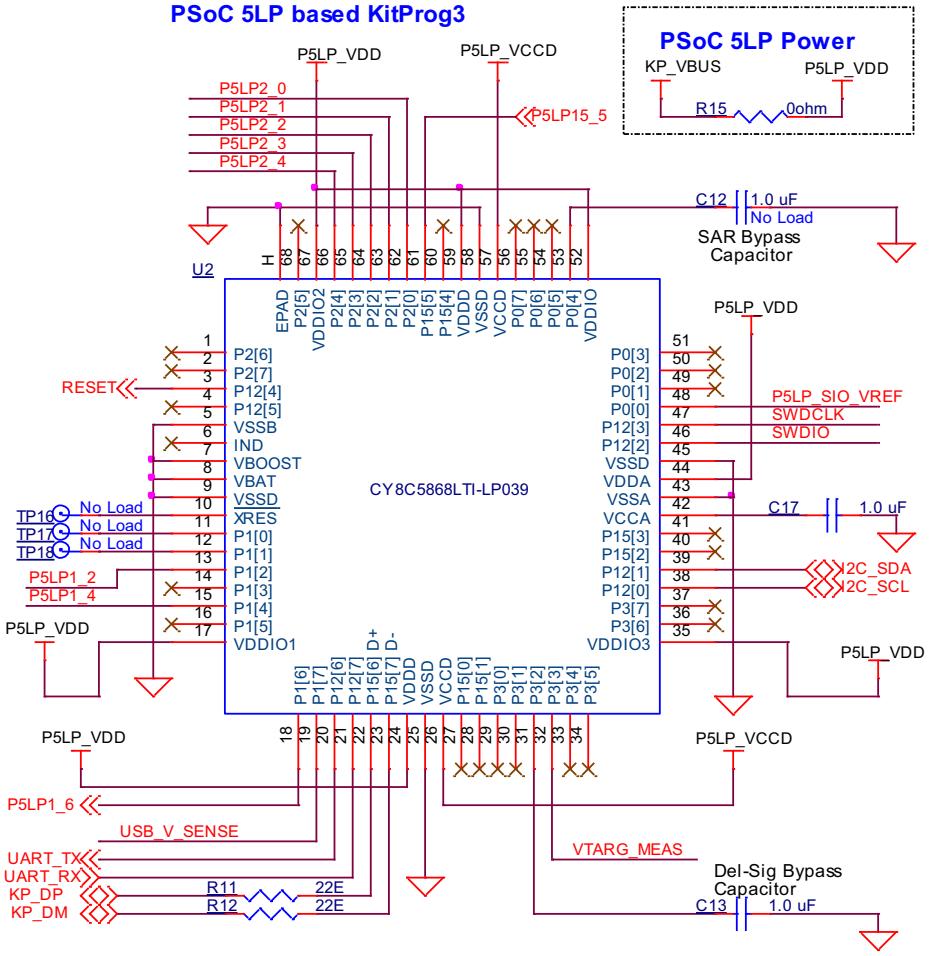


3.2.2 PSoC 5LP based KitProg3 (U2)

An onboard PSoC 5LP (CY8C5868LTI-LP039) is used as a KitProg3 to program and debug PSoC 6 MCU. The PSoC 5LP connects to the USB port of a PC through a USB connector and to the SWD and other communication interfaces of PSoC 6 MCU.

For more information, visit the PSoC 5LP webpage. Also, see the CY8C58LPxx Family datasheet.

Figure 3-2. Schematics of PSoC 5LP based KitProg3



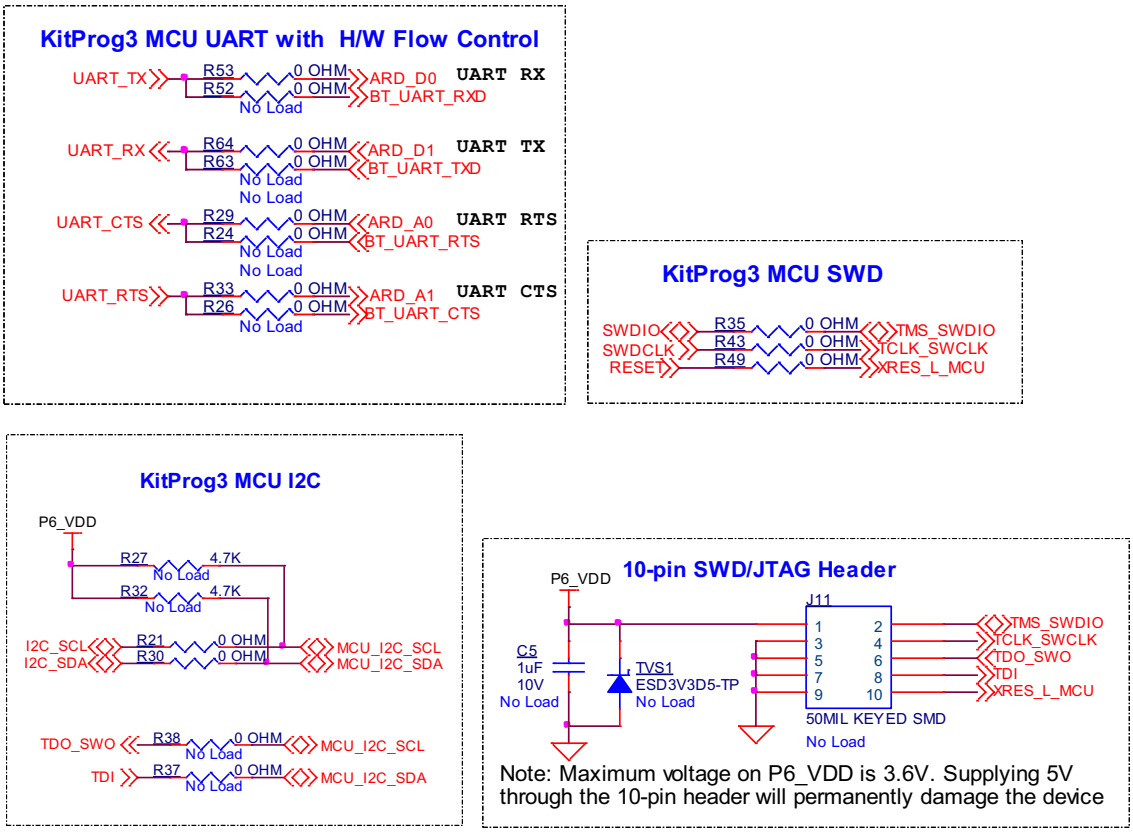
3.2.3 Serial Interconnection between PSoC 5LP and PSoC 6 MCU

In addition of use as an onboard programmer, the PSoC 5LP functions as an interface for the USB-UART and USB-I2C bridges, as shown in Figure 3-3. The USB-Serial pins of the PSoC 5LP are hard-wired to the I2C/UART pins of the PSoC 6 MCU. These pins are also available on the breadboard compatible I/O headers.

Note: The USB-UART bridge between KitProg3 and PSoC 6 MCU does not support UART hardware flow control by default. Populate R29 and R33 to enable this functionality.

The 10-pin header **J11** allows you to program and debug PSoC 6 MCU using an external programmer such as MiniProg4. This header has SWD enabled by default but can optionally support JTAG by removing R21, R30 and populating R37, R38 instead. Note that this will disconnect PSoC 6 MCU from KitProg3 USB-I2C bridge.

Figure 3-3. Schematics of Programming and Serial Interface Connections



3.2.3.1 BT UART

The board also has a provision to connect the BT core of CYW4343W to the KitProg3 USB-UART bridge. To do this, remove R53, R64, R29 and R33 and then load R52, R63, R24 and R26. When connecting to BT UART directly using an external USB-UART bridge or a KitProg3 that is separated from the board, please ensure to connect VTARG to the level translator's input pin of the external USB-UART bridge and GND to the corresponding ground pin of the external USB-UART bridge. This is to ensure proper level translation between the external USB-UART bridge and the CYW4343W.

3.2.4 Power Supply System

The power supply system on this board is versatile, allowing the input supply to come from the following sources:

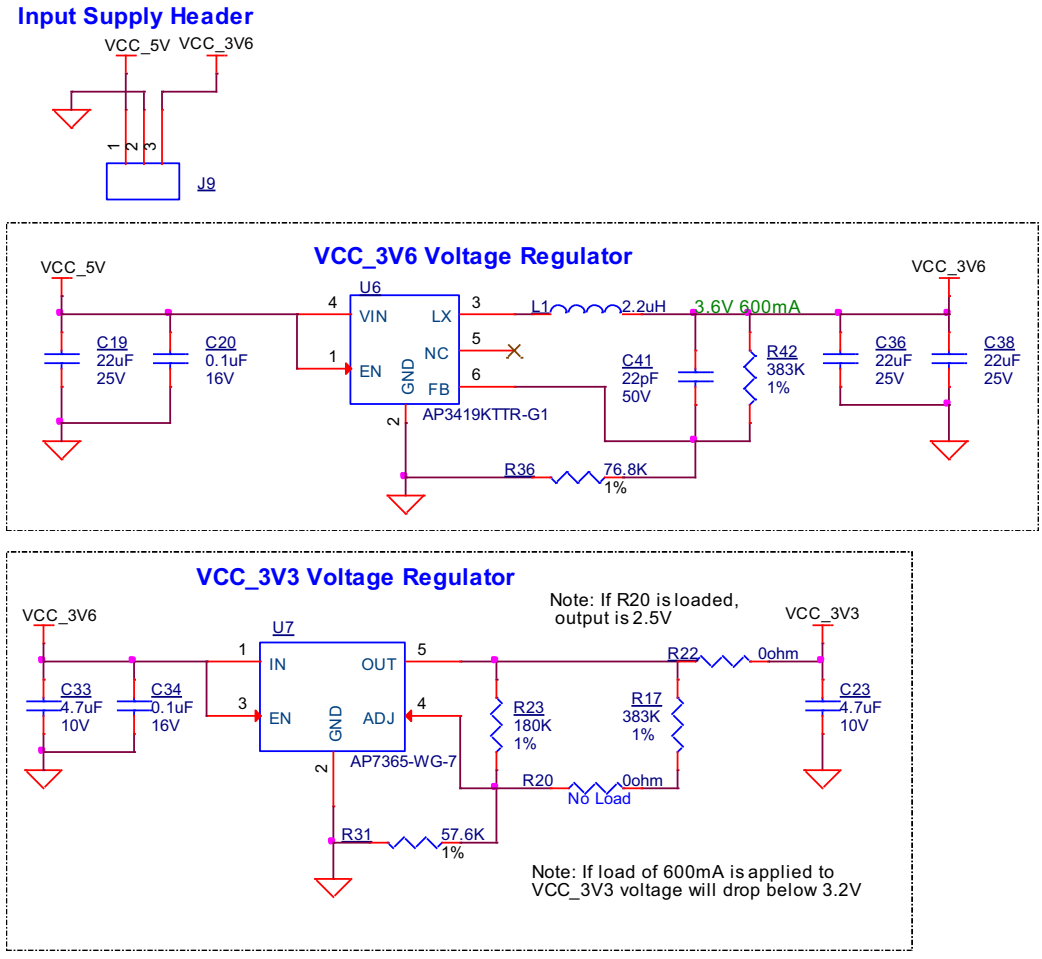
- 5 V from the onboard USB Micro-B connectors **(J8** and **J10)**
- 5 V from external power supply through VCC_5V at **J9.1**

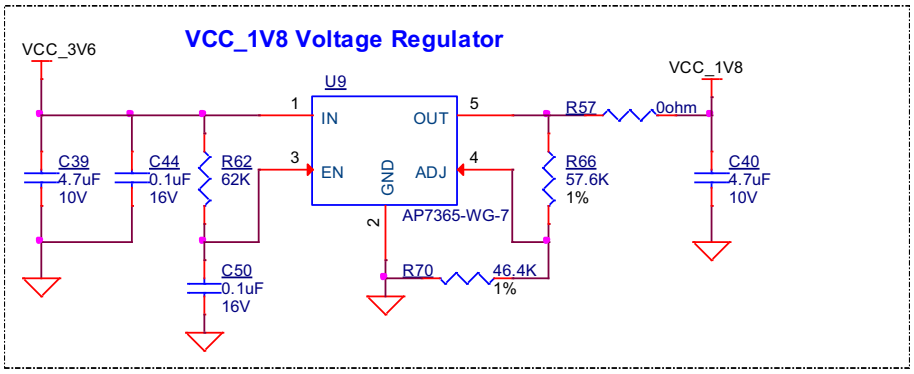
The power supply system is designed to support 1.8V to 3.3V operation of the PSoC 6 MCU. A voltage of 5V is provided from USB port and is required for the operation of KitProg3. There are three regulators used to achieve 3.6V, 3.3V, and 1.8V outputs - a buck regulator **(U6)** that generates a fixed 3.6V from an input of 5V, a fixed 3.3V regulator **(U7)** and a fixed 1.8V regulator **(U9)**. Both **U7** and **U9** are powered by VCC_3V6 produced by **U6**. Figure 3-4 shows the schematics of the voltage regulator and power selection circuits.

The voltage selection is made through jumper **(J3)**.

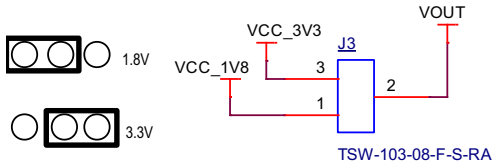
Note: VCC_3V3 can be optionally made to 2.5V for eFuse programming of PSoC 6 MCU by loading R20. Once completed it is expected that kit is reverted to 3.3V or 1.8V as operation of the board at 2.5V is not intended. VCC_3V3 powers the Quad SPI flash that requires voltage > 3 V and hence the flash will not function when VCC_3V3 is 2.5 V.

Figure 3-4. Schematics of Power Supply System

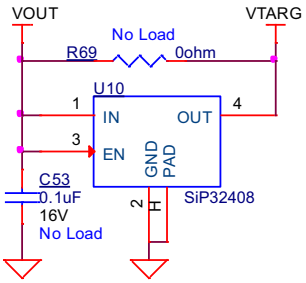




System Voltage Selection Header



Reverse Voltage Protection



3.2.4.1 *Current Measurement Headers*

The power supply is routed to the module pins through 0-ohm resistors and hence every domain powering CY8CMOD-062S3-4343W can be connected to an ammeter to measure current.

For PSoC 6 MCU core current measurement, **R59** must be removed and ammeter must be connected across VTARG **(J2.32)** and P6_VDD **(J2.31)**. Figure 3-5 shows the schematics of Module Power connections.

Figure 3-5. Schematics of Module Power connections

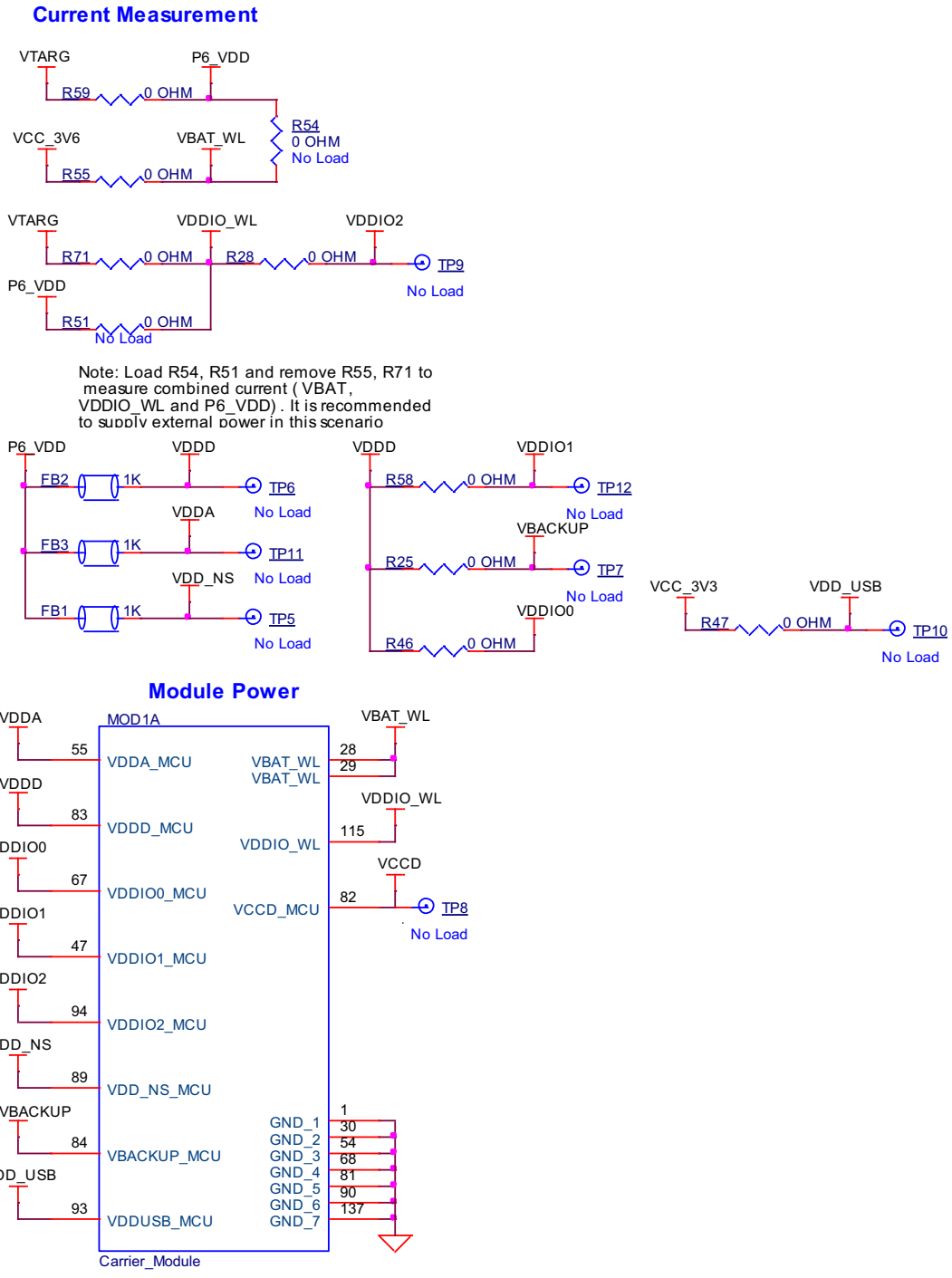


Figure 3-6. Location of Power Connection Resistors on the PSoC 62S3 Wi-Fi BT Prototyping Board

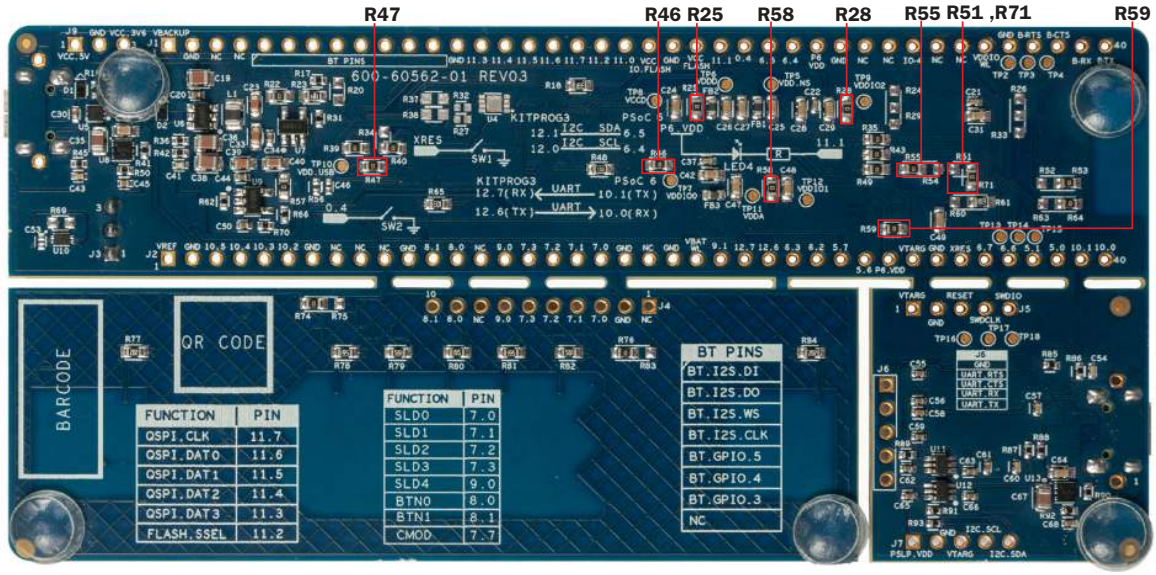


Table 3-1. Power Supply Pins

Voltage Source	Voltage Domain	Device Power Pins Powered by Domain	Operating Voltage Range		Supported Voltage	Voltage Selection Jumper
			Min (V)	Max (V)		
VCC_3V6	VBAT_WL	VBAT_WL	3.2	4.2	3.6V	N/A
VTARG	VDDIO_WL	VDDIO2, VDDIO_WL	1.7	3.6	1.8V, 3.3V	J3
VTARG	P6_VDD	VDDD, VDDIO0, VDDIO1, VDDA, VDD_NS, VBACKUP	1.7	3.6	1.8V, 3.3V	J3
VCC_3V3	VDD_USB	VDD_USB	1.7	3.6	3.3V	N/A

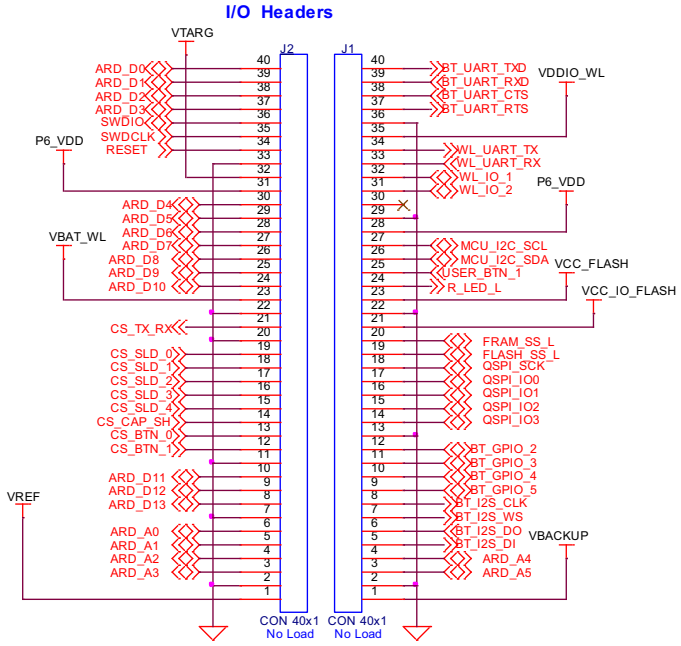
3.2.5 Expansion Connectors

3.2.5.1 I/O Headers (J1 and J2)

These headers provide connectivity to PSoC 6 MCU and CYW4343W GPIOs. Some of these pins are multiplexed with onboard peripherals like Quad SPI flash and CapSense slider and buttons.

The KitProg3 and CapSense functionality are contained in sections that can be broken away from the main (PSoC 6 MCU) section. To re-connect the individual sections, headers **J4** and **J5** are provided. These are not loaded by default.

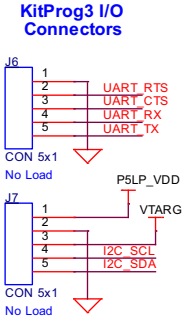
Figure 3-7. Schematics of I/O Headers (J1 and J2)



3.2.5.2 PSoC 5LP GPIO Headers (J6 and J7)

J6 and **J7** are 5x1 headers provided on the KitProg3 section of the board that bring out the USB-UART and USB-I2C bridge pins that can be used when the section is broken apart. Note that the RTS and CTS lines on these headers are from the voltage level translators (U11 and U12). **J6** and **J7** are not loaded by default.

Figure 3-8. Schematics of PSoC 5LP GPIO Headers (J6 and J7)

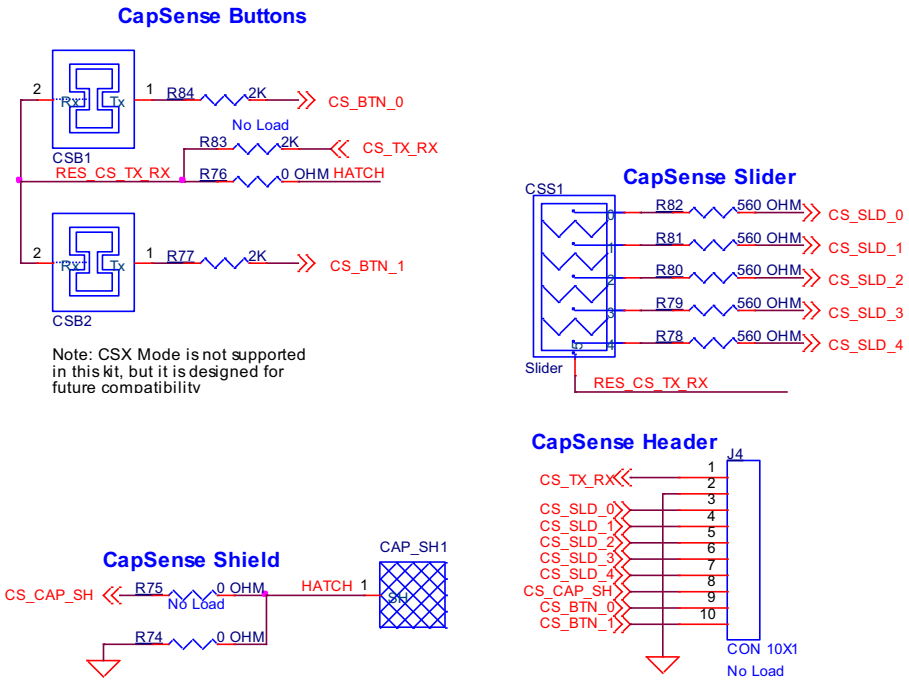


3.2.6 CapSense Circuit

The board supports a 5-segment CapSense slider and two buttons. The slider and buttons support only CSD sensing mode. An external capacitor, CMOD is provided on the CY8CMOD-062S3-4343W for CSD. For details on using CapSense including design guidelines, see the Getting Started with CapSense Design Guide.

The CapSense section can be broken away and re-connected to PSoC 6 MCU at **J2.12** to **J2.21** through **J4**.

Figure 3-9. Schematics of CapSense Circuit

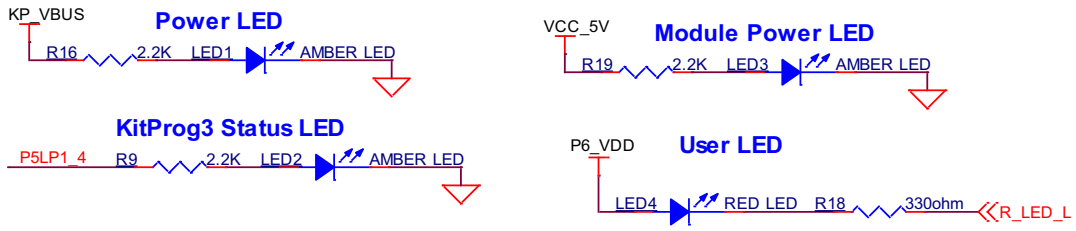


3.2.7 LEDs

LED2 (Amber) indicates the status of the KitProg3 (See the KitProg3 User Guide for details). **LED1** and **LED3** (Amber LEDs) indicates the status of power supplied to PSoC 5LP and PSoC 6 MCU respectively.

The board also has one user controllable LED **(LED4)** connected to PSoC 6 MCU pin P11[1] for user applications.

Figure 3-10. Schematics of LEDs

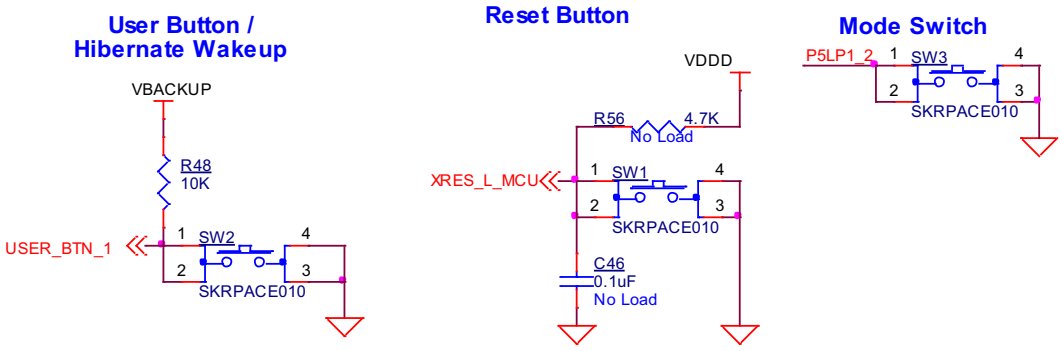


3.2.8 Push Buttons

The PSoC 62S3 Wi-Fi BT Prototyping Board has a reset button and 1 user button. The reset button **(SW1)** is connected to the XRES pin of the PSoC 6 MCU and is used to reset the device. One user button **(SW2)** is connected to pin P0[4] of the PSoC 6 MCU. In addition, the Mode selection button **SW3** is connected to the PSoC 5LP device for programming mode selection (Refer to the KitProg3 User Guide for details). All the buttons connect to ground on activation (active low).

The CY8CMOD-062S3-4343W provides pull-up for the XRES line of PSoC 6 MCU.

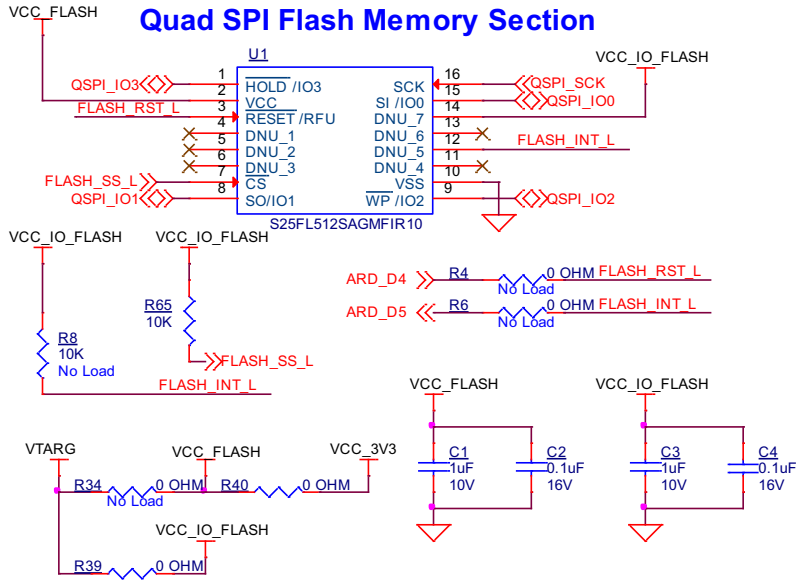
Figure 3-11. Schematics of Push Buttons



3.2.9 Cypress Quad SPI NOR Flash

The PSoC 62S3 Wi-Fi BT Prototyping Board has a Cypress NOR flash memory (S25FL512SAGMFIR10) of 512 Mbit capacity. The NOR Flash is connected to the Quad SPI interface of the PSoC 6 MCU. The NOR device can be used for both data and code memory with execute-in-place (XIP) support and encryption.

Figure 3-12. Schematics of QSPI Flash



3.3 Bill of Materials

Refer to the BOM files in the kit webpage.

3.4 Frequently Asked Questions

1. How does CY8CPROTO-062S3-4343W handle voltage connection when multiple power sources are plugged in?

   There are 3 different options to power the baseboard; KitProg3 Micro-B USB connector **(J8)**, PSoC 6 Micro-B USB connector **(J10)** and External DC supply via VCC_5V input header **(J9)**. The voltage from each of the USB connectors passes through a current limiting switch that also protects against reverse voltage. Optionally, P6_VDD can be supplied by an external programmer / debugger at J11. This is not loaded by default and is not recommended as not all peripherals will be powered.

2. What are the input voltage tolerances? Is there any overvoltage protection on this kit?

   Input voltage level are as follows:

Table 3-2. Input voltage levels

Supply	Typical I/P Voltage	Absolute max
USB Micro-B connector **(J8, J10)**	4.5 V to 5.5 V	5.5 V
Input Supply Header **(J9)**	5 V to 5.5 V	6 V
Program and Debug header **(J11)**	1.8 V to 3.3 V	3.6 V

   There is no overvoltage protection on this kit.

3. Why is the voltage of the kit restricted to 3.3 V? Can't it drive external 5 V interfaces?

   PSoC 6 MCU is not meant to be operated at voltages greater than 3.6 V. Hence, it cannot drive I/O system with > 3.6 V supply voltages. Powering PSoC 6 MCU to more than 4 V will damage the chip.

4. I am unable to program the target device.
   a. Check J3 to ensure that a jumper shunt is placed.
   b. Make sure that no external devices are connected to J2.32 to J2.36.
   c. Update your KitProg3 version to the latest version using the steps mentioned in the KitProg3 User Guide.
   d. Ensure that target device used in the IDE application is CY8C6245LQI-S3D72.

5. Does the kit get powered when I power the kit from another Cypress kit through the **J9** header?

   Yes, VIN pin on **J9** header is a supply input/output pin and can take up to 5.5V.

6. What additional overlays can be used with the CapSense?

   Any kind of overlays (up to 5 mm thickness) like wood, acrylic, and glass can be used with this CapSense. Note that additional tuning may be required when the overlay is changed.

7. Can I use this kit as a programmer to program external PSoC devices?

   Yes, the onboard KitProg3 can program any PSoC 4/5/6 devices connected to **J5** header, once it is broken away from the PSoC 6 MCU section of the board.

8. Which third-party IDEs does this Kit support?

   Multiple third-party IDEs are supported; IAR and µVision are some examples. For more details on all supported devices and procedures to export to these IDEs, see AN225588 - Using ModusToolbox Software with a Third-Party IDE.

Revision History

Document Revision History

Document Title: CY8CPROTO-062S3-4343W PSoC 62S3 Wi-Fi BT Prototyping Kit Guide Document Number: 002-28070			
Revision	**ECN Number**	**Issue Date**	**Description of Change**
**	6669459	10/11/2019	New kit guide.
*A	6753753	12/27/2019	Updated Safety and Regulatory Compliance Information chapter on page 4: Updated description. Updated Introduction chapter on page 8: Updated “Kit Contents” on page 9: Updated Figure 1-1. Updated “Board Details” on page 11: Updated Figure 1-2. Updated Table 1-1. Updated Kit Operation chapter on page 16: Updated “Theory of Operation” on page 16: Updated description. Updated hyperlinks in required places. Updated Figure 2-4. Updated “KitProg3: On-Board Programmer/Debugger” on page 20: Updated “Programming and Debugging using ModusToolbox IDE” on page 20: Updated Figure 2-5. Updated “Using the OOB Example – PSoC 6 MCU: Hello World” on page 23 (Updated description; added hyperlinks in required places). Updated “USB-UART Bridge” on page 24: Updated Figure 2-13 (Updated caption only). Updated “USB-I2C Bridge” on page 24: Updated Figure 2-14 (Updated caption only). Updated Hardware chapter on page 25: Updated “Hardware Functional Description” on page 25: Updated “Power Supply System” on page 31: Updated “Current Measurement Headers” on page 33 (Updated Figure 3-6 (Updated caption only); updated Table 3-1). Updated “Frequently Asked Questions” on page 38: Updated description. Updated Table 3-2.