September 2008

FAN5361
6MHz, 600mA TinyBuck™ Synchronous Buck Regulator

Features

- 6MHz Fixed-Frequency Operation
- 35µA Typical Quiescent Current
- Best-in-Class Load Transient
- 600mA Output Current Capability
- 2.3V to 5.5V Input Voltage Range
- 1.0 to 1.82V Fixed Output Voltage
- Low Ripple Light-Load PFM Mode
- Forced PWM and External Clock Synchronization
- Internal Soft-Start
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 6-bump WLCSP, 0.4mm Pitch
- 6-pin 2 x 2mm UMLP

Applications

- Cell Phones
- Portable Media Players
- WLAN, 3G, and 4G Data Cards

Description

The FAN5361 is a 600mA, step-down, switching voltage regulator that delivers a fixed output from an input voltage supply of 2.3V to 5.5V. Using a proprietary architecture with synchronous rectification, the FAN5361 is capable of delivering a peak efficiency of 92%, while maintaining efficiency over 80% at load currents as low as 1mA.

The regulator operates at a nominal fixed frequency of 6MHz, which reduces the value of the external components to 470nH for the output inductor and 4.7µF for the output capacitor. The PWM modulator can be synchronized to an external frequency source.

At moderate and light loads, pulse frequency modulation is used to operate the device in power-save mode with a typical quiescent current of 35µA. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 6MHz. In shutdown mode, the supply current drops below 1µA, reducing power consumption. For applications that require minimum ripple or fixed frequency, PFM mode can be disabled using the MODE pin.

The FAN5361 is available in 6-bump, 0.4mm pitch, Wafer-Level Chip-Scale Package (WLCSP) and a 6-lead 2 x 2mm ultra-thin MLP package.

Typical Applications

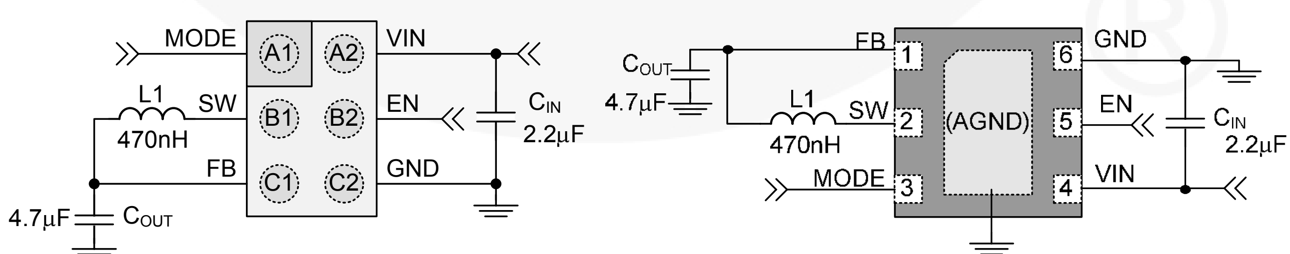

Figure 1. Typical Applications

Ordering Information

Part Number	Output Voltage[(1)]	Package	Eco Status	Temperature Range	Packing
FAN5361UC10X[(2)]	1.0V	WLCSP-6 0.4mm Pitch	Green	–40 to +85°C	Tape and Reel
FAN5361UC12X	1.2V				
FAN5361UC13X[(2)]	1.3V				
FAN5361UC15X[(2)]	1.5V				
FAN5361UC18X[(2)]	1.8V				
FAN5361UC182X	1.82V				
FAN5361UMP10X[(2)]	1.0V	6 Lead UMLP 2 x 2mm	RoHS	–40 to +85°C	Tape and Reel
FAN5361UMP12X[(2)]	1.2V				
FAN5361UMP13X[(2)]	1.3V				
FAN5361UMP15X[(2)]	1.5V				
FAN5361UMP18X[(2)]	1.8V				

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Notes:
1. Other voltage options available on request. Contact a Fairchild representative.
2. Preliminary release.

Pin Configuration

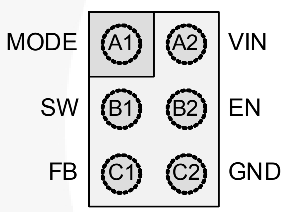

Figure 2. WLCSP, Bumps Facing Down

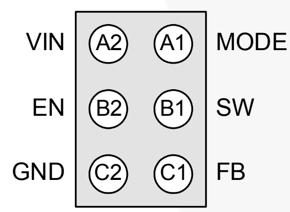

Figure 3. WLCSP, Bumps Facing Up

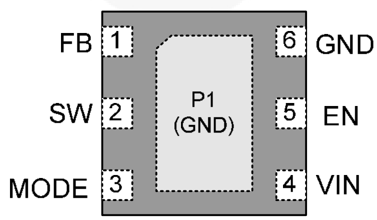

Figure 4. UMLP, Leads Facing Down

Pin Definitions

Pin #		Name	Description
WLCSP	MLP		
A1	3	MODE	**MODE**. Logic 1 on this pin forces the IC to stay in PWM mode. A logic 0 allows the IC to automatically switch to PFM during light loads. The regulator also synchronizes its switching frequency to four times the frequency provided on this pin. Do not leave this pin floating.
B1	2	SW	**Switching Node**. Connect to output inductor.
C1	1	FB	**Feedback / VOUT**. Connect to output voltage.
C2	6	GND	**Ground**. Power and IC ground. All signals are referenced to this pin.
B2	5	EN	**Enable**. The device is in shutdown mode when voltage to this pin is <0.4V and enabled when >1.2V. Do not leave this pin floating.
A2	4	VIN	**Input Voltage**. Connect to input power source.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Units
V_{IN}	Input Voltage		–0.3	7.0	V
V_{SW}	Voltage on SW Pin		–0.3	V_{IN} + 0.3[(3)]	V
V_{CTRL}	EN and MODE Pin Voltage		–0.3	V_{IN} + 0.3[(3)]	V
	Other Pins		–0.3	V_{IN} + 0.3[(3)]	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	4		kV
		Charged Device Model per JESD22-C101	1.5		kV
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:
3. Lesser of 7V or V_{IN}+0.3V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage Range	2.3		5.5	V
I_{OUT}	Output Current	0		600	mA
L	Inductor		0.47		µH
C_{IN}	Input Capacitor		2.2		µF
C_{OUT}	Output Capacitor		4.7		µF
T_A	Operating Ambient Temperature	–40		+85	°C
T_J	Operating Junction Temperature	–40		+125	°C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 1s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate T_A.

Symbol	Parameter		Typical	Units
θ_{JA}	Junction-to-Ambient Thermal Resistance	WLCSP	150	°C/W
		MLP	49	°C/W

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Electrical Characteristics

Minimum and maximum values are at V_{IN} = V_{EN} = 2.3V to 5.5V, AUTO Mode, T_A = -40°C to +85°C; circuit of Figure 1, unless otherwise noted. Typical values are at T_A = 25°C, V_{IN} = V_{EN} = 3.6V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies						
I_Q	Quiescent Current	No load, Not Switching		35	55	µA
		PWM Mode		6		mA
$I_{(SD)}$	Shutdown Supply Current	V_{IN} = 3.6V, EN = GND		0.05	1.00	µA
V_{UVLO}	Under-Voltage Lockout Threshold	Rising V_{IN}		2.15	2.25	V
V_{UVHYST}	Under-Voltage Lockout hysteresis			150		mV
$V_{(ENH)}$	Enable HIGH-Level Input Voltage		1.2			V
$V_{(ENL)}$	Enable LOW-Level Input Voltage				0.4	V
$I_{(EN)}$	Enable Input Leakage Current	EN to V_{IN} or GND		0.01	1.00	µA
$V_{(MH)}$	MODE HIGH-Level Input Voltage		1.2			V
$V_{(ML)}$	MODE LOW-Level Input Voltage				0.4	V
$I_{(M)}$	MODE Input Leakage Current	MODE to V_{IN} or GND		0.01	1.00	µA
Switching and Synchronization						
f_{SW}	Switching Frequency	V_{IN} = 3.6V, T_A = 25°C	5.4	6.0	6.6	MHz
f_{SYNC}	MODE Synchronization Range[4]	Squarewave at MODE Input	1.3	1.5	1.7	MHz
Regulation						
V_O	Output Voltage Accuracy, 1.82V	I_{LOAD} = 0 to 600mA	1.784	1.820	1.875	V
	1.82V	PWM Mode	1.784	1.820	1.856	V
	1.80V	I_{LOAD} = 0 to 600mA	1.764	1.800	1.854	V
	1.80V	PWM Mode	1.764	1.800	1.836	V
	1.50V	I_{LOAD} = 0 to 600mA	1.470	1.500	1.545	V
	1.50V	PWM Mode	1.470	1.500	1.530	V
	1.30V	I_{LOAD} = 0 to 600mA	1.274	1.300	1.339	V
	1.30V	PWM Mode	1.274	1.300	1.326	V
	1.20V	I_{LOAD} = 0 to 600mA	1.174	1.200	1.239	V
	1.20V	PWM Mode	1.174	1.200	1.226	V
	1.00V	I_{LOAD} = 0 to 600mA	0.974	1.000	1.039	V
	1.00V	PWM Mode	0.974	1.000	1.026	V
t_{SS}	Soft-Start	From EN Rising Edge		150	300	µs
Output Driver						
$R_{DS(on)}$	PMOS On Resistance	V_{IN} = V_{GS} = 3.6V		350		mΩ
	NMOS On Resistance	V_{IN} = V_{GS} = 3.6V		225		mΩ
I_{LIM}	PMOS Peak Current Limit	Open-Loop	900	1000	1250	mA
T_{TSD}	Thermal Shutdown	CCM Only		150		°C
T_{HYS}	Thermal Shutdown Hysteresis			15		°C

Notes:

4. Limited by the effect of t_{OFF} minimum *(see Figure 13 in Typical Performance Characteristics)*.

Typical Performance Characteristics

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6V$, $V_{MODE} = 0V$, $V_{OUT} = 1.82V$, $T_A = 25°C$.

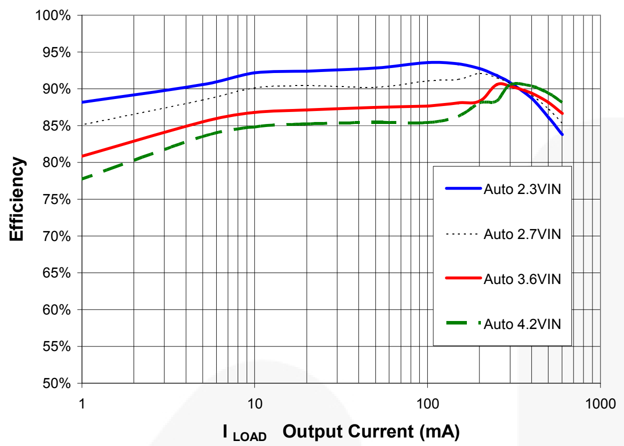

Figure 5. Efficiency vs. Load Current vs. Input Supply

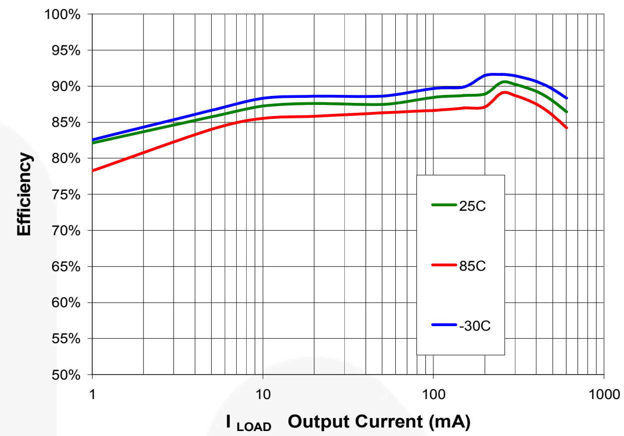

Figure 6. Efficiency vs. Load Current vs. Temperature

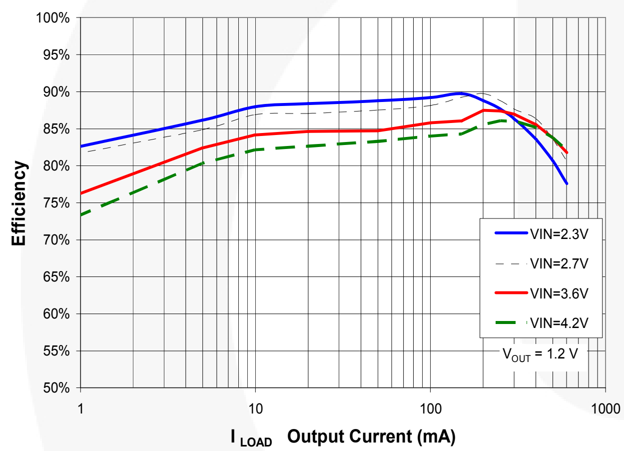

Figure 7. Efficiency vs. Load Current vs. Input Supply

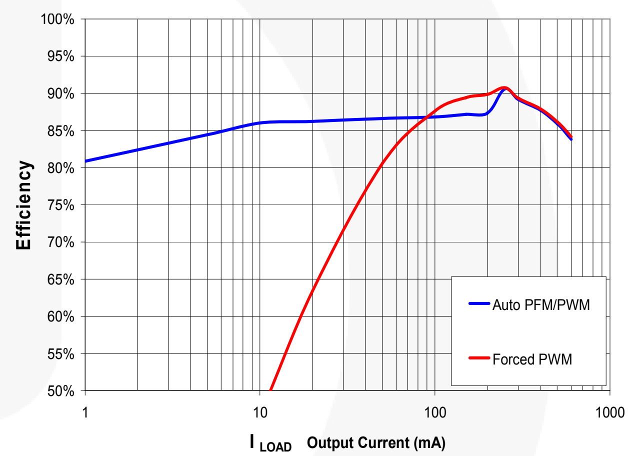

Figure 8. Efficiency, Auto PWM/PFM vs. Forced PWM

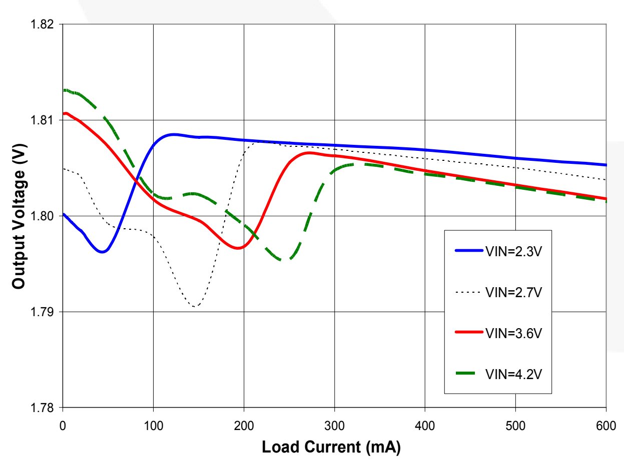

Figure 9. Load Regulation vs. Input Supply

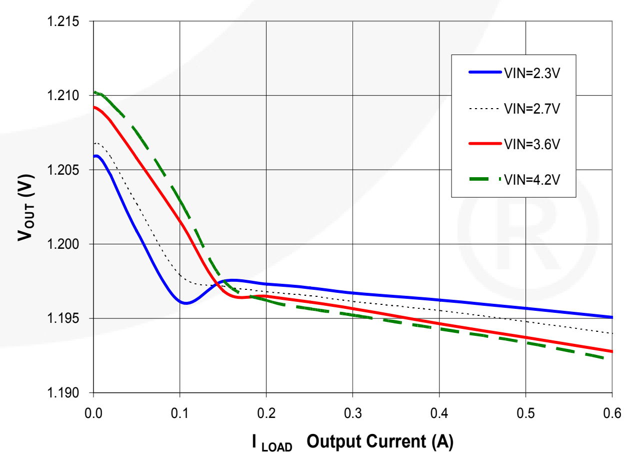

Figure 10. 1.2V_{OUT} Load Regulation vs. Input Supply

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6V$, $V_{MODE} = 0V$, $V_{OUT} = 1.82V$, $T_A = 25°C$.

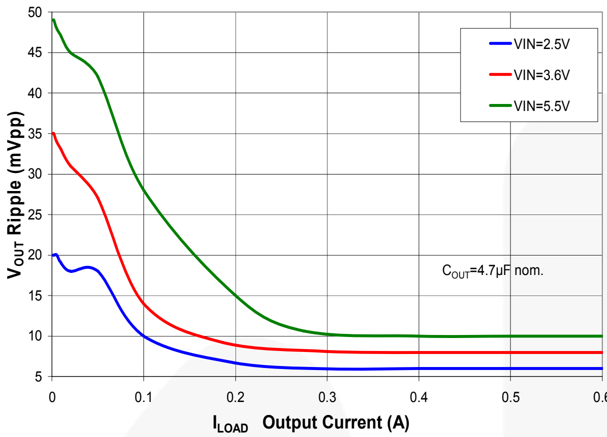

Figure 11. Peak-to-Peak Output Voltage Ripple

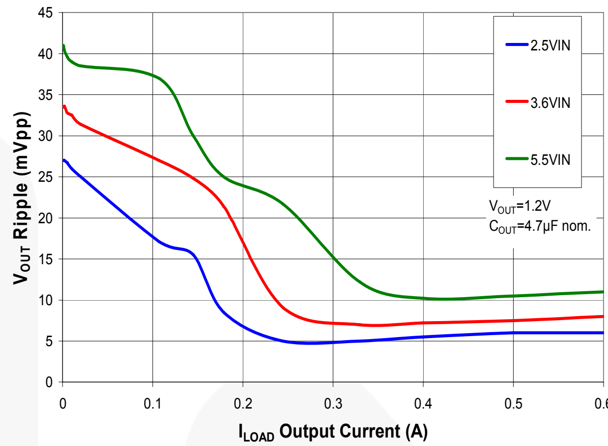

Figure 12. 1.2V_{OUT} Peak-to-Peak Output Voltage Ripple

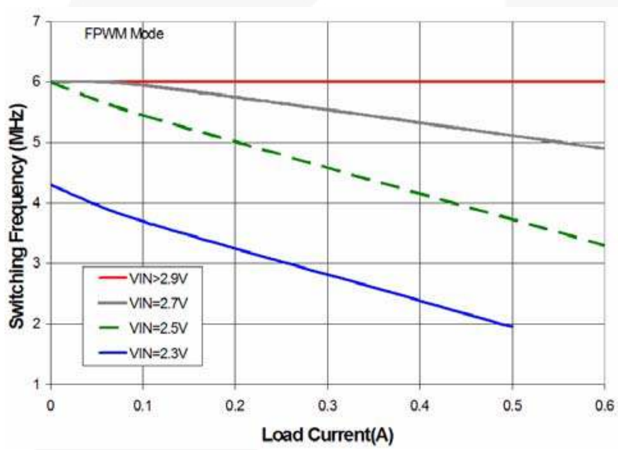

Figure 13. Effect of $t_{OFF(MIN)}$ on Switching Frequency

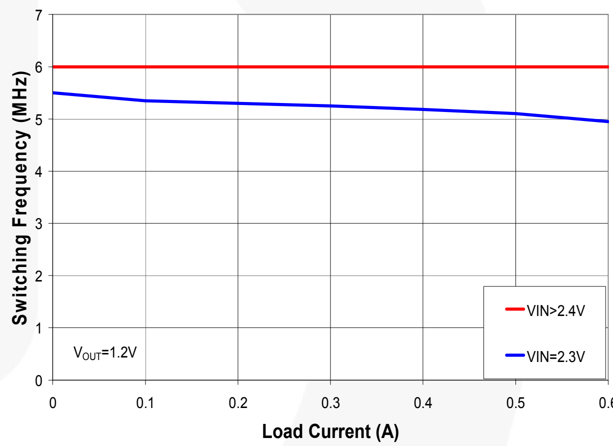

Figure 14. 1.2V_{OUT} Effect of $t_{OFF(MIN)}$ on Switching Frequency

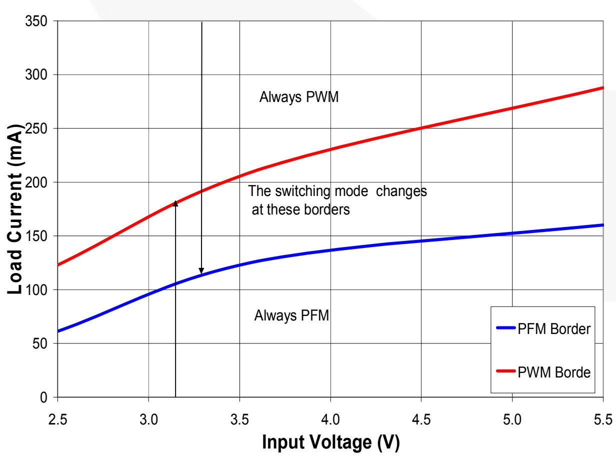

Figure 15. PFM / PWM Boundaries

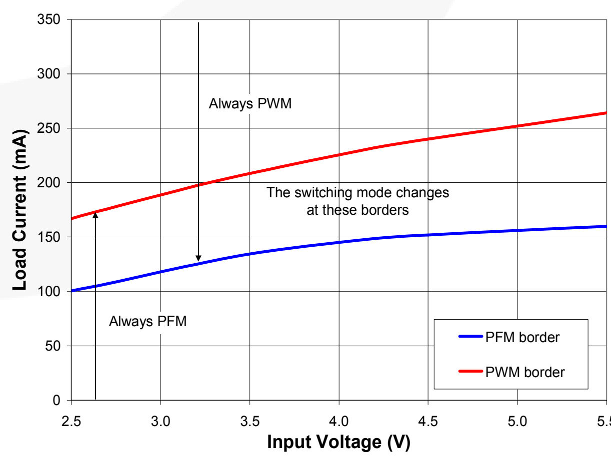

Figure 16. 1.2V_{OUT} PFM / PWM Boundaries

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6V$, $V_{MODE} = 0V$, $V_{OUT} = 1.82V$, $T_A = 25°C$.

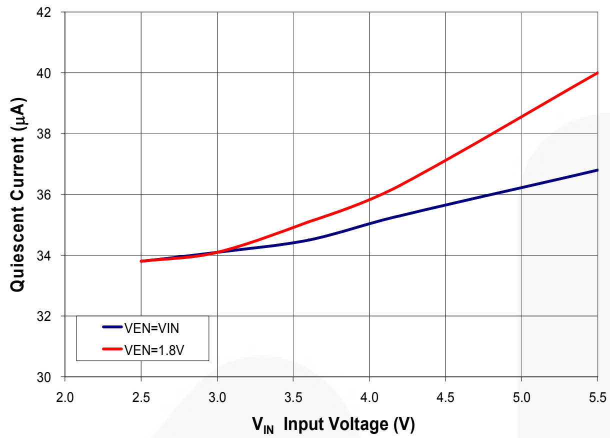

Figure 17. Quiescent Curent vs. Input Voltage

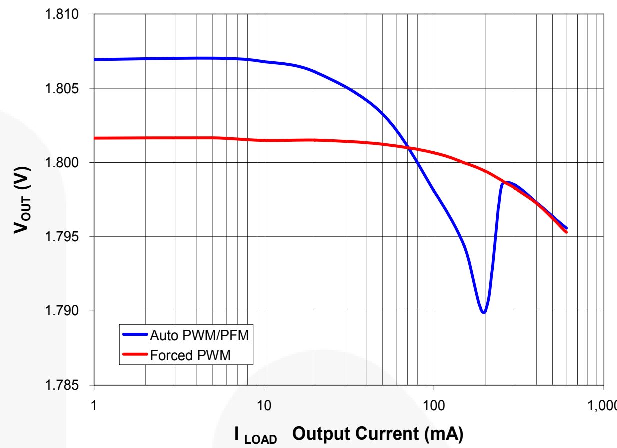

Figure 18. Load Regulation, Auto PFM / PWM and Forced PWM

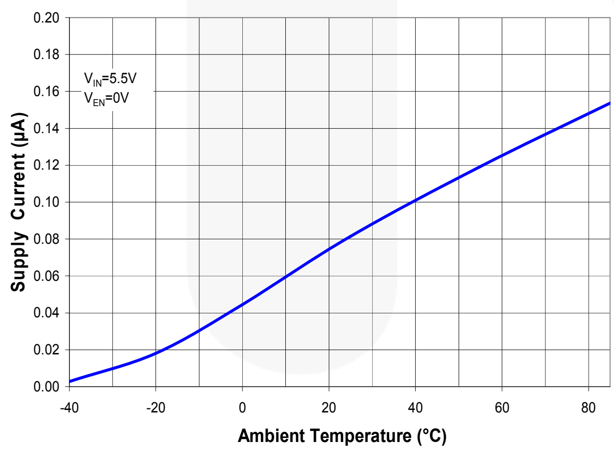

Figure 19. Shutdown Current vs. Temperature

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6V$, $V_{MODE} = 0V$, $V_{OUT} = 1.82V$, $T_A = 25°C$, 5µs/div. horizontal sweep.

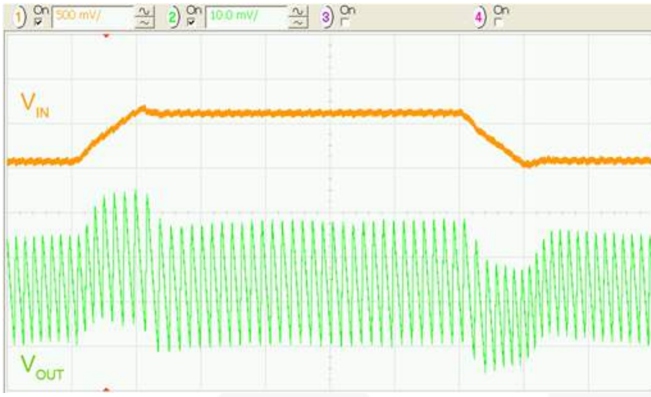

Figure 20. Line Transient $3.3V_{IN}$ to $3.9V_{IN}$, 50mA Load, 10µs/div.

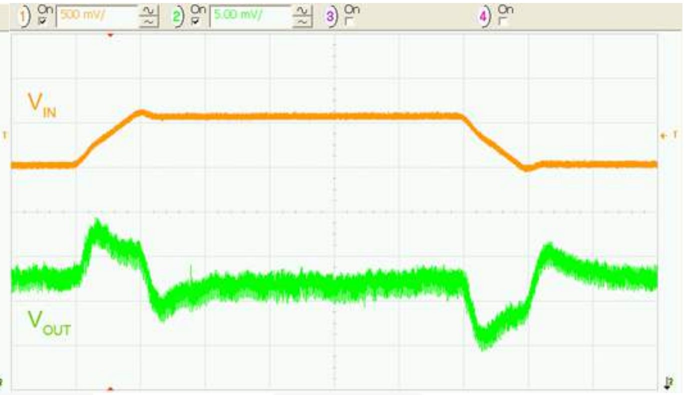

Figure 21. Line Transient $3.3V_{IN}$ to $3.9V_{IN}$, 250mA Load, 10µs/div.

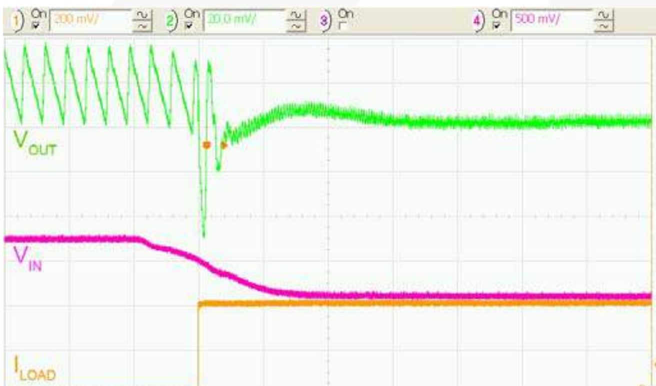

Figure 22. Combined Line/Load Transient 3.3 to $3.9V_{IN}$ Combined with 400mA to 40mA Load Transient

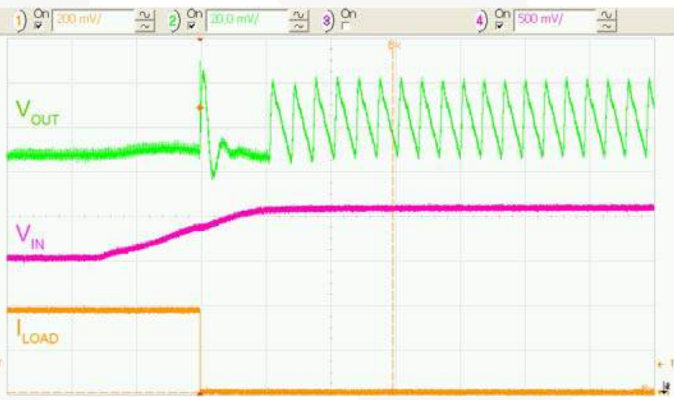

Figure 23. Combined Line/Load Transient 3.9 to $3.3V_{IN}$ Combined with 400mA to 40mA Load Transient

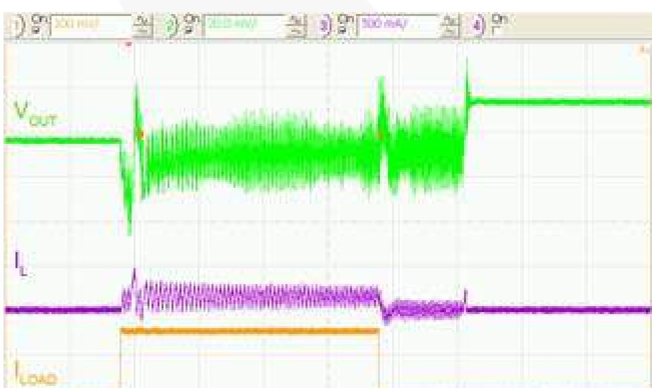

Figure 24. Load Transient 0 to 150mA, $2.5V_{IN}$

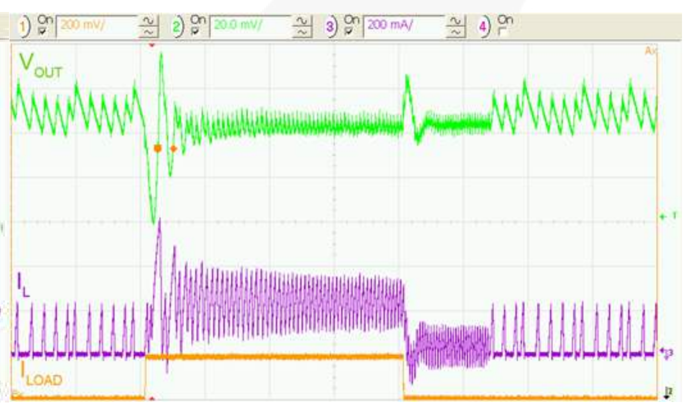

Figure 25. Load Transient 50 to 250mA, $2.5V_{IN}$

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6V$, $V_{MODE} = 0V$, $V_{OUT} = 1.82V$, $T_A = 25°C$, 5µs/div. horizontal sweep.

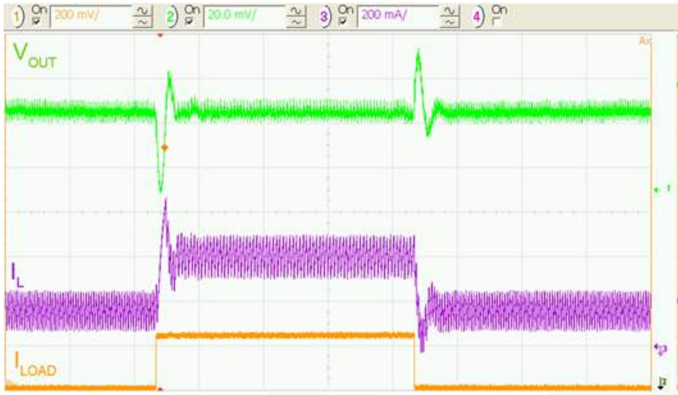

Figure 26. Load Transient 150 to 400mA, 2.5V_{IN}

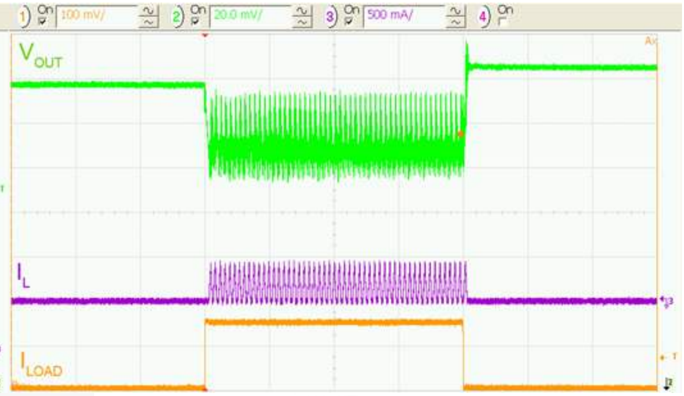

Figure 27. Load Transient 0 to 150mA, 3.6V_{IN}

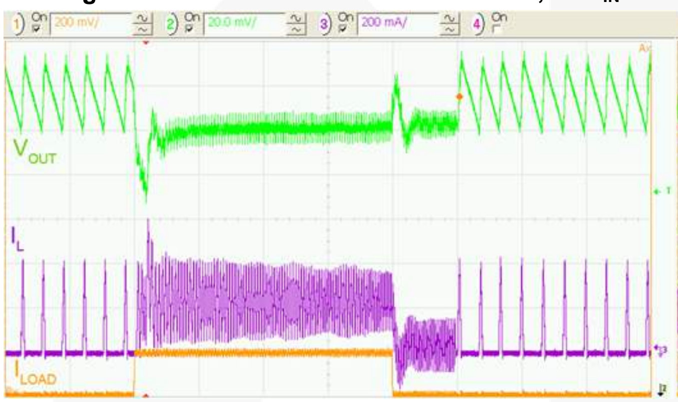

Figure 28. Load Transient 50 to 250mA, 3.6V_{IN}

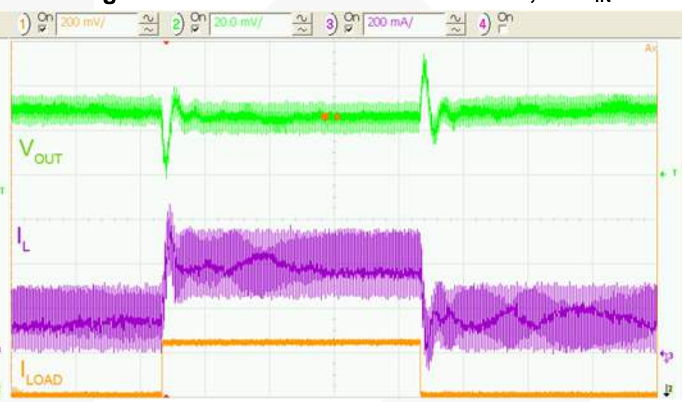

Figure 29. Load Transient 150 to 400mA, 3.6V_{IN}

Figure 30. Load Transient 0 to 150mA, 4.5V_{IN}

Figure 31. Load Transient 50 to 250mA, 4.5V_{IN}

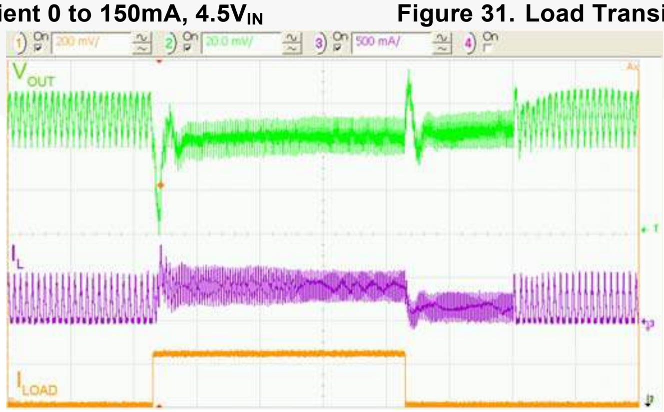

Figure 32. Load Transient 150 to 400mA, 4.5VIN

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6V$, $V_{MODE} = 0V$, $V_{OUT} = 1.82V$, $T_A = 25°C$, 5µs/div. horizontal sweep.

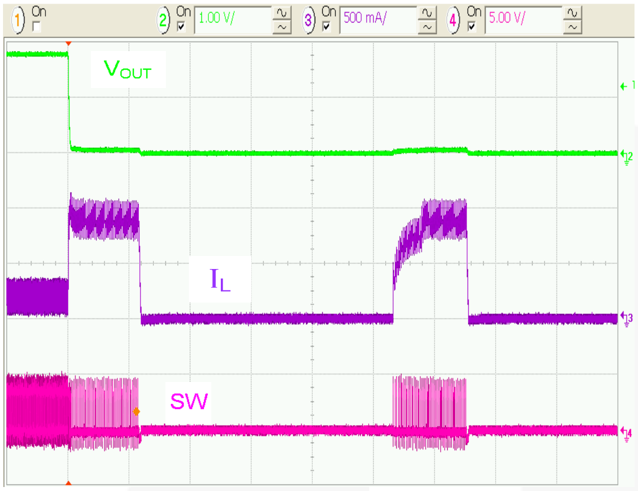

Figure 33. Metallic Short Applied at V_{OUT}, 20µs/div.

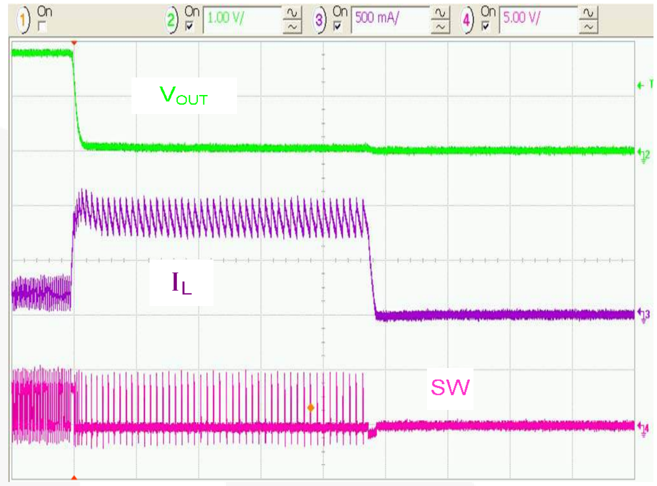

Figure 34. Metallic Short Applied at V_{OUT}

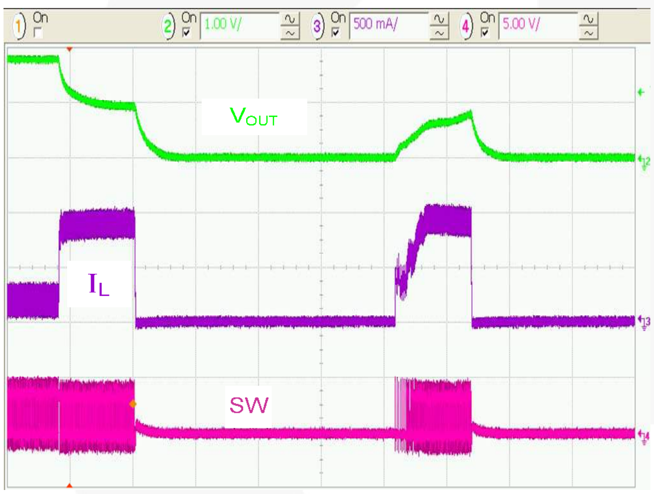

Figure 35. Over-Current Fault Response, R_{LOAD} = 1Ω, 20µs/div.

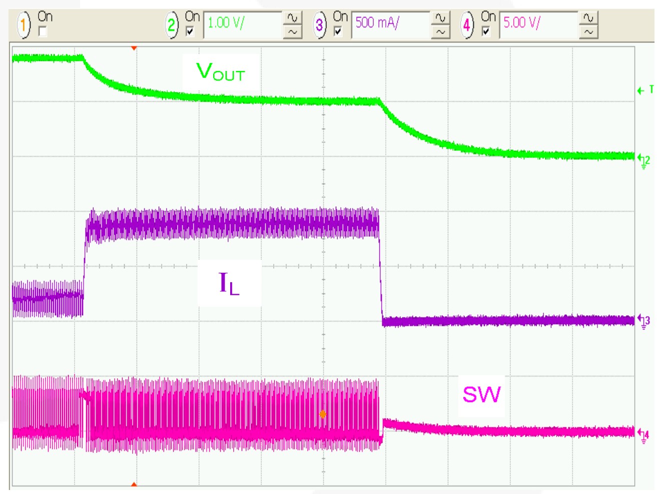

Figure 36. Over-Current Fault Response, R_{LOAD} = 1Ω

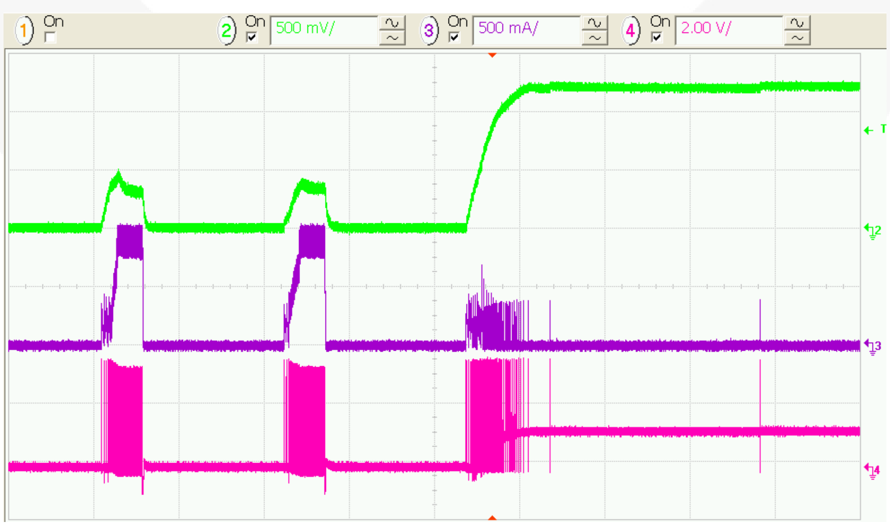

Figure 37. 1.2V_{OUT} Overload Recovery to Light Load

Typical Performance Characteristics (Continued)

Unless otherwise noted, $V_{IN} = V_{EN} = 3.6V$, $V_{MODE} = 0V$, $V_{OUT} = 1.82V$, $T_A = 25°C$.

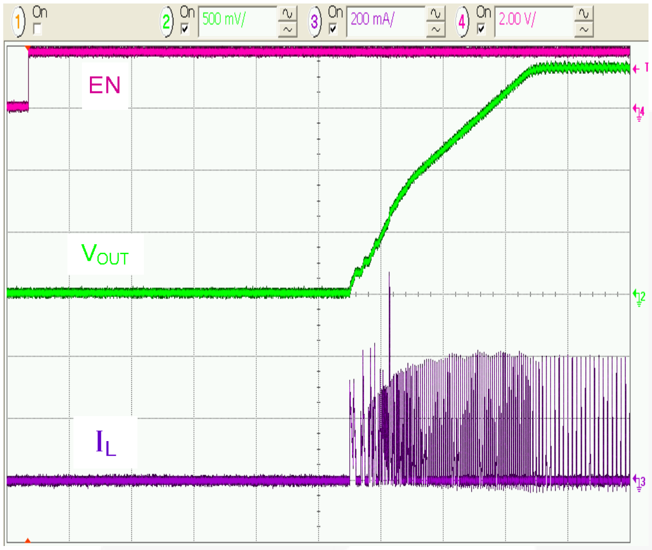

Figure 38. Soft-Start, $R_{LOAD} = 50\Omega$, 20µs/div.

Figure 39. SW-Node Jitter (Infinite Persistence), I_{LOAD} = 200mA, 50ns/div.

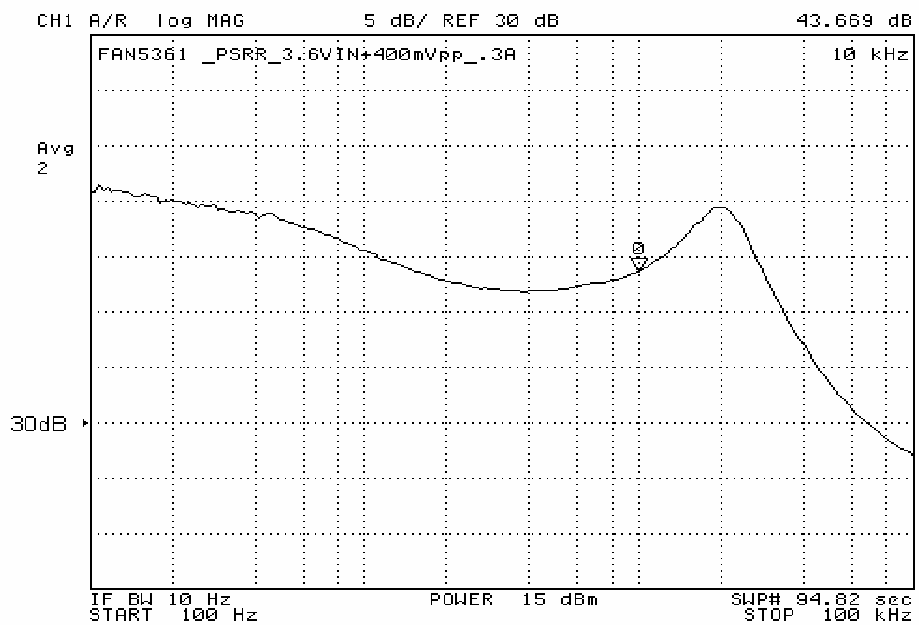

Figure 40. Power Supply Rejection Ratio at 300mA Load

Operation Description

The FAN5361 is a 600mA, step-down, switching voltage regulator that delivers a fixed output from an input voltage supply of 2.3V to 5.5V. Using a proprietary architecture with synchronous rectification, the FAN5361 is capable of delivering a peak efficiency of 92%, while maintaining efficiency over 80% at load currents as low as 1mA. The regulator operates at a nominal frequency of 6MHz at full load, which reduces the value of the external components to 470nH for the inductor and 4.7µF for the output capacitor.

Control Scheme

The FAN5361 uses a proprietary, non-linear, fixed-frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN5361 operates in discontinuous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is seamless, with a glitch of less than 18mV at V_{OUT} during the transition between DCM and CCM modes.

Combined with exceptional transient response characteristics, the very low quiescent current of the controller (35µA) maintains high efficiency; even at very light loads, while preserving fast transient response for applications requiring tight output regulation.

Enable and Soft-Start

Maintaining the EN pin LOW keeps the FAN5361 in non-switching mode, in which all circuits are off and the part draws ~50nA of current. Increasing EN above its threshold voltage activates the part and starts the soft-start cycle. The output ramp during soft-start is a fixed slew rate of 50mV/µs from 0 to $1V_{OUT}$, then 25mV/µs for $1.82V_{OUT}$ or 12mV/µs for $1.2V_{OUT}$ until the output reaches its setpoint.

MODE pin

Logic 1 on this pin forces the IC to stay in PWM mode. A logic 0 allows the IC to automatically switch to PFM during light loads. If the MODE pin is toggled, the converter synchronizes its switching frequency to four times the frequency on the mode pin (f_{MODE}). The mode pin must be held LOW for at least 10µs or HIGH for 10µs to ensure that the converter does not attempt to synchronize to this pin.

Current Limit, Fault Shutdown, and Restart

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching this point, the high-side switch turns off, preventing high currents from causing damage. The regulator continues to limit the current cycle-by-cycle. After 21µs of current limit, the regulator triggers an over-current fault, causing the regulator to shut down for about 86µs before attempting a restart.

If the fault was caused by short circuit, the soft-start circuit attempts to restart at 33% of normal current limit and produces an over-current fault after about 21µs, which results in a duty cycle of less than 25% providing current into a short.

Under-Voltage Lockout (UVLO)

When EN is high, the under-voltage lock-out keeps the part from operating until the input supply voltage rises high enough to properly operate. This ensures no misbehavior of the regulator during start-up or shutdown.

Thermal Shutdown (TSD)

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the output switching is disabled until the temperature on the die has fallen sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 15°C hysteresis.

Minimum Off-Time Effect on Switching Frequency

$t_{OFF(MIN)}$ is 50ns. This imposes constraints on the maximum $\frac{V_{OUT}}{V_{IN}}$ that the FAN5361 can provide, while maintaining a fixed switching frequency in PWM mode.

$$\frac{V_{OUT}}{V_{IN}} \le 1 - t_{OFF(MIN)} \bullet f_{SW} \approx 0.7$$

$$f_{SW} \approx \frac{V_{IN} - V_{OUT}}{50ns \bullet V_{IN}}$$

The switching frequency drops when the regulator cannot provide sufficient duty cycle at 6Mhz to maintain regulation. This occurs when V_{OUT} is 1.8V or 1.82V and V_{IN} is below 3V at high load currents *(see Figure 13)*.

The calculation for switching frequency is given by:

$$f_{SW} = \min\left(\frac{1}{t_{SW(MAX)}}, \frac{1}{166.6ns}\right) \quad (1)$$

where:

$$t_{SW(MAX)} = 50ns \bullet \left(1 + \frac{V_{OUT} + I_{OUT} \bullet R_{OFF}}{V_{IN} - I_{OUT} \bullet R_{ON} - V_{OUT}}\right) \quad (2)$$

where:

$$R_{OFF} = R_{DSON\_N} + DCR_L$$

$$R_{ON} = R_{DSON\_P} + DCR_L$$

Applications Information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy handling capability of the application. The inductor value affects average current limit, the PWM-to-PFM transition point, output voltage ripple, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}} \right) \quad (3)$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$ by the ripple current, given by:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad (4)$$

The transition between PFM and PWM operation is determined by the point at which the inductor valley current crosses zero. The regulator DC current when the inductor current crosses zero, I_{DCM}, is:

$$I_{DCM} = \frac{\Delta I}{2} \quad (5)$$

The FAN5361 is optimized for operation with L = 470nH, but is stable with inductances up to 1.2µH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do the core and skin effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^2 + \frac{\Delta I^2}{12}} \quad (6)$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs, as well as the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Table 1 shows the effects of inductance higher or lower than the recommended 470nH on regulator performance.

Output Capacitor

Table 2 suggests 0402 capacitors. 0603 capacitors may further improve performance in that the effective capacitance is higher. This improves transient response and output ripple.

Increasing C_{OUT} has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is:

$$\Delta V_{OUT} = \Delta I \bullet \left(\frac{1}{8 \bullet C_{OUT} \bullet f_{SW}} + ESR \right) \quad (7)$$

Input Capacitor

The 2.2µF ceramic input capacitor should be placed as close as possible between the VIN pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as VIN increases due to DC Bias effects. This has no significant impact on regulator performance.

Table 1. Effects of Changes in Inductor Value (from 470nH Recommended Value) on Regulator Performance

Inductor Value	$I_{MAX(LOAD)}$	ΔV_{OUT} EQ. 7	Transient Response
Increase	Increase	Decrease	Degraded
Decrease	Decrease	Increase	Improved

Table 2. Recommended Passive Components and their Variation Due to DC Bias

Component	Description	Vendor	Min.	Typ.	Max.	Comment
L1	470nH, 2012, 90mΩ,1.1A	Murata LQM21PNR47MG0 Hitachi Metals JLSI-2012AG-R47(D2A)	300nH	470nH	520nH	Minimum value occurs at maximum current
C_{IN}	2.2µF, X5R, 0402	Murata or Equivalent GRM155R60J225ME15	1.0µF	2.2µF	2.4µF	Decrease primarily due to DC bias (V_{IN}) and elevated temperature
C_{OUT}	4.7µF, X5R, 0402	Murata or Equivalent GRM155R60G475M	1.6µF	4.7µF	5.2µF	Decrease primarily due to DC bias (V_{OUT})

PCB Layout Guidelines

There are only three external components: the inductor and the input and output capacitors. For any buck switcher IC, including the FAN5361, it is important to place a low-ESR input capacitor very close to the IC, as shown in Figure 41. The input capacitor ensures good input decoupling, which helps reduce noise appearing at the output terminals and ensures that the control sections of the IC do not behave erratically due to excessive noise. This reduces switching cycle jitter and ensures good overall performance. It is important to place the common GND of C_{IN} and C_{OUT} as close as possible to the FAN5361 C2 terminal. There is some flexibility in moving the inductor further away from the IC; in that case, V_{OUT} should be considered at the C_{OUT} terminal.

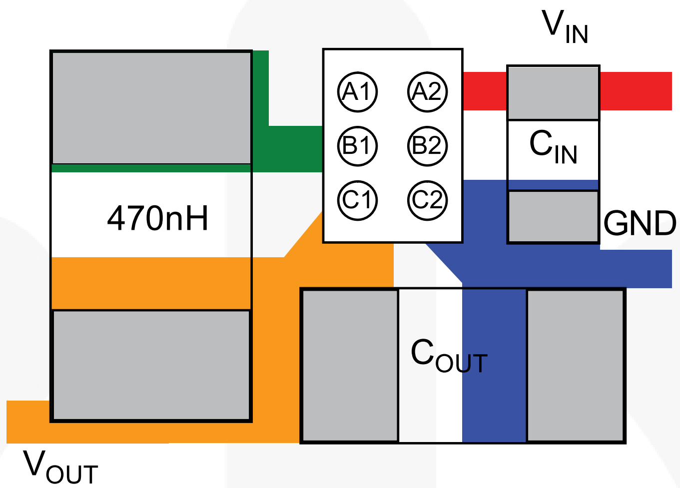

Figure 41. PCB Layout Guidance

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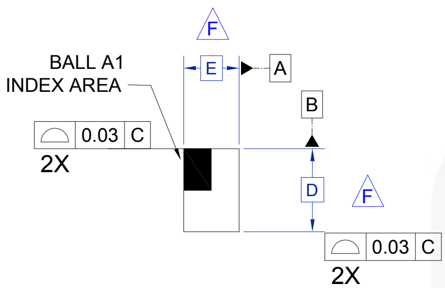
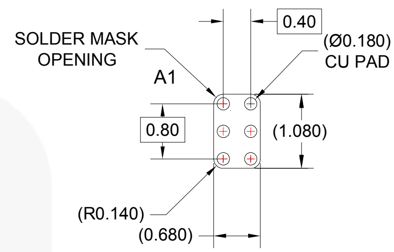
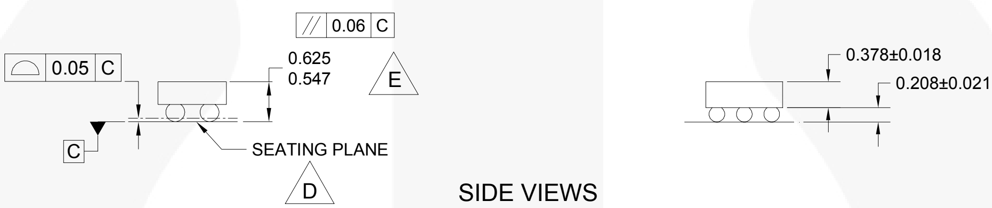
Physical Dimensions



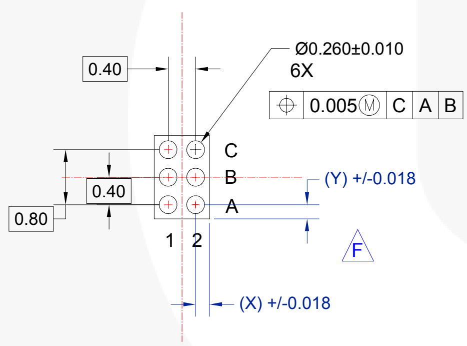
TOP VIEW



RECOMMENDED LAND PATTERN (NSMD)



SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASMEY14.5M, 1994.

D. DATUM C, THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. BALL COMPOSITION: Sn95.5-Ag3.9-Cu0.6.

H. DRAWING FILENAME: UC006ACrev1.

Figure 42. 6-Bump WLCSP, 0.4mm Pitch

Product Specific Dimensions

Product	D	E	X	Y
FAN5361UCX	1.390 +/-0.030	0.990 +/-0.030	0.295	0.295

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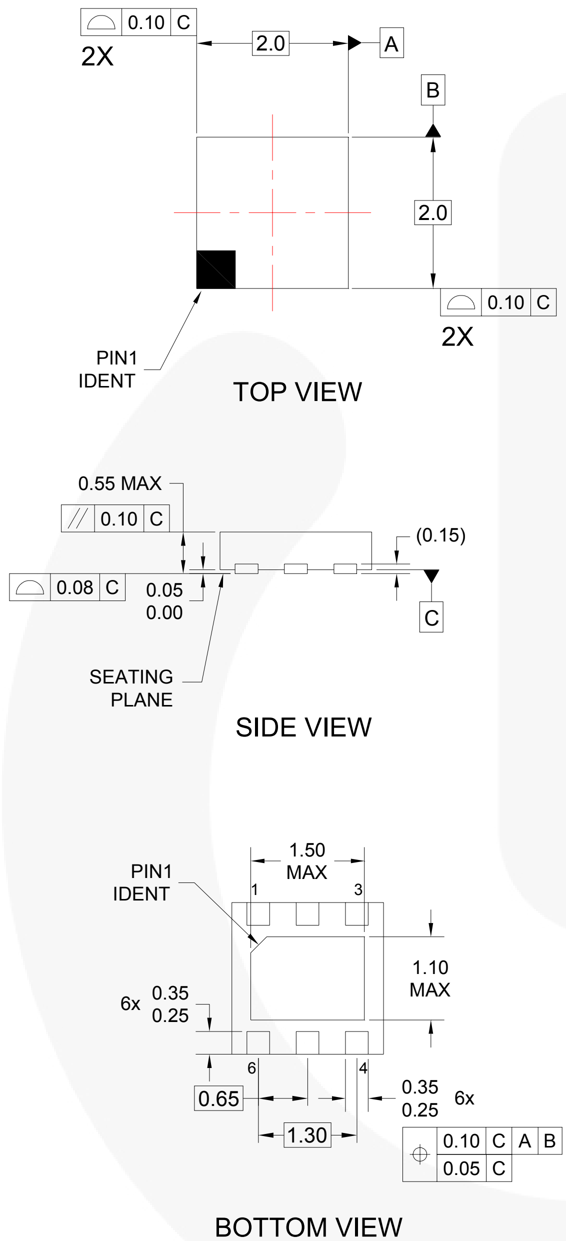
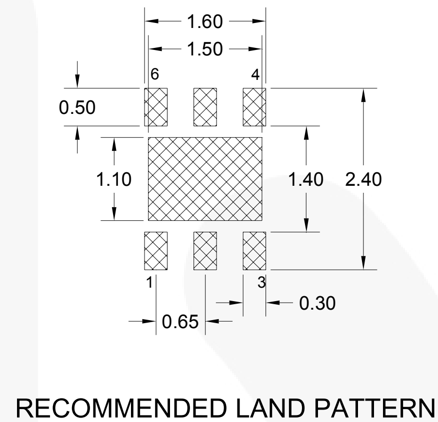
Physical Dimensions





NOTES:

A. OUTLINE BASED ON JEDEC REGISTRATION MO-229, VARIATION VCCC.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. DRAWING FILENAME: MKT-UMLP06Crev1

Figure 43. 6-Pin UMLP

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