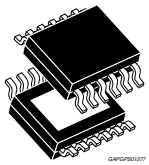
L9777

Low power voltage regulator

Datasheet - production data



PowerSSO-12 (exposed DIE Pad)

Features

- Operating DC supply voltage range 5.6 V to 31 V
- Low current consumption (110 µA typ @ I_{out} = 0)
- High precision output voltage (2 %)
- Low dropout voltage
- VDD tracking regulator switchable on/off by VDD_EN pin
- Reset circuit sensing the output voltage down to 1 V.
- Double reset function
- Adjustable reset threshold
- External capacitor to set NMI/ reset power up delay and watchdog frequency
- Over temperature protection
- Wide temperature range (T_J = -40 °C to 150 °C)
- Short circuit proof
- Suitable for use in automotive electronics

Description

The L9777 is a monolithic integrated low drop regulator which can supply up to 200 mA, available in the PowerSSO-12 package.

It is designed to supply microprocessor systems under severe conditions of automotive applications and therefore equipped with additional protection functions against over load, short circuit and over temperature.

Of course the L9777 can also be used in other applications where a regulated voltage is required.

Table 1. Device summary

Order code	Package	Packing
L9777A	PowerSSO-12	Tray
L9777B	PowerSSO-12	Tray
L9777B13TR	PowerSSO-12	Tape and reel
L9777C	PowerSSO-12	Tray
L9777C13TR	PowerSSO-12	Tape and reel

This is information on a product in full production. www.st.com

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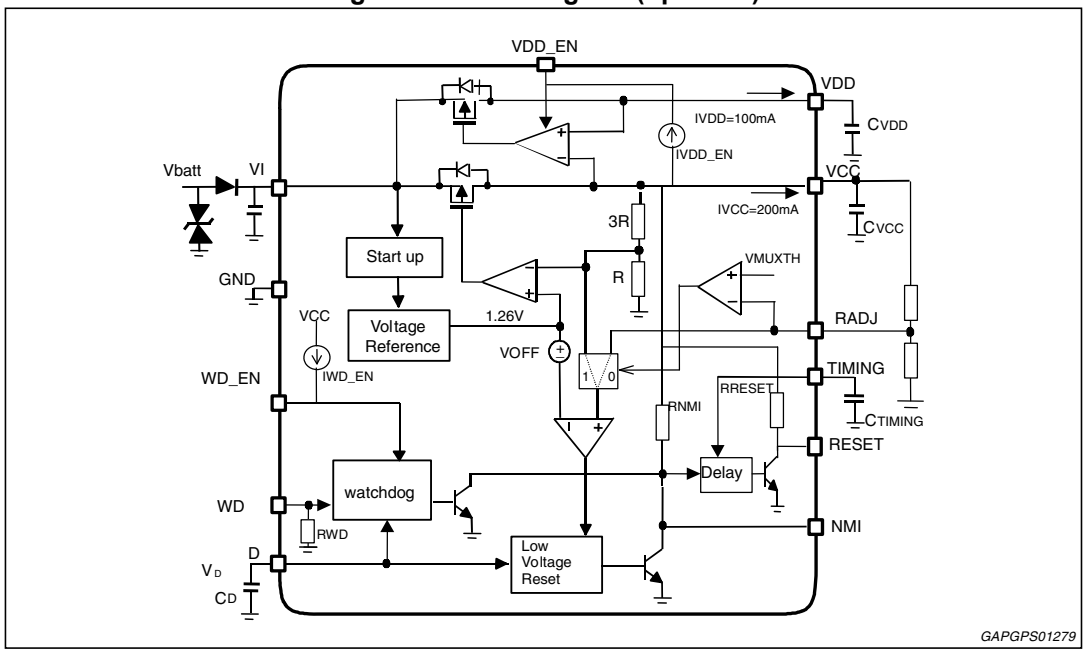
Figure 1. Block diagram (option A)



1.2 Option B features

- VDD can sustain short to 40 V regardless of VI battery voltage
- Current capability of VDD scaled down to 50 mA with dropout of 1.5 V (Max.)
- In default condition, VDD and WD functions are disabled using 2 pull down current on VDD_EN and WD_EN pin
- Standby current consumption reduced to 100 µA (Typ.)

Figure 2. Package pin configuration (options A and B)

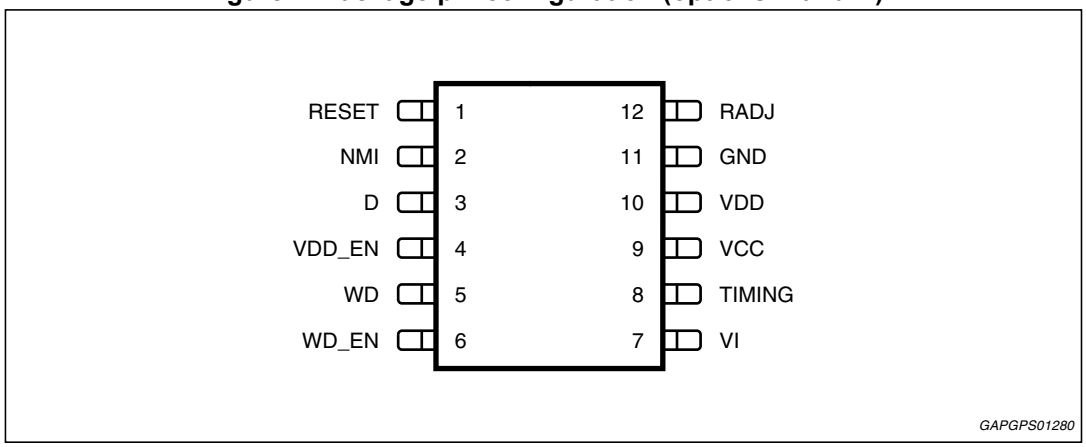


Figure 3. Block diagram (option B)

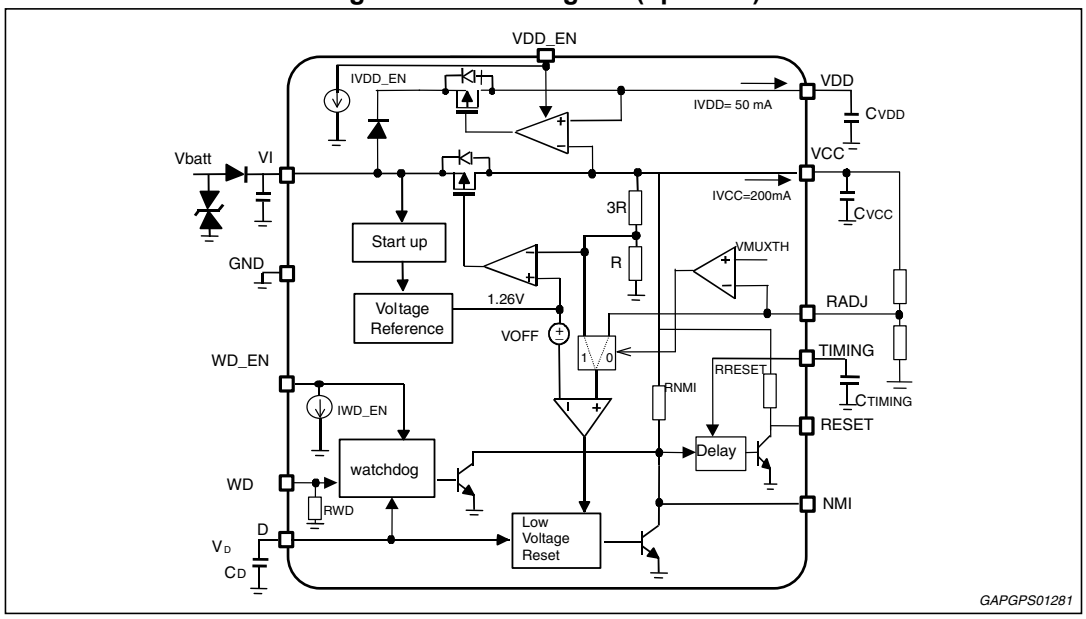
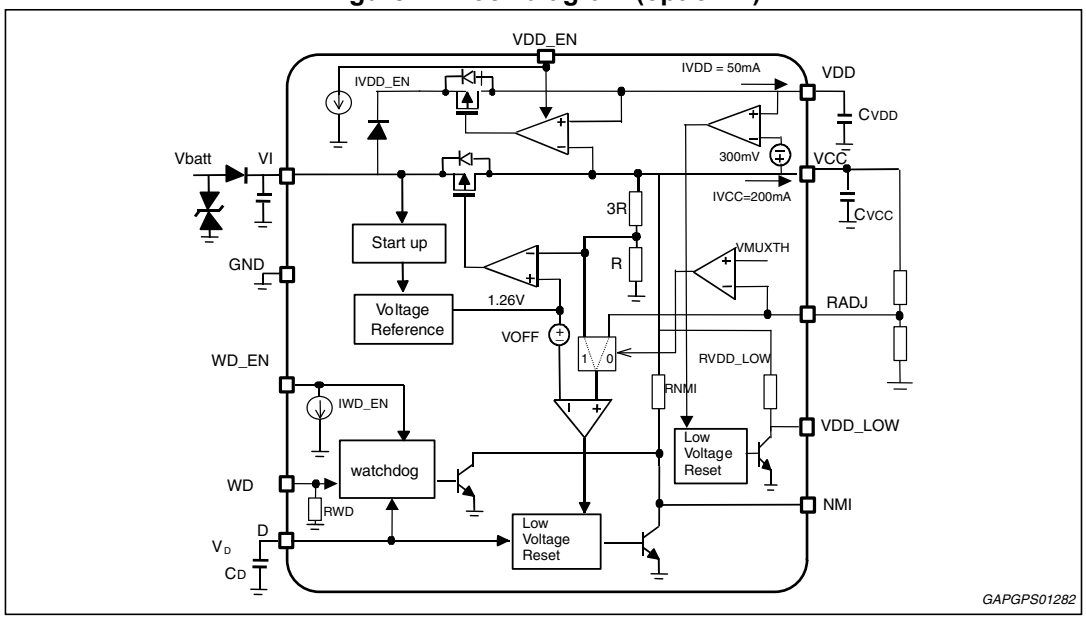


Figure 4. Block diagram (option C)



1.3 Option C features

- VDD can sustain short to 40 V regardless of VI battery voltage
- Current capability of VDD scaled down to 50 mA with dropout of 1.5V (Max.)
- In default condition, VDD and WD functions are disabled using 2 pull down current on VDD_EN and WD_EN pin
- Double reset function removed and pin RESET used to detect undervoltage condition on VDD regulated voltage (VDD_LOW pin)

Figure 5. Package pin configuration (option C)

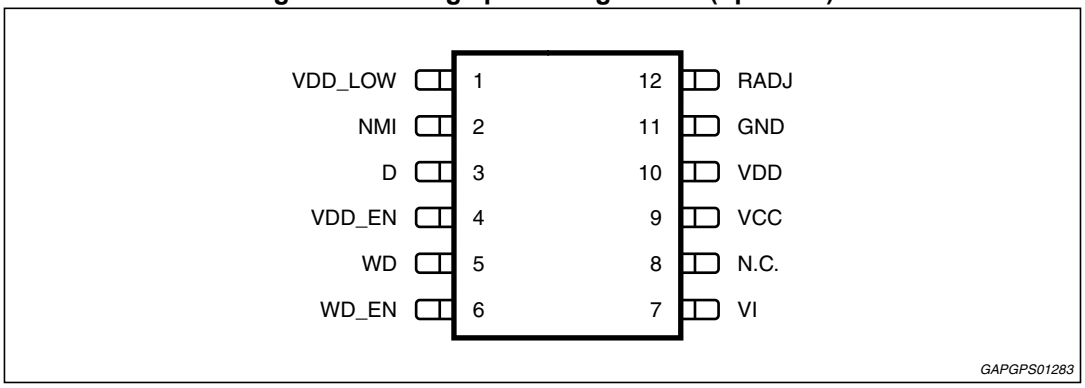


Table 2. Pin description

Pin#	I/O	Name	Function
1	O	RESET/VDD_LOW	**OPTION A & B**: RESET output. This pin is set low if NMI output goes low for adjustable filter time **OPTION C:** VDD_LOW output This pin is set low when undervoltage on VDD is detected
2	O	NMI	Non maskable Interrupt Output This pin is set low when low voltage on VCC is detected or frequency of WD signal is too low.
3	I	D	NMI/RESET power up delay. External cap on this pin sets the time response of the VCC low voltage detector and the time response of the watchdog monitor.
4	I	VDD_EN	VDD control. **OPTION A:** If this pin is low VDD output voltage is not available (connect this pin to VCC or left floating to switch on VDD output voltage) **OPTION B & C:** If this pin is low or left floating VDD output voltage is not available (connect this pin to VCC to switch on VDD regulator)
5	I	WD	Watchdog input. If the frequency at this input pin is too low, the NMI output is activated low

Table 2. Pin description (continued)

Pin#	I/O	Name	Function
6	I	WD_EN	Watchdog function enable/disable **OPTION A:** If this pin is low the watchdog function is disabled, if connected to VCC or left floating the watchdog function is enabled. **OPTION B & C:** If this pin is low or floating, the watchdog function is disabled, if connected to VCC the watchdog function is enabled.
7	I	VI	Input voltage Block to GND with a capacitor of value at least 100 nF
8	I	TIMING	**OPTION A & B:** RESET filter time External cap on this pin sets the delay time between NMI and RESET output **OPTION C:** not used and should be left floating or shorted to ground.
9	O	VCC	Voltage regulator output External cap CVCC ≥ 220 nF is needed to stabilize the regulator
10	O	VDD	VDD Output regulated voltage switched on/off by VDD_EN pin. External cap CVDD=100 nF is needed to stabilize the regulator
11		GND	Ground
12	I	RADJ	VCC under voltage Threshold Adjustment By connecting this pin to an external resistor divider vs. VCC, is possible to set the VCC under voltage threshold. If this pin is connected to GND the under voltage threshold is set by internal circuit.

2 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
Input voltage VI				
V_{VI}	Voltage	-0.3	40	V
I_{VI}	Current	Internal limited		
VCC				
V_{VCC}	Voltage	-0.3	5.5	V
I_{VCC}	Current	Internal limited		
NMI				
V_{NMI}	Voltage	-0.3	VCC+0.3	V
I_{NMI}	Current	Internal limited		
D				
V_D	Voltage	-0.3	VCC+0.3	V
	Current	Internal limited		
RADJ				
V_{RADJ}	Voltage	-0.3	VCC+0.3	V
I_{RADJ}	Current	Internal limited		
WD				
V_{WD}	Voltage	-0.3	VCC+0.3	V
I_{WD}	Current	Internal limited		
WD_EN				
V_{WD_EN}	Voltage	-0.3	VCC+0.3	V
I_{WD_EN}	Current	Internal limited		
VDD_EN				
V_{VDD_EN}	Voltage	-0.3	VCC+0.3	V
I_{VDD_EN}	Current	Internal limited		
RESET				
V_{RESET}	Voltage	-0.3	VCC+0.3	V
I_{RESET}	Current	Internal limited		

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Min.	Max.	Unit
Timing **VI + 0.3 (Opt. A)** **40V (Opt. B)** **Not connected (Opt. C)**				
V_{TIMING}	Voltage	-0.3	-	V
I_{TIMING}	Current	Internal limited		
VDD				
V_{VDD}	Voltage	-0.3	VI + 0.3 (Opt. A) 40V (Opt. B) 40V (Opt. C)	V
I_{VDD}	Current	Internal limited		
Temperature				
T_J	Junction temperature	-40	150	°C
ESD voltage level				
V_{ESD}	HBM-MIL STD 883C	-1.5	1.5	kV

3 Functional description

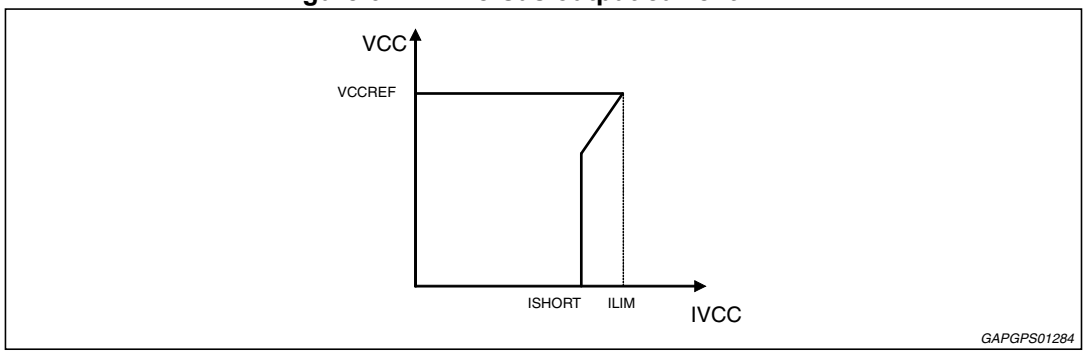
3.1 Voltage regulator

This device supply an always active 5 V regulated voltage on pin V_{CC} with a current capability up to 200 mA. V_{CC} voltage has an accuracy of 2% over a wide supply voltage (V_I = 5.6 V to 31 V) and temperature range (T_J = -40 °C to 150 °C).

A short circuit protection to GND is provided (see *Figure 6*).

By means of tracking regulator, it is available a second output regulated voltage on pin VDD with a current capability up to 50 mA. This regulated output is switchable on/off by external pin VDD_EN.

Figure 6. VCC versus output current IVCC



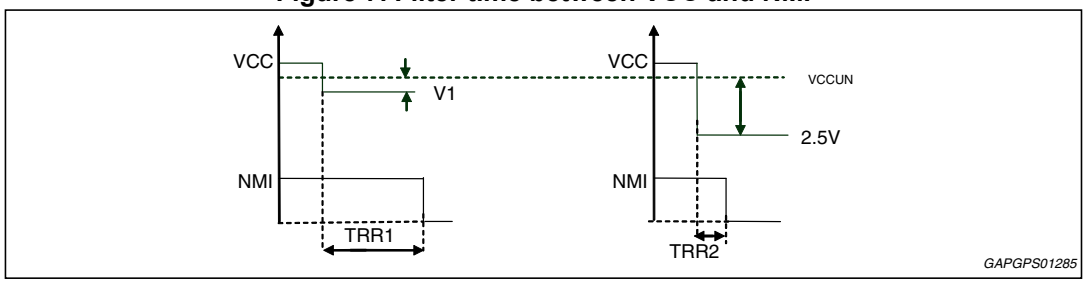
3.2 Reset

The reset circuit monitors the output voltage VCC. In case of internal reset threshold, if the output voltage stays lower than VCCUN for a filter time TRR, then NMI goes low.

This filter time depends on the distance between the VCC output and the under voltage reset threshold (VCCUN): this solution increases the noise immunity of the voltage regulator be-cause the filter time between the reset event and the falling of NMI output changes according to the depth of spike on output voltage (see following picture).

A minimum filter time of 1 µs (TRR1) is guaranteed if VCC goes down to 2.5 V and V_S > 5.6 V.

Figure 7. Filter time between VCC and NMI



Otherwise, in case of external reset threshold fixed by means of external resistor divider on pin RADJ, there is only a constant filter time (TRRADJ) of 1 µs min value.

In both cases, if the output voltage VCC becomes lower than 2.0V (typ) than NMI may go immediately low without any delay. The NMI low signal is guaranteed for an output voltage VCC greater than 1V.

When VCC returns over VCCUN threshold NMI goes high with a filter time TRD. This time is obtained by 127 period of an oscillator with an additional initial time. The oscillator period is given by:

$$TOSC = \frac{[(VDU - VDRL) \cdot CD]}{IRC} + \frac{[(VDU - VDRL) \cdot CD]}{IRD}$$

where:

ICR = 20 µA (typ) is a current internally generated,

IDR = 20 µA (typ) is a current internally generated,

VDU = 1.24 V and VDRL = 0.62 V are two typical internal thresholds,

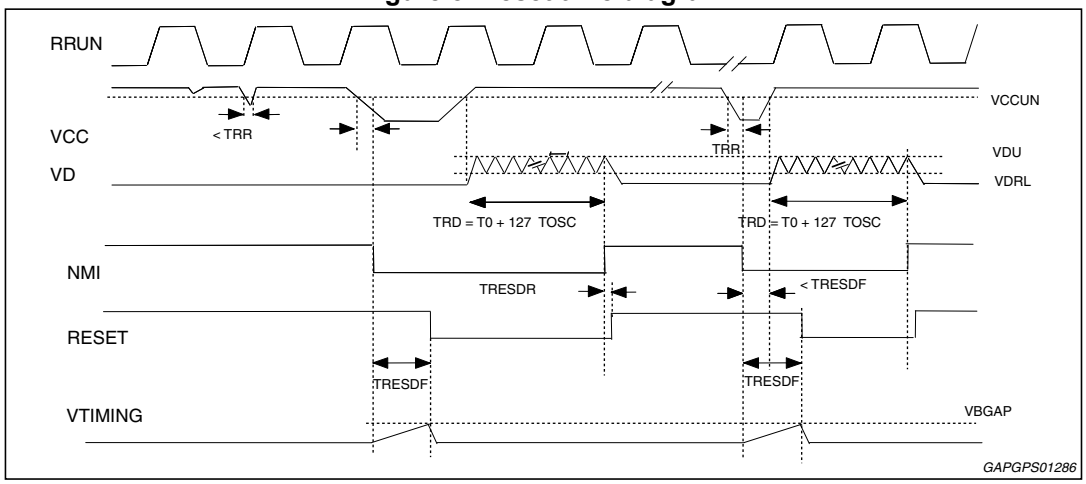
CD is the external capacitance on pin D.

TRD is given by:

$$TRD\ (s) = T0 + 127 \times TOSC = 0.62*10\text{-}3 \quad + 7.874* 106 * CD \quad (typ)$$

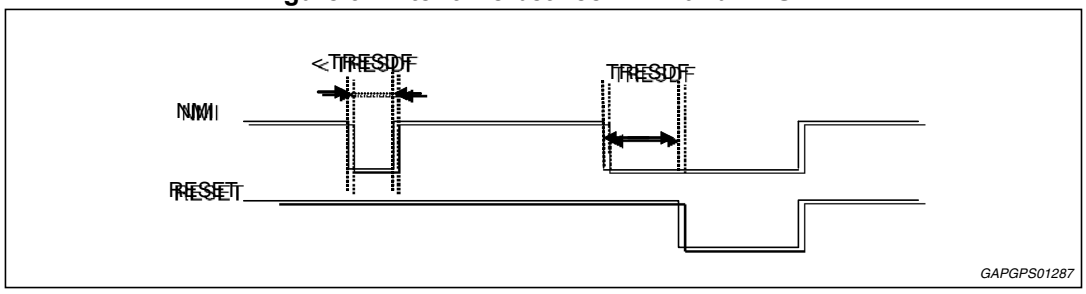
Where T0 is the initial ramp between 0 V and VDU as in *Figure 8*.

Figure 8. Reset time diagram



If NMI output goes to 0 V for filter time TRESDF (which is fixed by external cap on TIMING pin) also the RESET signal goes to 0 V. RESET low signal is guaranteed for VCC > 1 V.

Figure 9. Filter time between NMI and RESET



3.3 NMI and RESET driver delay

NMI and RESET pins are driven by bipolar transistor with a maximum current capability internally limited of value respectively INMIL and IRESL.

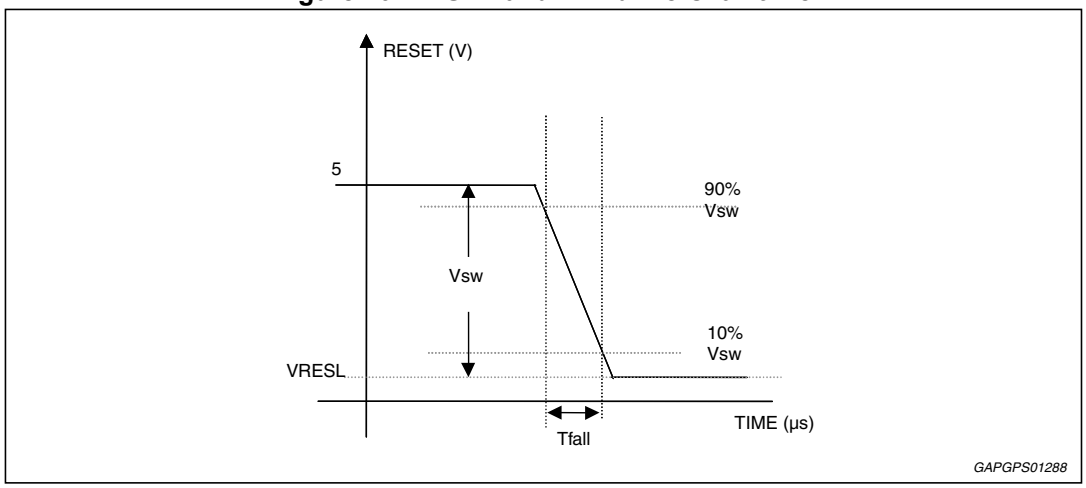
For this reason, when the drivers are activated, the capacitors present on pin NMI or RESET are discharged with constant current. The waveform on output pin is a voltage ramp with a slope linearly dependent on external capacitance.

The fall time needed by drivers to discharge external capacitor can be calculated in first approximation using this expression.

$$t_{fall} = \frac{(\Delta V \cdot C_{ext})}{I_{lim}}$$

Where ΔV is the voltage difference between 90% and 10% of total voltage swing of the transition, Cext is the total pin capacitance and Ilim is the current limitation of the driver (IRESL and INMIL).

Figure 10. RESET and NMI drivers fall time



3.4 RESET adjustable threshold

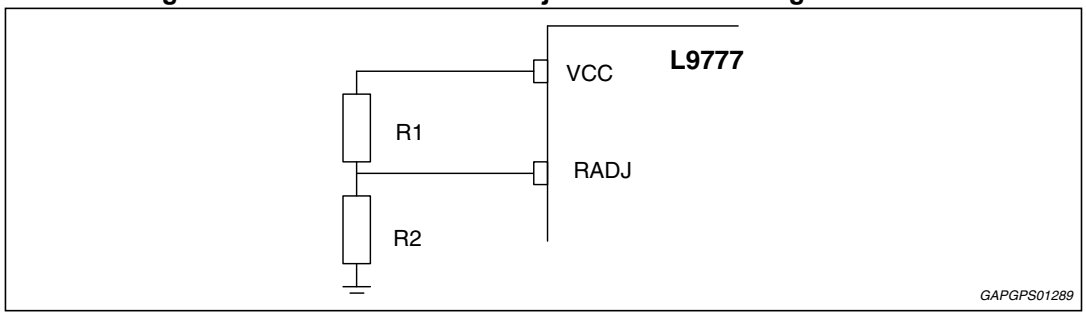
The under voltage threshold value (VCCUN) can be set between 0.7VCC (typ.) and 0.96VCC (typ) by connecting external resistor divider to RADJ pin (see *Figure 11*). This feature can be used with microprocessors that guarantee a safe operation with supply voltage lower than internal reset threshold. The calculation of this threshold is given by:

VCCUN_ext = VRADJTH (1+R1/R2) (neglecting RADJ input current)

where: VRADJTH=1.2V (typ) and VCCUN_ext is the reset threshold.

If this features is not needed, RADJ pin has to be connected to GND, in this case the internal under voltage threshold value is 0.94 * VCC (typ.).

Figure 11. Resistor divider to adjust the under voltage threshold



3.5 Watchdog

The watchdog input WD monitors a connected microcontroller. If pulses are missing, the output NMI is set to low. The minimum WD frequency to avoid reset event can be set with the external capacitor CD. The watchdog circuit charges and discharges the capacitor CD with the constant currents IWC and IWD, counting the number of oscillations as for TRD delay time. If no rising edge is sensed on pin WD between 48 oscillation periods (TWOP - TWOL, time A to B in *Figure 12*), a watchdog reset is generated. To prevent this reset the microcontroller must generate a positive edge during this time window in order to reset the counter.

Minimum frequency of microprocessor input signal can be calculated using following equation:

$$TWOP - TWOL = 48 * TOSC = 2.976*10^{6}*CD\ s$$

Every WD positive edge resets the counter and makes a synchronization between internal oscillator and external WD input signal.

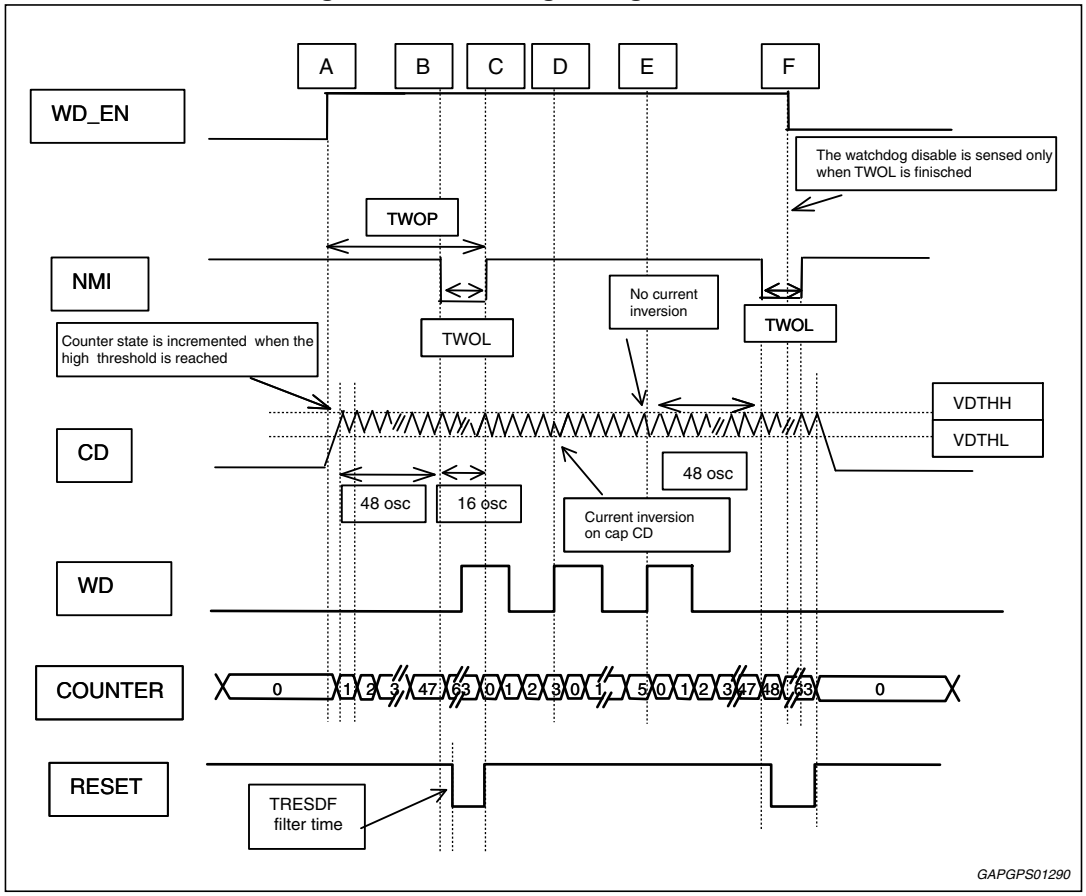
Synchronization is realized changing the current from charging to discharging if rising edge is detected during rising ramp on CD (time D in *Figure 12*). Otherwise if rising edge is detected during falling ramp on CD, no current inversion is performed (time E). This operation leads to a maximum error of half oscillation period on TWOP - TWOL time window. When NMI goes low for watchdog reset, the counter will go on for other 16 counts, returning to initial state (time B to C in *Figure 12*). During this time (TWOL) the NMI remains low and WD edges are masked, so the TWOL reset time is fully guaranteed.

The Watchdog operation is not active only if WD_EN input pin is set low.

In this case the capacitor CD, when not used for VCC undervoltage condition, is pulled down to 0V by an active switch.

At time F we can see that during TWOL reset time, WD_EN pin is not sensed, so the watchdog function can be disabled only when TWOL is finished. In this way a full reset time is guaranteed even in this condition.

Figure 12. Watchdog timing waveforms



4 VDD regulated voltage

L9777 provides a second regulated voltage in tracking with VCC main regulator capable to source load with up to 100 mA output current capability.

VDD tracking regulator function is controlled by VDD_EN input pin. If pin is set high VDD voltage becomes available. If pin is set low or left floating regulator is disabled.

Note that VDD regulator will be disable also in case of undervoltage condition on VCC main regulator, so at power up regulator will start up only when VCC rises over undervoltage threshold without TRD power up delay time, even if VDD_EN pin is set high.

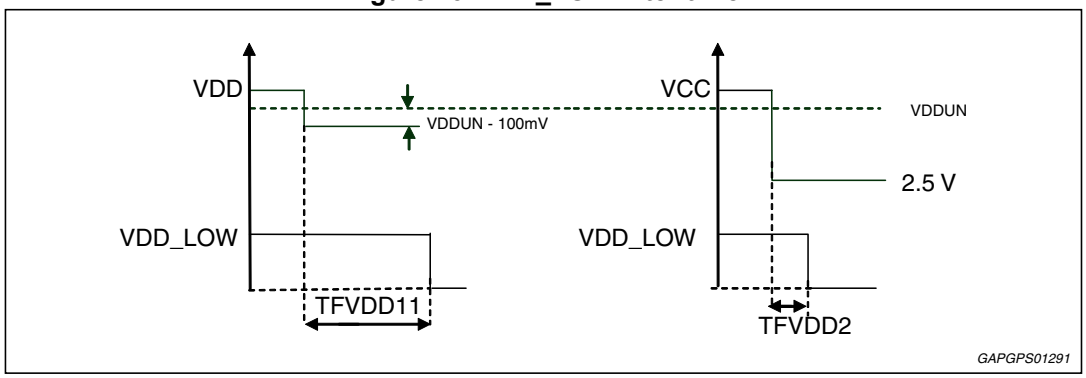
5 VDD_LOW (option C)

VDD_LOW circuit monitors VDD regulated voltage. When VDD falls below VDDUN for a filter time TFVDD VDD_LOW output voltage is set low.

VDDUN is a reference voltage 300 mV (Typ) lower than VCC regulated voltage.

Filter time TFVDD is spike dependent as TRR1 for VCC regulator so the same consideration applies also in this case.

Figure 13. VDD_LOW filter time



6 Device options

6.1 Option A

This is the standard configuration with VDD output capable to source up to 100 mA to an external load with low dropout (400 mV max.) and double reset function provided (NMI and RESET output).

Note that as we can see in absolute section VDD and TIMING pin are capable to sustain only short to VI pin.

With this option input digital pins VDD_EN and WD_EN are both pulled up by 5 µA typ current source (minimum quiescent current is 110 µA typ.).

6.2 Option B

With this option VDD and TIMING pins are both capable to sustain short to 40V regardless of VI battery voltage. To provide this feature a series diode is introduced between VI pin and VDD power PMOS source. In this configuration current capability on VDD output is scaled down to 50 mA while dropout voltage increases to 1.5V (Max). All other features are un-changed and double reset capability is maintained.

In option B VDD_EN and WD_EN are both pulled down with 10 µA typ internal current source so minimum quiescent current is reduced to 100 µA typ.

6.3 Option C

Using option C VDD is capable to sustain short to 40 V as in option B. VDD output current is scaled down to 50 mA and dropout increase up to 1.5 V (Max).

Double reset feature is removed and RESET pin is used to monitor VDD output voltage

(VDD_LOW pin). A spike dependent filter time similar to VCC main regulator is provided and same low voltage reset specifications applies to bipolar output driver (VDD_LOW driver).

For this reason TIMING pin is no more used and can be left floating or shorted to ground. Note that NMI output pin behaves normally as in option A and becomes the main reset signal for VCC and watchdog monitor.

As in option B VDD_EN and WD_EN are both pulled down with 10 µA typ internal current source so minimum quiescent current is reduced to 100 µA typ.

7 Electrical and thermal characteristics

V_I = 5.6V to 31V, T_J = -40°C to +150°C unless otherwise specified.

Table 4. Electrical and thermal characteristics

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General							
VCC	V_{CCREF}	Output voltage	V_I = 5.6 to 31 V I_{VCC} = 0 to 200 mA	4.9	5.00	5.1	V
VCC	I_{SHORT}	Short circuit current	V_{CC} = 0 V	150	250	500	mA
VCC	I_{LIM1}	Output current limitation		210	300	600	mA
VI, VCC	I_{QS0}	Current consumption with watchdog not active $I_{QS0} = I_{VI}$-I_{VCC} Option A	V_I =13.5 V, I_{VCC} = 0 mA, WD_EN = 0 V VDD_EN = 0 V (VDD disabled)	-	110	220	µA
		Option B	V_I = 13.5 V, I_{VCC} = 0 mA, WD_EN floating or low, VDD_EN floating or low (VDD disabled)	-	100	200	µA
		Option C	V_I = 13.5 V, I_{VCC} = 0 mA, WD_EN floating or low, VDD_EN floating or low (VDD reset active)	-	400	700	µA
	I_{QS200}	Current consumption IQS200 = I_{VI}-I_{VCC}	V_I = 13.5 V, I_{VCC} = 200 mA	-	2	3	mA
VI, VCC	V_{DP1}	Dropout voltage	I_{VCC} = 200 mA	-	200	400	mV
VCC	V_{LINE1}	Line regulation voltage	V_I = 5.6 to 31 V I_{VCC} = 0 to 200 mA	-	-	25	mV
VCC	V_{LOAD1}	Load regulation voltage	I_{VCC} = 0 to 200 mA	-	-	25	mV
VCC	SVR	Ripple rejection	f_r = 100 Hz	55	-	-	dB
-	T_W	Thermal protection temperature	-	150	-	190	°C
-	T_{WH}	Thermal protection temperature hysteresis	-	-	10	-	°C
NMI							
NMI	V_{NMIL}	NMI output low voltage	R_{ext} = 5 kΩ to V_{CC}, V_{CC} > 1 V	-	-	0.4	V
NMI	I_{NMILK}	NMI output leakage current	V_{NMI} = 5 V	-	-	1	µA
NMI	R_{NMI}	Pull up internal resistance	-	12	25	50	kΩ

Table 4. Electrical and thermal characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
NMI	V_{CCUN}	VCC under voltage threshold	RADJ = 0 V	4.5V	0.94 VCC	0.96 VCC	-
RADJ	V_{RADJTH}	Threshold for VCC under voltage detection	-	1.15	1.20	1.25	V
RADJ	$V_{RJMUXTH}$	Threshold for RADJ multiplexer comparator	-	0.52	0.62	0.72	V
D	VDU	NMI timing high threshold	-	1.14	1.24	1.34	V
D	VDRL	NMI timing low threshold	-	0.52	0.62	0.72	V
D	I_{RC}	Charge current	V_I = 13.5 V V_D = 0.1 V	10	20	40	µA
D	I_{RD}	Discharge current	V_I = 13.5 V V_D = 2.5 V	10	20	40	µA
NMI	TRR1	NMI spike dependent filter time in case of internal reset threshold	V_{CC} > 2 V RADJ = 0 V	1	-	-	µA
NMI	TRRADJ	NMI fixed filter time in case of external reset threshold	External resistor divider on RADJ (see *Figure 11*). V_{CC} > 2 V	1	2.5	5	µs
NMI	TRD	NMI power up delay	V_I =13.5 V, CD=10 nF	45	80	115	ms
NMI	I_{NMIL}	NMI limitation current	-	5	-	25	mA
RESET (option A & B)							
RESET	V_{RESL}	Reset output low voltage	R_{ext} = 5 kΩ to V_{CC}, V_{CC} > 1 V	-	-	0.4	V
RESET	$I_{RESETLK}$	RESET output leakage current	-	-	-	1	µA
RESET	I_{RESL}	RESET limitation current	-	5		25	mA
RESET	TRESDF	RESET delay from NMI falling edge	C_{TIMING} = 2.2 nF	350	550	750	µs
RESET	T_{RESDR}	RESET delay from NMI rising edge	-	-	-	1	µs
RESET	R_{RESET}	Pull up internal resistance	-	12	25	50	kΩ
VDD_LOW (option C)							
VDD_LOW	V_{VDD_LOWL}	Reset output low voltage	R_{ext} = 5 kΩ to V_{CC}, V_{CC} > 1 V	-	-	0.4	V
VDD_LOW	I_{VDD_LOWLK}	RESET output leakage current	-	-	-	1	µA
VDD_LOW	I_{VDD_LOWL}	RESET limitation current	-	5	-	25	mA
VDD_LOW	R_{VDD_LOW}	Pull up internal resistance	-	12	25	50	kΩ

Table 4. Electrical and thermal characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD_EN							
VDD_EN	V_{VDDTHL}	VDD_EN input low threshold	-	-	-	0.30 V_{CC}	V
VDD_EN	V_{VDDTHH}	VDD_EN input high threshold	-	0.70 V_{CC}	-	-	V
VDD_EN	V_{VDDHY}	VDD_EN hysteresis	-	200	500	800	mV
VDD_EN	I_{VDD_EN}	Pull up current Option A	-	2.5	5	10	µA
VDD_EN	I_{VDD_EN}	Pull down current Option B and C	-	5	10	20	µA
VDD (option A)							
VDD,VCC	DIFFVR	Output voltage difference between VDD and VCC	I_{VDD}=1 to 100 mA	-25	-	25	mV
VDD	I_{LIM2}	VDD output limitation current	-	110	200	400	mA
VI,VDD	V_{DP2}	Dropout voltage	I_{VDD} = 100 mA	-	200	400	mV
VDD	V_{LINE2}	VDD Line regulation voltage	V_I = 5.6 to 31 V I_{VDD} = 1 to 100 mA	-	-	25	mV
VDD	V_{LOAD2}	VDD Load regulation voltage	I_{VDD} = 1 to 100 mA	-	-	25	mV
VDD (option B)							
VDD,VCC	DIFFVR	Output voltage difference between VDD and VCC	I_{VDD} = 1 to 50mA V_I = 6.6 to 31V	-25	-	25	mV
VDD	I_{LIM2}	VDD output limitation current	V_I = 6.6 to 31V	55	100	240	mA
VI,VDD	V_{DP2}	Dropout voltage	I_{VDD} = 50mA; V_I = 6.6 to 31V	-	-	1.5	V
VDD	V_{LINE2}	VDD Line regulation voltage	I_{VDD} = 1 to 50mA V_I = 6.6 to 31V	-	-	25	mV
VDD	V_{LOAD2}	VDD Load regulation voltage	I_{VDD} = 1 to 50mA V_I = 6.6 to 31V	-	-	25	mV

Table 4. Electrical and thermal characteristics (continued)

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD (option C)							
VDD,VCC	DIFFVR	Output voltage difference between VDD and VCC	I_{VDD} = 1 to 50 mA V_I = 6.6 to 31 V	-25	-	25	mV
VDD	I_{LIM2}	VDD output limitation current	V_I = 6.6 to 31 V	55	100	240	mA
VI,VDD	V_{DP2}	Dropout voltage	I_{VDD} = 50 mA; VI = 6.6 to 31 V	-	-	1.5	V
VDD	V_{LINE2}	VDD Line regulation voltage	V_I = 6.6 to 31 V I_{VDD} = 1 to 50 mA	-	-	25	mV
VDD	V_{LOAD2}	VDD Load regulation voltage	I_{VDD} = 1 to 50 mA V_I = 6.6 to 31 V	-	-	25	mV
VDD	V_{DDUN}	VDD undervoltage threshold	V_I = 6.6 to 31 V	V_{CC}-400	V_{CC}-300	V_{CC}-200	mV
VDD	T_{FVDD}	VDD spike dependent undervoltage filter time	VDD transition from 5 V to 4 V	1	-	-	µs
WD							
WD	V_{WDTHH}	Input high voltage	-	-	-	0.3 V_{CC}	V
WD	V_{WDTHL}	Input low voltage	-	0.7 V_{CC}	-	-	V
WD	V_{WDHY}	WD input hysteresis	-	250	500	800	mV
WD	R_{WD}	Pull down resistor	-	15	35	80	kΩ
D	I_{WDC}	Charge current	V_D = 0.1 V; V_I = 13.5 V	10	20	40	µA
D	I_{WDD}	Discharge current	V_D = 2.5 V; V_I = 13.5 V	10	20	40	µA
D	V_{DTHL}	Low threshold	-	0.52	0.62	0.72	
D	V_{DTHH}	High threshold	-	1.14	1.24	1.34	V
D	T_{WOP}	Watchdog period	CD =10 nF	20	40	80	ms
D	T_{WOL}	Watchdog output low time	CD =10 nF	5	10	20	ms
WD_EN							
WD_EN	V_{WENTL}	WD_EN input low voltage	-	-	-	0.30 V_{CC}	-
WD_EN	V_{WENTH}	WD_EN input high voltage	-	0.70 V_{CC}	-	-	-
WD_EN	V_{WENHY}	WD_EN input hysteresis	-	200	500	800	mV
WD_EN	I_{WD_EN}	Pull up current Option A	-	2.5	5	10	µA
WD_EN	I_{WD_EN}	Pull down current Option B and C	-	5	10	20	µA

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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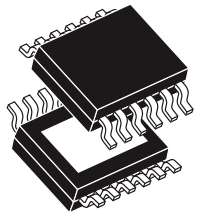
Figure 14. PowerSSO-12 mechanical data and package dimensions

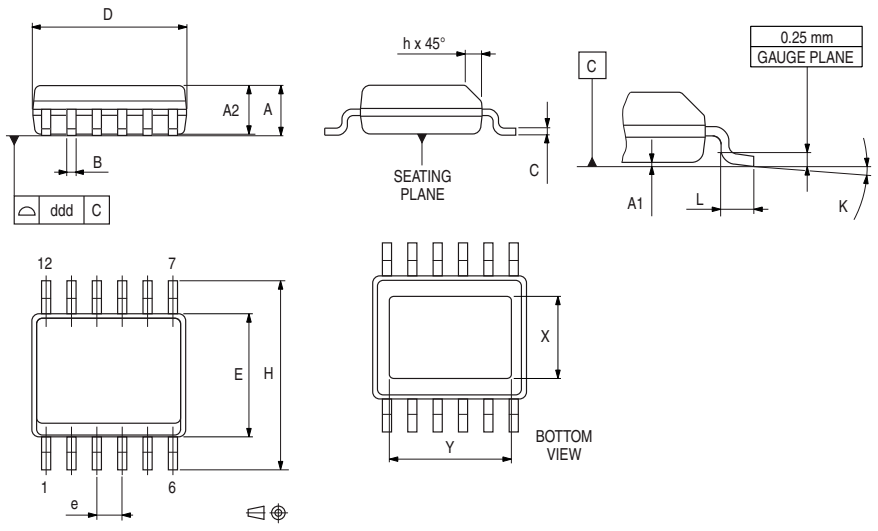
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.250		1.700	0.049		0.0669
A1	0.000		0.100	0.000		0.004
A2	1.100		1.600	0.043		0.063
B	0.230		0.410	0.009		0.016
C	0.190		0.250	0.007		0.010
D (1)	4.800		5.000	0.189		0.197
E	3.800		4.000	0.150		0.157
e		0.800			0.031	
H	5.800		6.200	0.228		0.244
h	0.250		0.550	0.010		0.0217
L	0.400		1.270	0.016		0.050
k	0°		8°	0°		8°
X	1.900		2.500	0.075		0.098
Y	3.600		4.200	0.142		0.165
ddd			0.100			0.004

Note: 1. D does not include mold flash or protrusions or gate burrs. Mold flash potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total.

OUTLINE AND MECHANICAL DATA



PowerSSO-12 (Exposed Pad)



GAPGPS01278

9 Revision history

Table 5. Revision history

Date	Revision	Description of changes
10-May-2007	1	Initial release.
14-Dec-2010	2	Changed ESD parameter values in *Table 3*. Modified *Section 1.3: Option C features on page 7*. Modified *Section 6.3: Option C on page 18*. Updated *Table 4: Electrical and thermal characteristics on page 19*. Document status promoted from preliminary data to datasheet.
11-Jan-2012	3	Update *Table 1: Device summary on page 1*. Updated *Figure 14: PowerSSO-12 mechanical data and package dimensions on page 23*.
20-Feb-2014	4	Updated disclaimer.

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