ANALOG DEVICES

EVAL-AD7175-2SDZ User Guide
UG-AD7175-2

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD7175-2 24-Bit, 250 kSPS, Sigma-Delta ADC with 20 µs Settling and Integrated Analog Input Buffers

FEATURES

Full featured evaluation board for the AD7175-2
PC control in conjunction with the SDP (see EVAL-SDP-CB1Z from Analog Devices, Inc. for additional information)
PC software for control and data analysis (time domain)
Standalone capability

EVALUATION KIT CONTENTS

EVAL-AD7175-2SDZ evaluation board
Evaluation software CD
7 V to 9 V ac-to-dc adapter

EQUIPMENT NEEDED

DC signal source

GENERAL DESCRIPTION

The EVAL-AD7175-2SDZ evaluation kit features the AD7175-2, a 24-bit, 250 kSPS analog-to-digital converter (ADC) with integrated rail to rail analog input buffers, on-board power supply regulation, and an external amplifier section for amplifier evaluation. A 7 V to 9 V ac-to-dc adapter is regulated to 5 V and 3.3 V; this supplies the AD7175-2 and support components. The EVAL-AD7175-2SDZ board connects to a USB port via the system demonstration platform (SDP) EVAL-SDP-CB1Z controller board.

The EVAL-AD7175-2SDZ evaluation software fully configures the AD7175-2 device functionality via a user accessible register interface and provides dc time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

FUNCTIONAL BLOCK DIAGRAM

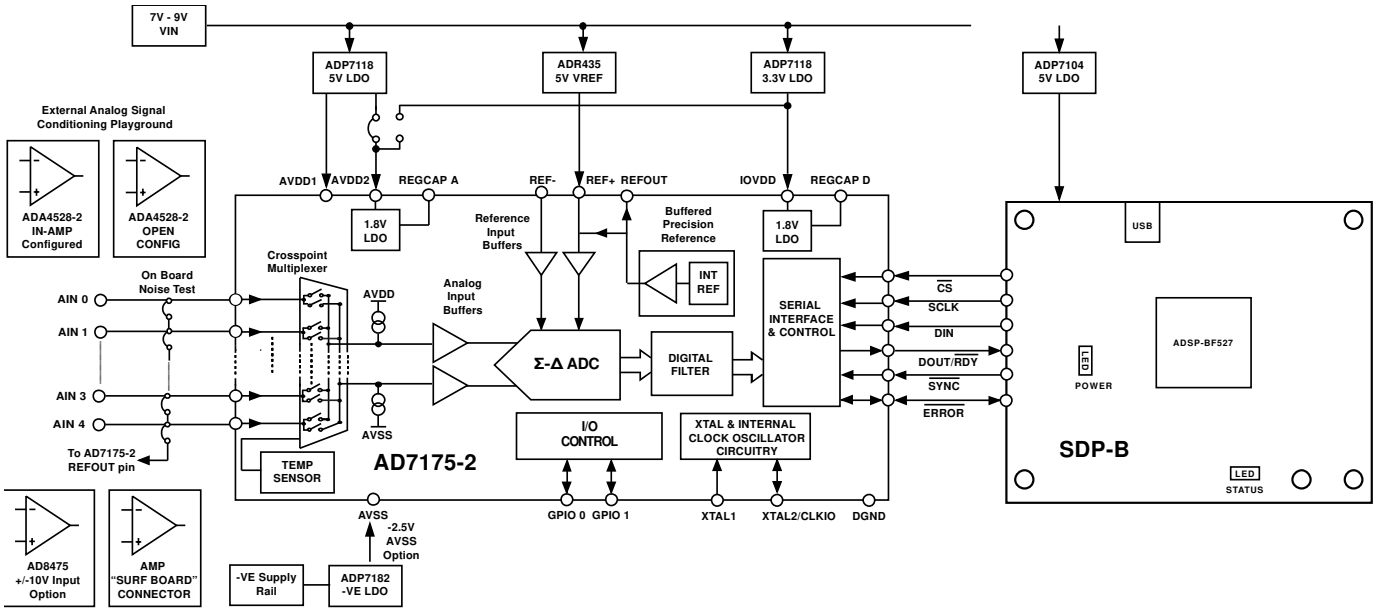

Figure 1. EVAL-AD7175-2SDZ Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

10/14—Revision Pr.A: Initial Preliminary Version

EVAL-AD7175-2SDZ QUICK START GUIDE

RECOMMENDED QUICK START GUIDE

Follow these steps to set up the board:

1. Disconnect the SDP-B board from the USB port of the PC. Install the EVAL-AD7175-2SDZ software from the enclosed CD. Restart the PC after installation.
2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7175-2SDZ board, as shown in Figure 2.
3. Fasten the two boards with the enclosed plastic screw washer set.
4. Connect the external 9 V power supply to Connector J5 of the EVAL-AD7175-2SDZ board as shown in Figure 2. Set LK2 to Position B.
5. Connect the SDP board to the PC via the USB cable. For Windows® XP, you may need to search for the SDP drivers. Choose to automatically search for the drivers for the SDP-B board if prompted by the operating system.
6. Launch the EVAL-AD7175-2SDZ software from the Analog Devices subfolder in the **Programs** menu.

QUICK START NOISE TEST

Use the following procedure to quickly test the noise performance:

1. Insert Link LK5 to Link LK9 to initiate the noise performance test mode. In this mode, analog input channels short to the REFOUT pin.
2. Click **Start Sampling** to acquire samples from the ADC (see Figure 7).

The **Samples** numeric control in the top right corner of the main window sets the number of samples collected in each batch.

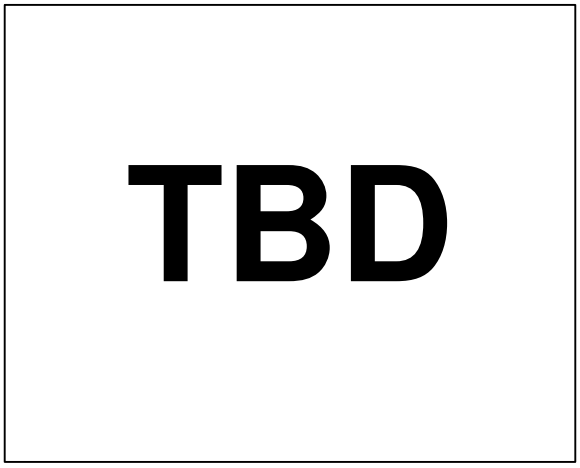

Figure 2. Hardware Configuration, Setting Up the EVAL-AD7175-2SDZ

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7175-2 is a highly accurate, high resolution, multiplexed, 2-/4-channel (fully differential/single-ended) Σ-Δ ADC. The AD7175-2 has a maximum channel-to-channel scan rate of 50 kSPS (20 µs) for fully settled data The output data rates range from 5 SPS to 250 kSPS. The device includes integrated rail to rail analog input and reference input buffers, an integrated precision 2.5 V reference, and an integrated oscillator.

See the AD7175-2 data sheet for complete specifications. Consult the data sheet in conjunction with this user guide when using the evaluation board. Full details for the EVAL-SDP-CB1Z are available on the Analog Devices website.

HARDWARE LINK OPTIONS

See Table 1 for default link options. By default, the board is configured to operate from the supplied 9 V ac-to-dc adapter connected to connector J5. The 5 V supply required for the AD7175-2 comes from the on-board low dropout regulator (LDO). The ADP7118, with a 5 V output voltage, receives its input voltage from J3 or J5 (depending on the position of LK2) and generates a 5 V output.

Table 1. Default Link and Solder Link Options

Link	Default Option	Description
LK1	A	Selects the voltage applied to the power supply sequencer circuit (U3); dependent on AVDD1. Place in Position A if using 5 V AVDD1, or Position B if using 2.5 V AVDD1.
LK2	B	Selects the external power supply from Connector J3 (Position A), or J4 (Position B).
LK5 to LK9	Inserted	Inserting these links sets up the on-board noise test. In this mode, all inputs short to the common voltage via SL11.
SL1	A	Sets the voltage applied to the AVDD2 pin. Operates using the AVDD1 supply (default). Position B sets the AVDD2 voltage to 3.3 V supply from the ADP7118 (3.3 V) (U10) regulator.
SL2	A	Selects between an external or on-board AVDD1 source. Supplies AVDD1 from the ADP7118 (5 V) (U7) (default).
SL3	A	Selects between an external or on-board AVSS source. Supplies AVSS from the ADP7182 (-2.5 V) (U4) (default).
SL4	A	Connects AIN4 to: A4 / J6 (Position A), REFOUT pin on the AD7175-2 (Position B) or AVSS (Position C). Positions B and C are used to simplify using a single ended input source.
SL5	B	Selects between an external or on-board IOVDD source. Supplies IOVDD from the ADP7118 (3.3 V) (U10) (default). The evaluation board operates with a 3.3 V logic.
SL8	A	Routes A0 to: AIN0 pin on the AD7175-2 (Position A), Buffer/Inamp U8 (Position B), Funnel Amp U9 with gain of 0.8x (Position C) or J10-1 (Position D).
SL9	A	Routes A2 to: AIN2 pin on the AD7175-2 (Position A), Buffer U12 (Position B) or Funnel Amp U9 gain of 0.4x (Position C).
SL10	A	Routes A3 to: AIN3 pin on the AD7175-2 (Position A), Buffer U12 (Position B) or Funnel Amp U9 gain of 0.4x (Position C).
SL11	A	Routes A1 to: AIN1 pin on the AD7175-2 (Position A), Buffer/Inamp U8 (Position B), Funnel Amp U9 with gain of 0.8x (Position C) or J10-7 (Position D).
R49 to R51	Inserted	Connects AVSS and AGND for single-supply operation. To operate in split supply mode, remove these links.

SOCKETS AND CONNECTORS

Table 2. Connector Details

Connector	Function	Connector Type	Manufacturer	Manufacturer Number	Order Code[1]
J1	Connector to the EVAL-SDP-CB1Z	120-way connector, 0.6 mm pitch	Hirose	FX8-120S-SV(21)	FEC1324660
J2	External MCLK Input	Straight PCB mount SMB/SMA jack	Tyco	1-1337482-0	Not applicable
J3	External bench top voltage supply for the EVAL-AD7175-2SDZ	Power socket block, 3-pin, 3.81 mm pitch	Phoenix Contact	MC 1,5/ 3-G-3,81	FEC3704737
J5	External ac-to-dc adapter input for the EVAL-AD7175-2SDZ, 7 V to 9 V	DC power connectors, 2 mm SMT power jack	Kycon	KLDX-SMT2-0202-A	MOUSER 806-KLDX-SMT20202A
J6	Analog input terminal block; wired connection to external source or sensor	Power socket block, 8-pin, 3.81 mm pitch	Phoenix Contact	MC 1,5/ 8-G-3,81	FEC3704774
J9	External bench top voltage supply option for AVDD1/AVDD2, IOVDD and AVSS inputs on the AD7175-2	Screw terminal block, 3.81 mm pitch	Phoenix Contact	MKDS 1/4-3.81	FEC3704592
J10	Optional header	7-way, 2.54 mm pin header	Samtec	SSW-107-01-T-S	FEC1803478
J13	Optional header	7-way, 2.54 mm socket	Samtec	TLW-107-05-G-S	FEC1668499
A0 to A4	Analog inputs to ADC	Straight PCB mount SMB/SMA jack	Tyco	1-1337482-0	Not applicable
A7	PMOD Compatible Header	6-Pin SIL Header (0.1" pitch)	Harwin	20-9990646	FEC 1022255

[1] Order codes starting with FEC are for Farnell.

SERIAL INTERFACE

The AD7175-2 evaluation board connects via the serial peripheral interface (SPI) to the Blackfin® ADSP-BF527 on the EVAL-SDP-CB1Z. There are four primary signals: $\overline{CS}$, SCLK, and DIN (all inputs), and one output from the ADC, DOUT/$\overline{RDY}$.

To operate the EVAL-AD7175-2SDZ in standalone mode, disconnect the evaluation board from the SDP-B controller board. Use the test points to connect the signals to an alternative digital capture setup or the PMOD compatible header (A7).

POWER SUPPLIES

Power the evaluation board from the ac-to-dc adapter connected to J5, or from an external bench top supply applied to J3 or J9. Linear LDOs generate the required voltages from the applied input voltage (V_{IN}) rail when using J3 or J5. Use J9 to bypass the on-board regulators. An ADP7118 regulator is used to generate the 5 V (single supply) and 2.5 V (split supply) supplies for the AVDD1 and AVDD2 rails to the ADC; a second ADP7118 generates 3.3 V for the IOVDD rail. The ADP7104 supplies 5 V for the SDP-B controller board as well as 5 V for the ADM660 voltage converter to generate -5 V to supply the ADP7182. The ADP7182 generates the -2.5 V supply for AVSS when operating in split supply mode. Each supply is decoupled where it enters the board and again at each device in accordance with the schematic. Table 3 shows the various power supply configurations available, including split supply operation.

Table 3. Power Supply Configurations[1]

Configuration	Input Voltage Range	Description
Single Supply (Regulated)	7 V to 9 V	The 7 V to 9 V input is regulated to 5 V for AVDD1/AVDD2 and 3.3 V for IOVDD. This also powers the external 5 V reference. See the Single Supply (Regulated) section in the Power Supply Configurations section.
Single Supply (Unregulated)	7 V to 9 V, 5 V, and 3.3 V	The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Single Supply (Unregulated) section in the Power Supply Configurations section.
Split Supply (Regulated)	7 V to 9 V and −2.5 V	The 7 V to 9 V input is regulated to 2.5 V for AVDD1/AVDD2 and 3.3 V for IOVDD. The 7 V to 9 V input powers the external 5 V reference, and the −2.5 V input is connected to AVSS directly (unregulated). See the Split Supply (Regulated) section in the Power Supply Configurations section.
Split Supply (Unregulated)	7 V to 9 V, ±2.5 V, and 3.3 V	The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Split Supply (Unregulated) section in the Power Supply Configurations section.

[1] Only one configuration can be used at a time.

POWER SUPPLY CONFIGURATIONS

Single Supply (Regulated)

There are two available power supply options for the single supply (regulated) configuration.

- An ac-to-dc adapter (included) connected to J5. Set LK2 to Position B.
- A bench top power supply connected to J3. Set LK2 to Position A and ensure that AVSS = AGND = 0 V.

Set all other links and solder links to the default settings as outlined in Table 1.

Single Supply (Unregulated)

To set up the board, use the following procedure:

1. Move SL2 and SL5 to Position A.
2. Connect the two terminals of J9 labeled AGND and AVSS.
3. Connect 0 V (GND) to J9 at the terminal labeled AGND.
4. Connect 5 V to J9 at the terminal labeled AVDD.
5. Connect 3.3 V to J9 at the terminal labeled IOVDD.
6. Connect the 7 V to 9 V input to J5.

Set all other links and solder links to the default settings as outlined in Table 1.

Split Supply (Regulated)

To set up the board, use the following procedure:

1. Remove R49 to R51. These links connect AVSS to AGND.
2. Insert a zero ohm resistor for R85.
3. Set LK1 to Position B. This sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.
4. Connect a bench top power supply to J5 and set LK2 to Position B.
5. Set LK1 to Position B. This sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.

Set all other links and solder links to the default settings as outlined in Table 1.

Split Supply (Unregulated)

To set up the board, use the following procedure:

1. Move SL2, SL3 and SL5 to Position A.
2. Remove R49-R51.
3. Connect 0 V (GND) to J9 at the terminal labeled AGND.
4. Connect 2.5 V to J9 at the terminal labeled AVDD.
5. Connect −2.5 V to J9 at the terminal labeled AVSS.
6. Connect 3.3 V to J9 at the terminal labeled IOVDD.
7. Connect 7 V to 9 V to J5.
8. Set LK1 to Position B. This sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.

Set all other links and solder links set to the default settings as outlined in Table 1.

ANALOG INPUTS

The EVAL-AD7175-2SDZ primary analog inputs can be applied in two separate ways.

- J6 connector on the left side of the board
- A0 to A4 SMB/SMA footprints on the evaluation board

The analog inputs route directly to the associated analog input pins on the AD7175-2, provided that the LK5 to LK9 links (on-board noise test) are removed. The EVAL-AD7175-2SDZ software is set up to analyze dc inputs to the ADC. The AD7175-2 input buffers work for dc input signals.

REFERENCE OPTIONS

The EVAL-AD7175-2SDZ includes an external 5 V reference, the ADR445. The AD7175-2 includes an internal 2.5 V reference. The default operation is to use the external reference input, which is set to accept the 5 V ADR445 on the evaluation board.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The EVAL-AD7175-2SDZ evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the installer. The default installation location for the software is **C:\Program Files\Analog Devices\EVAL-AD7175-2SDZ\.**

Install the evaluation software before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC. This ensures that the evaluation system is correctly recognized when connected to the PC.

There are two parts to the installation.

- AD7175-2 evaluation board software installation
- EVAL-SDP-CB1Z system demonstration platform board drivers installation

Place the software and drivers in the appropriate locations by proceeding through all of the installation steps. Connect the EVAL-SDP-CB1Z board to the PC only after the software and drivers install. The installer may prompt you to allow the program to make changes to the computer. Click **Yes** to proceed (see Figure 3).

Figure 3. AD7175-2 User Account Control Permission Dialog Box

You may receive a security warning as part of the SDP-B controller board driver installation. Click **Install** to proceed with the installation of the driver (see Figure 4). Without this confirmation, the software cannot operate correctly.

Figure 4. EVAL-SDP-CB1Z Drivers Installation Confirmation Dialog Box

After installation is complete, connect the EVAL-AD7175-2SDZ to the EVAL-SDP-CB1Z, as shown in Figure 2. Connect the EVAL-SDP-CB1Z board via the USB cable to the computer. Follow these steps to verify the SDP-B controller board driver is installed and working correctly:

1. Allow the **Found New Hardware Wizard** to run.
2. Once the drivers are installed, check that the board has connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be found by right clicking **My Computer**, selecting **Manage**, then **Device Manager** from the list of **System Tools** (see Figure 5).
3. The EVAL-SDP-CB1Z board appears under **ADI Development Tools** as **Analog Devices System Development Platform** or similar. The installation is complete.

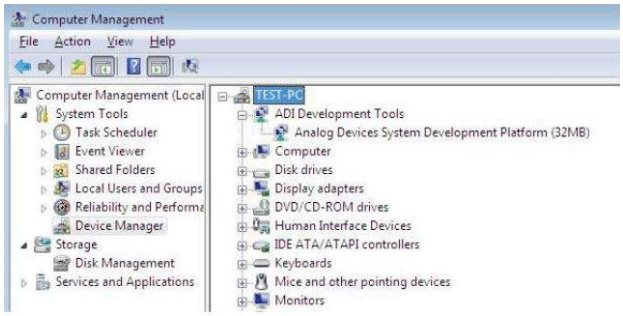

Figure 5. Device Manager

LAUNCHING THE SOFTWARE

The AD7175-2 software can be launched when the EVAL-AD7175-2SDZ and EVAL-SDP-CB1Z are correctly connected to the PC.

To launch the software, complete the following:

1. From the **Start** menu, click **Programs**, **Analog Devices**, then **EVAL-AD7175-2SDZ**. The main window of the software then displays (see Figure 7).
2. If the AD7175-2 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched the "Select Interface…" dialog box appears. Connect the evaluation board to the USB port of the PC, wait a few seconds, click the green arrows to rescan the USB ports. Once connected then click work online to proceed.

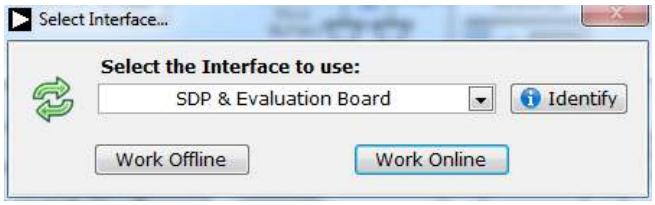

Figure 6. Select Interface Dialog Box

SOFTWARE OPERATION

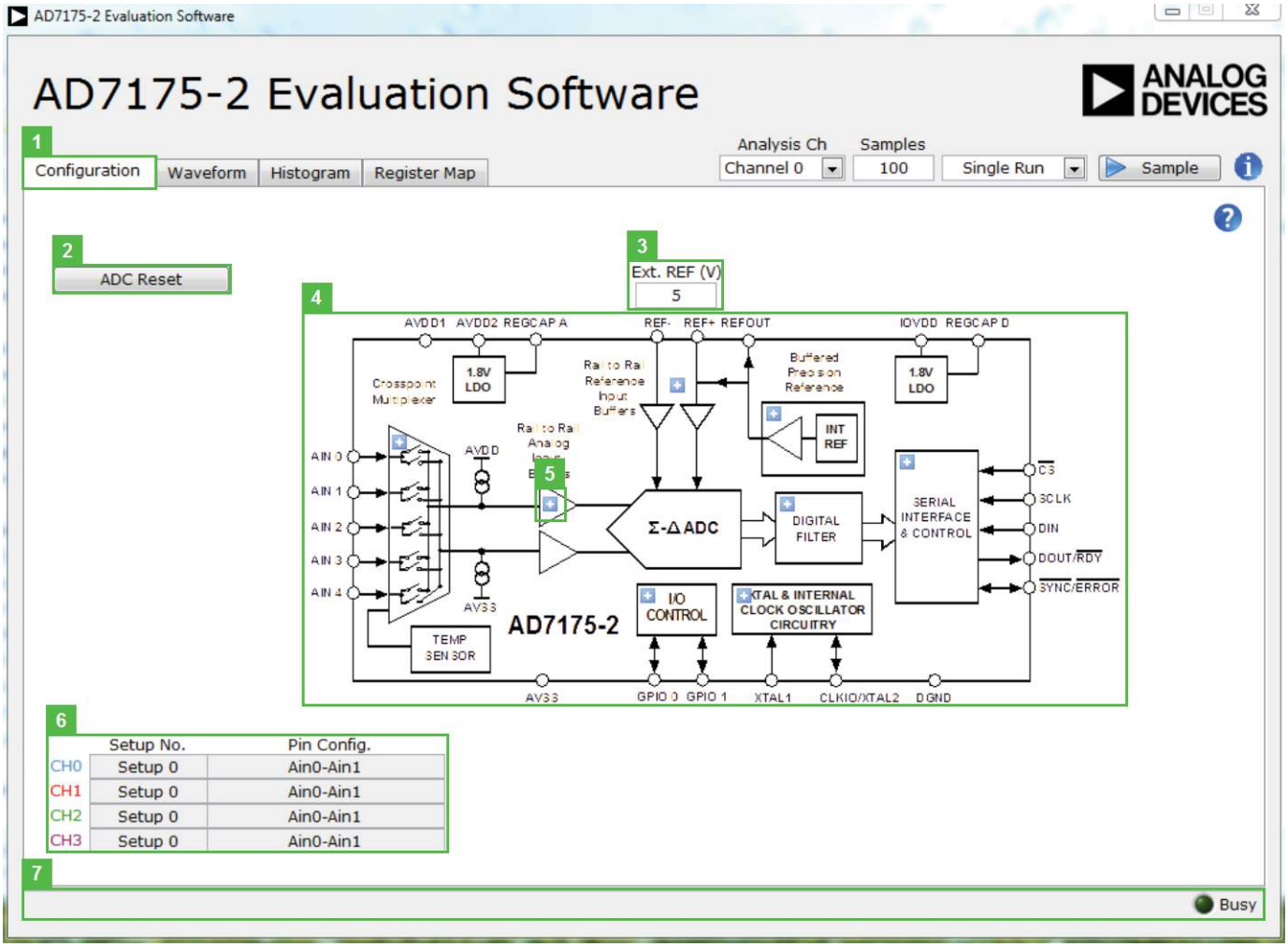

Figure 7. Configuration Tab of the AD7175-2 Evaluation Board Software

OVERVIEW OF THE MAIN WINDOW

The main window of the software displays the significant control buttons and analysis indicators of the AD7175-2 evaluation board software (see Figure 7). This window is divided into four tabs.

CONFIGURATION TAB (1)

ADC Reset (2)

Click **ADC Reset** to perform a software reset of the AD7175-2. There is no hardware reset pin. Perform a hard reset by removing power to the board. The software reset has the same effect as a hard reset.

Ext. Ref (3)

Sets the external reference voltage used for calculating the results on the Waveform and Histogram tabs. The evaluation board has an external 5 V ADR445 reference but this can be bypassed and so you can change the external reference voltage value here to ensure correct calculation of results on the Waveform and Histogram tabs.

Functional Block Diagram (4)

This is the functional block diagram of the ADC showing each of the separate functional blocks within the ADC. Clicking on one of the configuration buttons on this graph will open the configuration popup window for that block. Not all blocks will have a configuration button.

Configuration Popup Button (5)

This is one of the configuration popup buttons. Each button will open a different window allowing for configuration of the relevant functional block.

Channel Configuration Overview (6)

This section shows the channel configuration including setup and analog inputs. This allows for a quick check of how the ADC is setup.

Status Bar (7)

This section display status updates such as **Analysis Completed** and **Reset Completed** during software use as well as the software version and busy indicator.

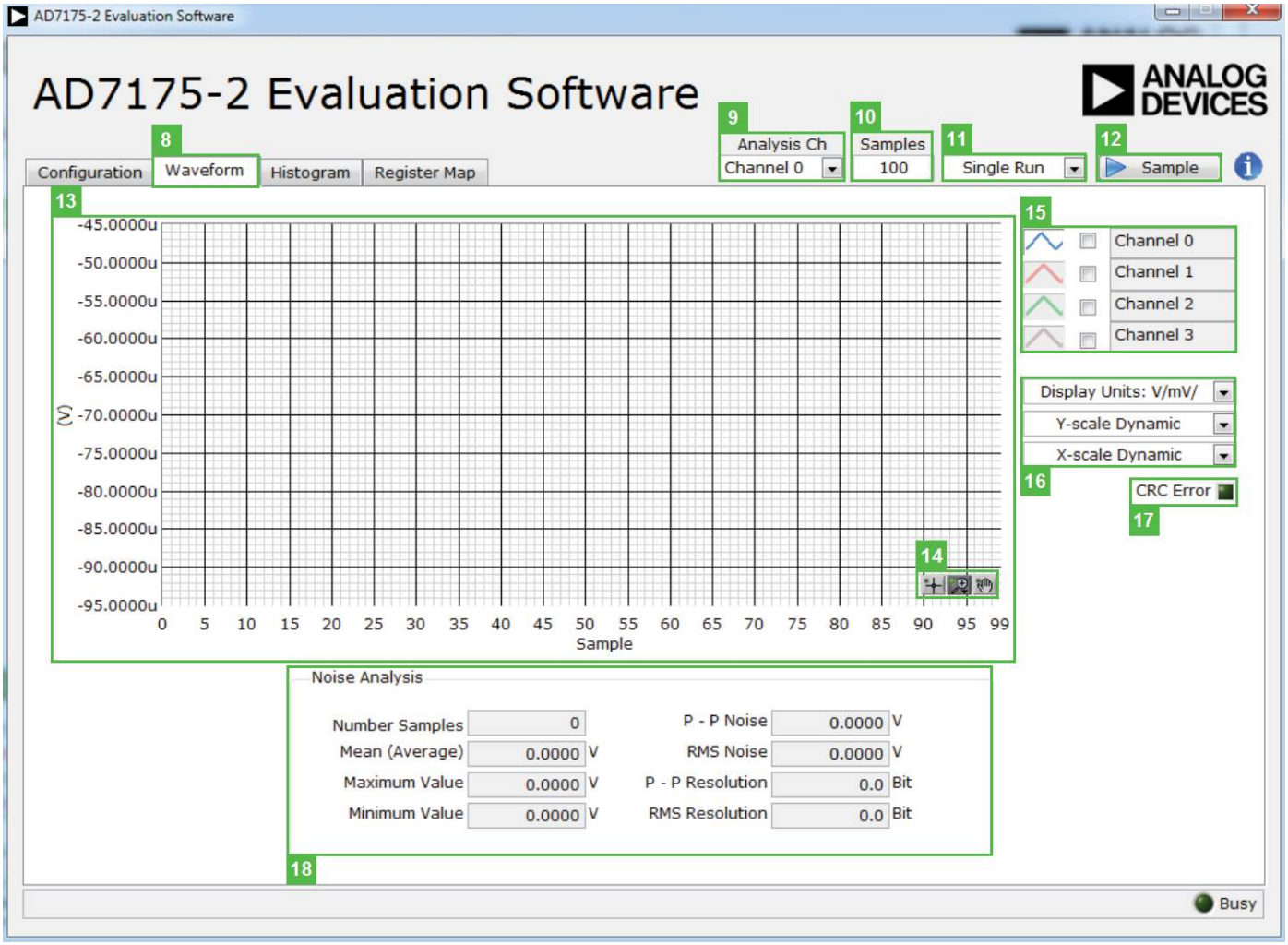

Figure 8. Waveform Tab of the AD7175-2 Evaluation Board Software

WAVEFORM TAB (8)

Analysis Channel (9)

The Noise Analysis section and Histogram Graph shows the analysis of the channel selected via this Analysis Channel control.

Samples (10 & 11)

The **Samples** (10) numeric control and batch control (11) set the number of samples gathered per batch and whether only a single batch of multiple batches of samples are gathered. This is unrelated to the ADC mode. You can capture a defined sample set, or continuously gather batches of samples. In both cases, the number of samples set in the **Samples** (10) numeric input dictates the number of samples.

Sample (12)

This starts gathering ADC results. Results appear in the Waveform Graph (13)

Waveform Graph and Controls(13 & 14)

The data waveform shows each successive sample of the ADC output. The control toolbar (14) in the graph allows you to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

Channel Selection (15)

This control allows you to choose which channels display on the data waveform. It also shows the analog inputs for that channel labeled next to the on and off controls. These controls only

affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

Display Units and Axis Controls(16)

Click **Display Units** to select whether the data graph displays in units of voltages or codes. This affects both the Waveform Graph and the Histogram Graph. The axis controls can be switched between dynamic and fixed. When "dynamic" is switched on the axis with automatically adjust to show the entire range of the ADC results after each batch of sample. When "fixed" is used the user can program the axis ranges and they will not adjust after each sample batch.

CRC Error (17)

This LED icon illuminates when a cyclic redundancy check (CRC) error is detected in the communications between the software and the AD7175-2. The CRC functionality on the AD7175-2 is disabled by default and must be enabled for this indicator to work.

Noise Analysis (18)

This section displays the results of the noise analysis for the selected analysis channel. This includes both noise and resolution measurements.

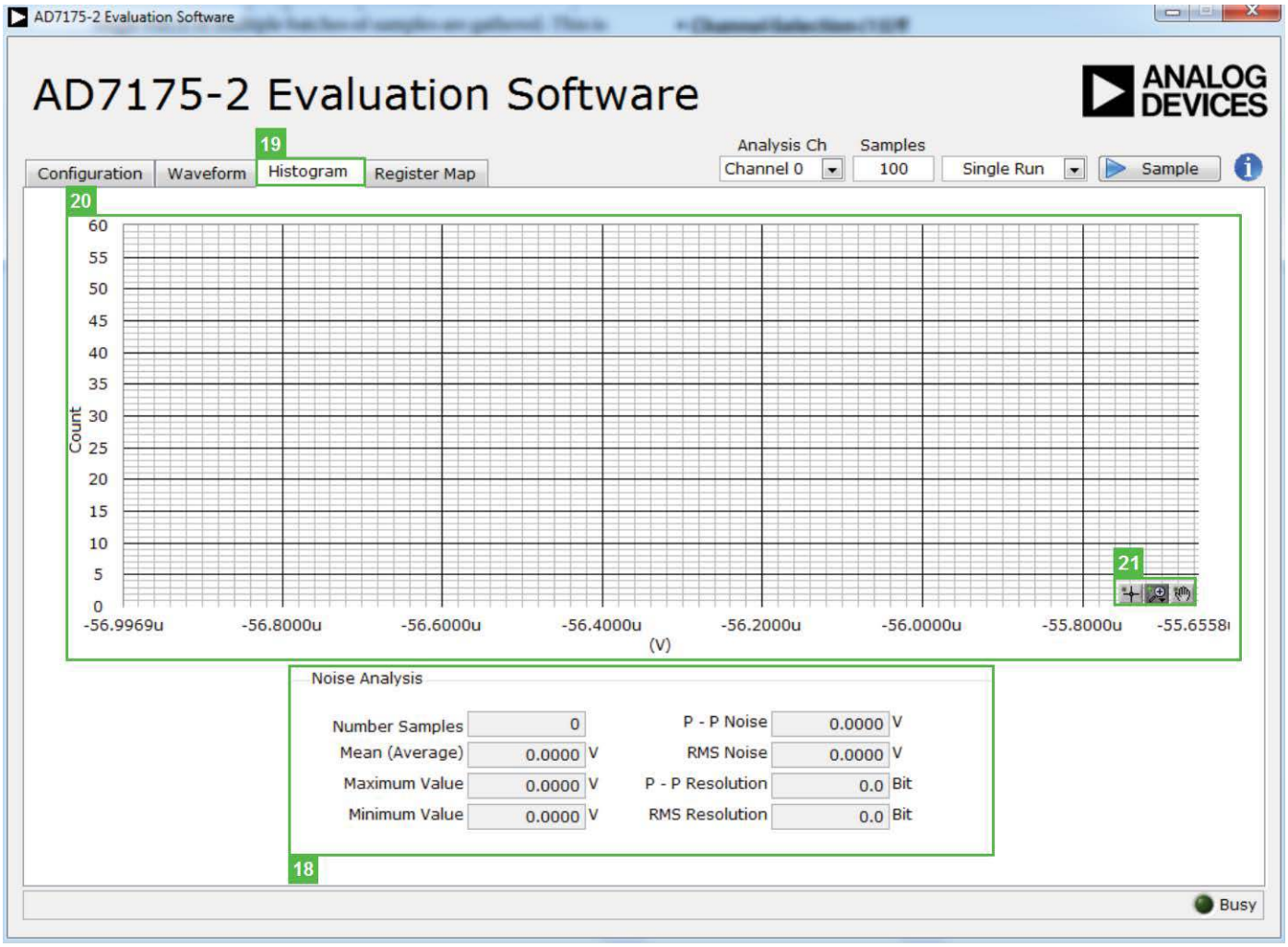

Figure 9. Waveform Tab of the AD7175-2 Evaluation Board Software

HISTOGRAM TAB (19)

Histogram Graph and Controls(20 & 21)

The data histogram shows each the number of times each sample of the ADC output occurs. The control toolbar (21) in the graph allows you to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

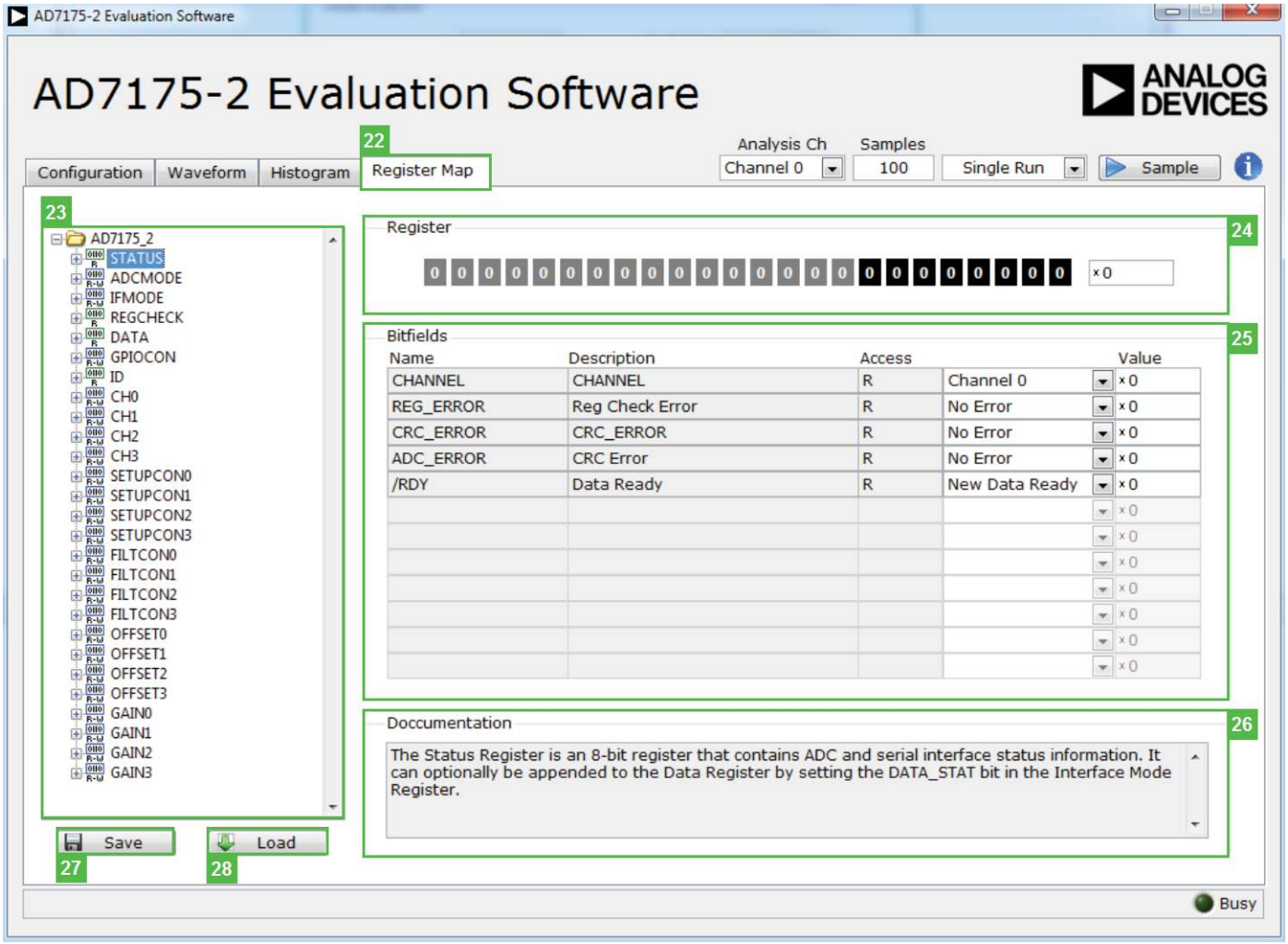

Figure 10. Register Map Tab of the AD7175-2 Evaluation Board Software

REGISTER MAP TAB (22)

Register Tree (23)

This control show the full register map in a tree control. Each register is shown and clicking on the expand button next to each register will show all the bitfields contained within that register.

Register Control (24)

This control allows the user to change the individual bit of the register selected in the Register Tree (23) by clicking on them or program the register value directly into the number control on the right.

Bitfield List(25)

This list shown all the bitfields of the register selected in the Register Tree (23). The values can be changed using the drop down menu or directly entering a value into the number control on the right.

Documentation (26)

This field contains the documentation for the register of bitfield selected in the Register Tree (23).

Save & Load (27 & 28)

These buttons allow the user to save the current register map setting to a file and load the setting from the same file.

EXITING THE SOFTWARE

To exit the software, click the close button at the top, right corner of the main window (see Figure 7).

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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