Transition-mode PFC Controller

FEATURES

- Transition - mode control of PFC pre-regulator
- Low input current THD
- Ultra-low (≤50μA) start up current
- Low (≤3.5 mA) quiescent current
- Precise internal reference voltage
- Zero-current switching
- Leading edge blanking instead of RC filtering
- Clamp gate output voltage
- Adjustable line compensation
- Adjustable Output Overvoltage Protection
- Vcc Over Voltage Protection
- Open control loop protection
- IC Over Temperature Protection(OTP)
- Disable function
- Dip-8/SOP-8 packages

APPLICATIONS

- IEC61000-3-2 compliant SMPS (TV, desktop PC, monitor) up to 150W
- Hi-end AC-DC adapter/charger
- Entry level server & web server

DESCRIPTION

The FT821x is a current-mode PFC controller operating in Transition Mode (TM). The FT821x has rich protections. It provides a controlled on-time to regulate the output DC voltage and achieve natural power factor correction.

The highly linear multiplier makes the device capable of working in wide input voltage range applications (from 85V to 265V) with an excellent THD.

The output voltage is controlled by means of a voltage-mode error amplifier and a precise internal voltage reference.

The device features extremely low consumption and includes a disable function suitable for IC remote ON/OFF control, which makes it easier to comply with energy saving norms.

An effective two-step OVP enables to safely handle overvoltages either occurring at start-up or resulting from load disconnection.

The totem-pole output stage is capable of driving a MOSFET or IGBT with source and sink currents of ± 400mA typically. The device is operating in transition mode and it is optimized for Electronic Lamp Ballast application, AC-DC adapters and SMPS.

TYPICAL APPLICATION CIRCUIT

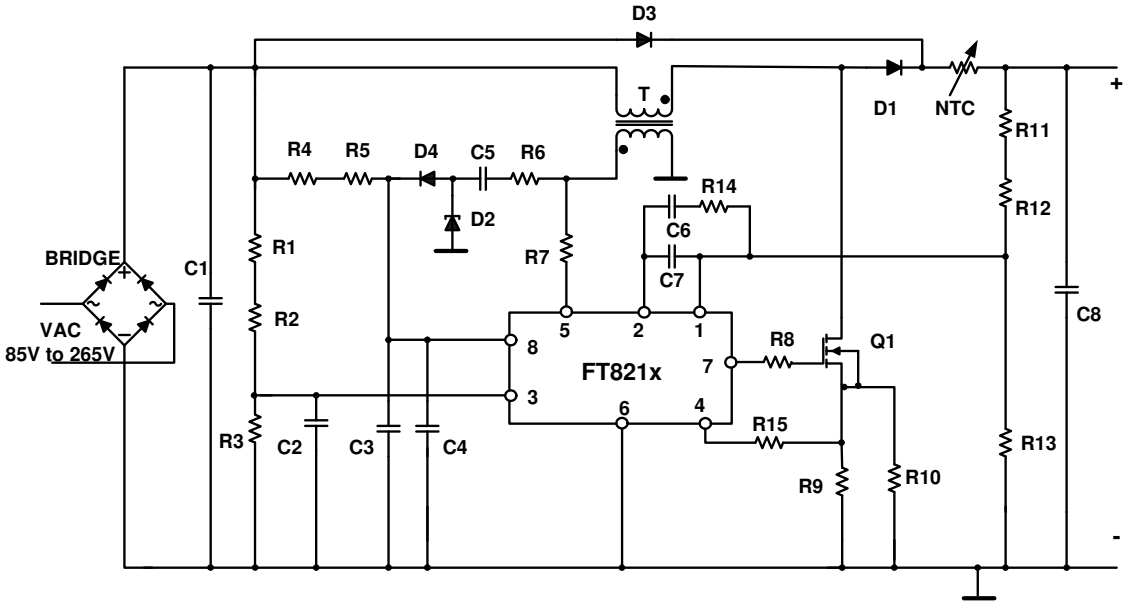


Figure 1: Typical Application Circuit

ABSOLUTE MAXIMUM RATINGS

Vcc to GND…… -0.3V to +28V
INV to GND ……..…… -0.3V to +7V
COMP to GND…….-0.3V to +7V
MULT to GND……. ..-0.3V to +7V
CS to GND……..... ... -0.3V to 7V
IZCD…… -5mA (source) / 5mA(sink)
Operating Temperature Range…… -40℃ to +125℃
Junction Temperature……. ...-40℃ to +150℃
Storage Temperature Range ……. -40℃ to +150℃
ESD Protection HBM…….3500V
ESD Protection MM……... ……... . 200V

*** Stresses exceed those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at conditions beyond those listed in the specification is not guaranteed. Prolonged exposure to extreme conditions may affect device reliability or functionality.**

PIN CONFIGURATION

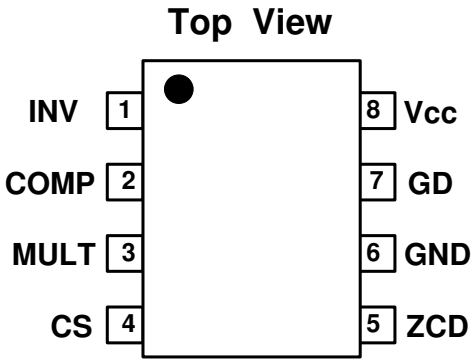


Figure 2: Pin Assignments

TERMINAL DESCRIPTION

No.	PIN	FUNCTION
1	INV	Inverting input of error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider. The pin also as an ON/OFF control input.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin #1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage together with line compensation voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground.
7	GD	Gate drive output. The totem pole output stage is able to drive power MOSFET's and IGBT's. The high-level voltage of this pin is clamped at about 14V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	V_{CC}	Supply Voltage of both the signal part of the IC and the gate driver.

Table1

ORDERING INFORMATION

FT821①②

DESIGNATOR	SYMBOL	DUAL OUTPUT VOLTAGE
①	A	NO
	B	YES
②	**SYMBOL**	**PACKAGE TYPE**
	a	SOP-8
	b	DIP-8

Table 2

MARKING RULE

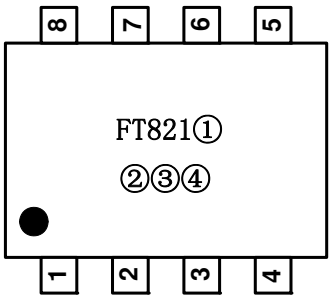


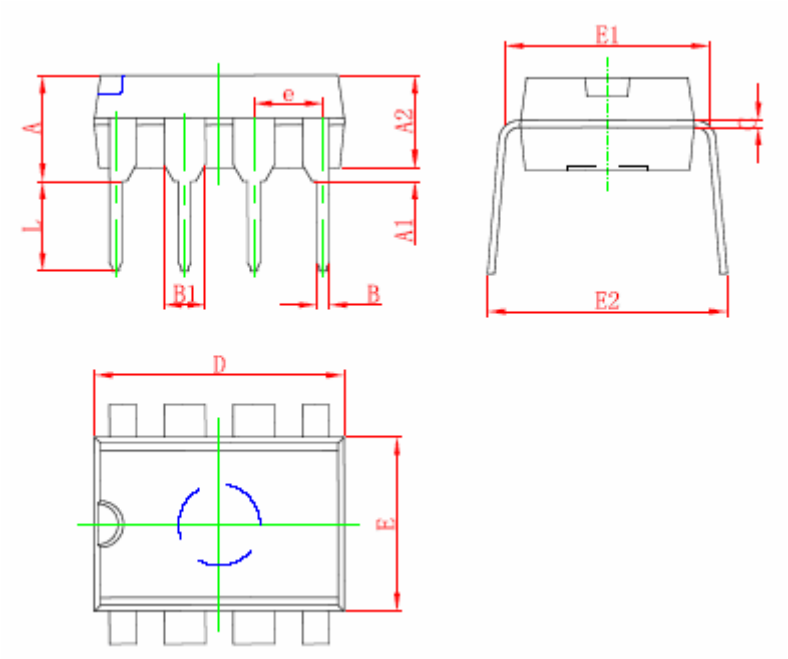
Figure 3

① Represent with or without dual output voltage function

②③④ for internal reference

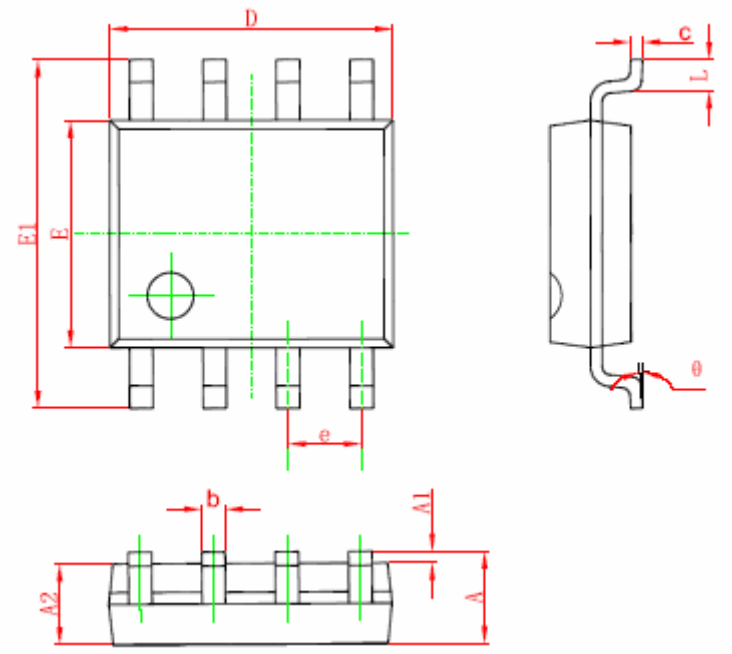
PAKAGING INFORMATION

DIP – 8 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524（BSC）		0.060（BSC）	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540 (BSC)		0.100（BSC）	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

SOP – 8 Package



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Mix	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050（BSC）	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°