



VC-715 LVPECL Voltage Controlled Crystal Oscillator



Features

- Small Industry Standard Package, 5.0 x 7.5 x 2.0 mm
- 19.44 MHz to 77.76 MHz Output Frequency
- 3.3 V Operation
- Fundamental crystal for ultra low jitter
- Complementary PECL Outputs
- Low phase noise and custom options
- 0/70 or -40/85° C operating temperature
- Enable /Disable (PECL)
- Lead Free

Applications

PLL circuits for Clock Smoothing and Frequency Translation

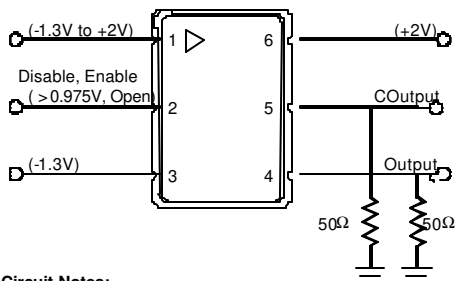
- Fiber Channel
- SONET
- SDH, ITU-T G.709
- SONET, GR-253-CORE Issue3

Description

The VC-715 is a voltage controlled crystal oscillator that operates at the fundamental frequency of the internal crystal. The crystal is a high-Q quartz device that enables the circuit to achieve low phase jitter performance over a wide operating temperature range. The oscillator is housed in an industry standard hermetically sealed leadless surface mount package and is available on tape and reel.

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Electrical Performance					
Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	f_o	19.440		77.76	MHz
Supply Voltage (+3.3 V)	V_{DD}	3.135	3.30	3.465	V
Supply Current	I_{DD}			<65	mA
Output Logic Levels					
Output Logic High	0 / 70 °C	V_{OH}	$V_{DD} - 1.025$	$V_{DD} - 0.880$	V
Output Logic Low	0 / 70 °C	V_{OL}	$V_{DD} - 1.810$	$V_{DD} - 1.620$	V
Output Logic High	-40 / 85 °C	V_{OH}	$V_{DD} - 1.085$	$V_{DD} - 0.880$	V
Output Logic Low	-40 / 85 °C	V_{OL}	$V_{DD} - 1.830$	$V_{DD} - 1.555$	V
Transition Times					
Rise Time	t_R			1	ns
Fall Time	t_F			1	ns
Symmetry or Duty Cycle	SYM	45	50	55	%
Operating temperature		0/70 or -40/85			°C
Test Conditions for APR	V_C	0.3		3.0	V
Absolute Pull Range	APR	± 50			ppm
Gain Transfer		Positive			ppm/V
Control Voltage Bandwidth (-3dB)	BW	10			kHz
Input Leakage, Control Voltage Input				± 1	μA
Package Size		5.0 x 7.5 x 2.0			mm



Test Circuit Notes:
 1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased [
 2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply
 3) 50Ω Terminations are Within Test Equipment.

Figure 1 Production Test Circuit

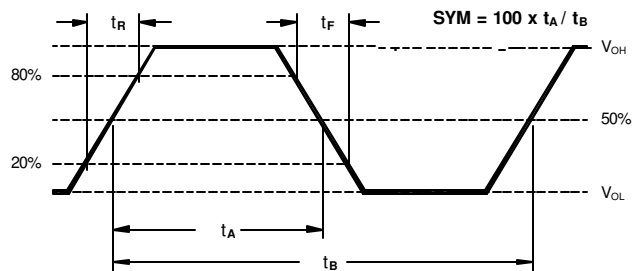
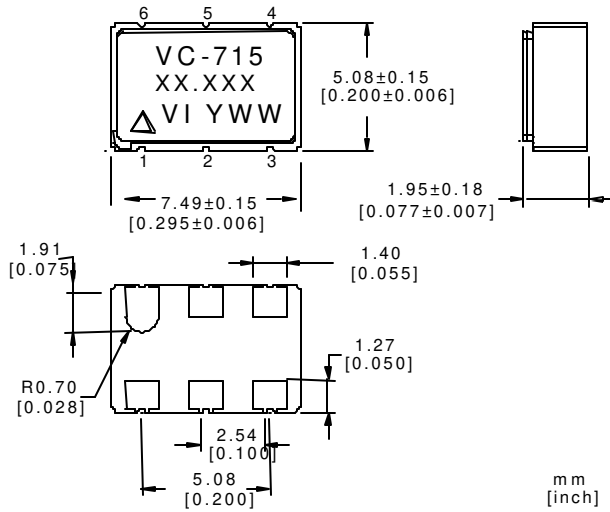


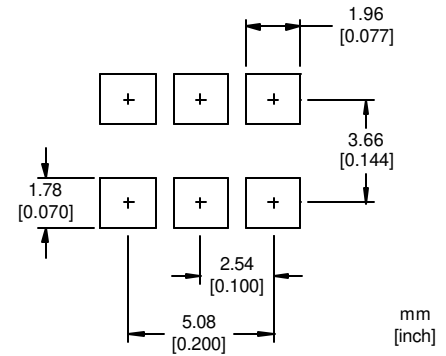
Figure 2. PECL Waveform

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Outline Diagram



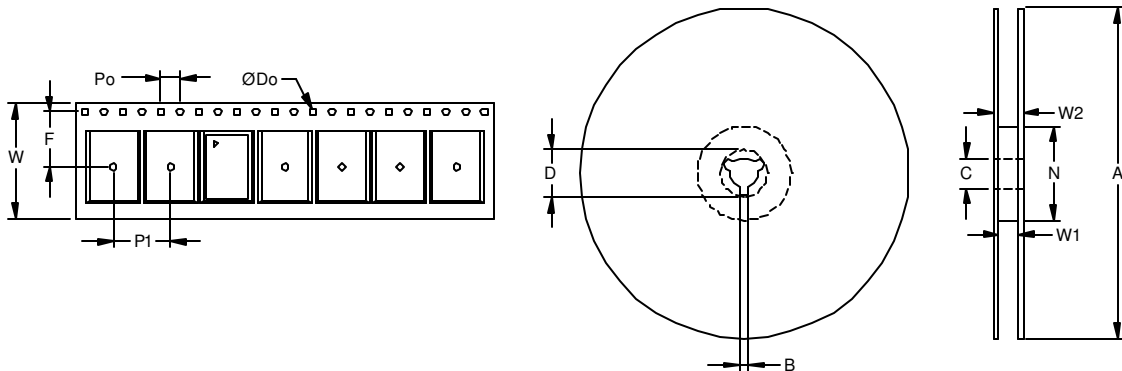
Pad Layout



Pin Out

Pin	Symbol	Function
1	V _c	VCXO Control Voltage
2	OE	Output Enable/Disable Enabled = PECL Logic 1 (or Open) Disabled = PECL Logic 0
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V _{cc}	Power Supply Voltage (3.3 V)

Tape and Reel (EIA-481-2-A)



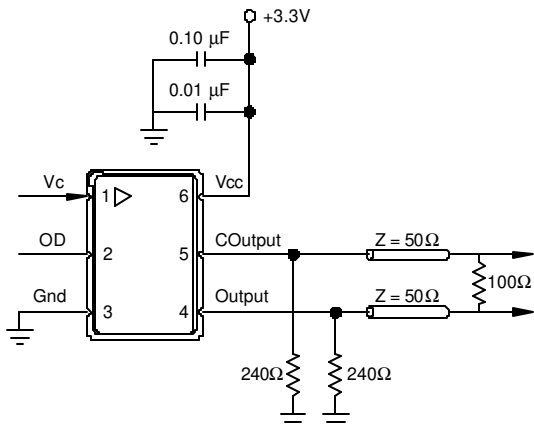
Tape Dimensions (mm)

Reel Dimensions (mm)

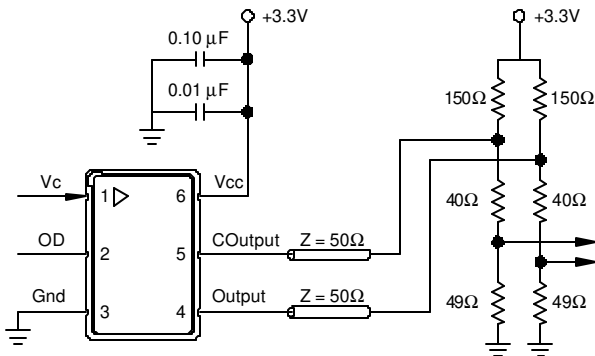
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	
VC-715	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

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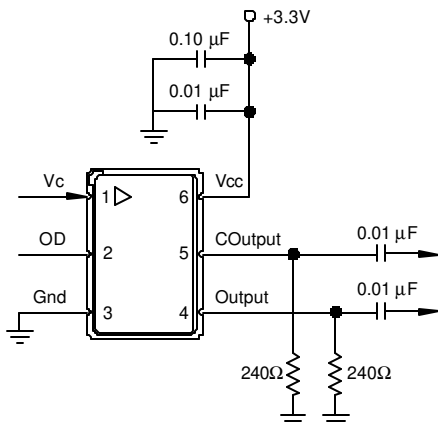
Suggested Output Load Configurations



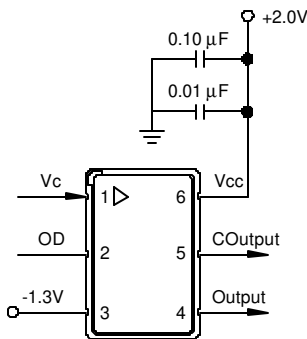
LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.



Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplies as shown. Similar to Figure 1.

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Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Output Current	I_{out}	25	mA
Voltage Control Range	V_c	0 to V_{CC}	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time ²	T_{LS}	240/10	°C/sec

1) Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

2) Contact pads are gold over nickel, the maximum solder temp can be lower, e.g. 220C.

Reliability

The VC-715 family is capable of meeting the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015

Handling Precautions

Although ESD protection circuitry has been designed into the VC-715 proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings

Model	Minimum	Conditions
Human Body Model	500	MIL-STD 883, Method 3015
Charged Device Model	500	JESD 22-C101

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-715's are hermetically sealed so an aqueous wash is not an issue. Contact pads are gold over nickel.

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Ordering Information

VC - 715 - D F F - G F L - 19.440

Product Family

VC: VCXO

Package

715: 5.0 x 7.5 x 2.8 mm
Low Frequency PECL

Input

D: 3.3 Vdc \pm 5%

Output

F: Complementary PECL

Frequency

Part Specific

Linearity, Stability

L: \pm 10 linearity, A: N/A

Enable - Disable

F: Pin 2

Absolute Pull Range

G: \pm 50 ppm

Operating Temperature

F: -40 to 85 °C

C: 0 to 70 °C

For Additional Information, Please Contact:



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