NX2114/2114A

300kHz & 600kHz SYNCHRONOUS PWM CONTROLLER

PRELIMINARY DATA SHEET

Pb Free Product

DESCRIPTION

The NX2114 controller IC is a synchronous Buck controller IC designed for step down DC to DC converter applications. Synchronous control operation replaces the traditional catch diode with an Nch MOSFET resulting in improved converter efficiency. Although the NX2114 controller is optimized to convert single 5V bus voltages to supplies as low as 0.8V output voltage, however using a few external components it can also be used for other input supplies such as 12V input (See NX2113 data sheet for more optimized solution). The NX2114 operates at 300kHz while 2114A is set at 600kHz operation which together with less than 50 nS of dead band provides an efficient and cost effective solution. Other features of the device are:
Internal digital soft start; Vcc undervoltage lock out; Output undervoltage protection with digital filter and shutdown capability via the enable pin.

FEATURES

- Synchronous Controller in 8 Pin Package
- Bus voltage operation from 2V to 25V
- Single 5V Supply Operation
- Short protection with feedback UVLO
- Internal 300kHz for 2114 and 600kHz for 2114A
- Internal Digital Soft Start Function
- Shut Down via pulling comp pin low
- Pb-free and RoHS compliant

APPLICATIONS

- Graphic Card on board converters
- Memory Vddq Supply in mother board applications
- On board DC to DC such as
  5V to 3.3V, 2.5V or 1.8V
- Hard Disk Drive
- Set Top Box

TYPICAL APPLICATION

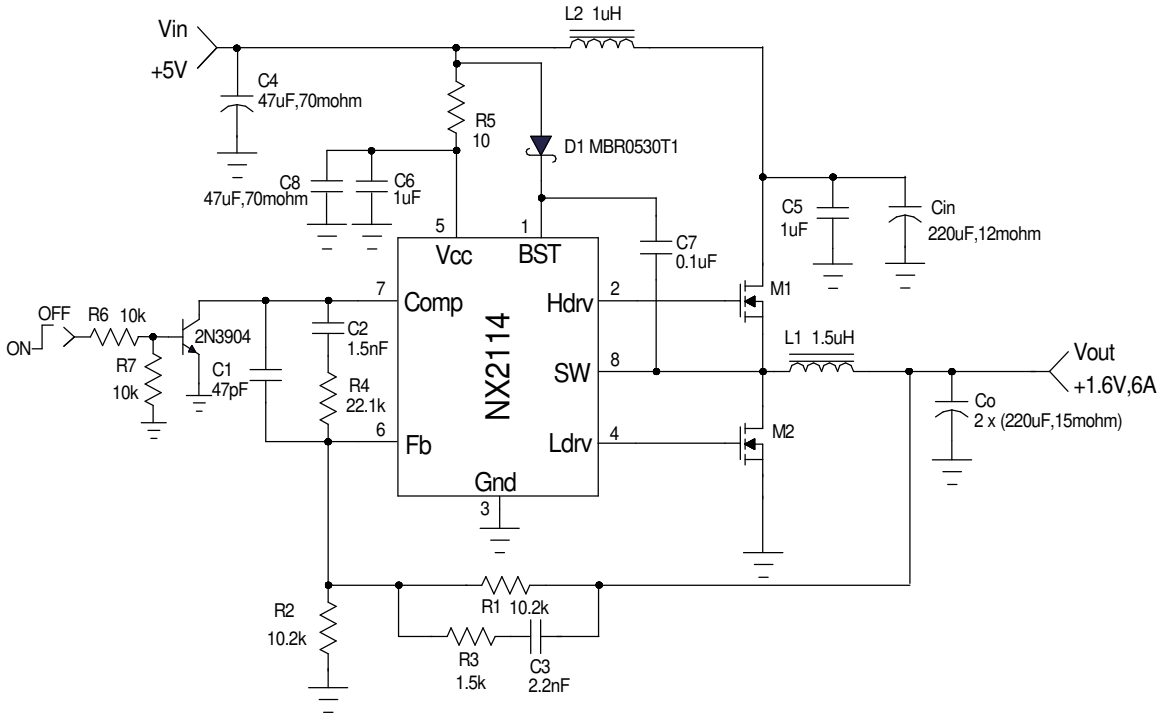

Figure1 - Typical application of 2114

ORDERING INFORMATION

Device	Temperature	Package	Frequency	Pb-Free
NX2114CSTR	0 to 70°C	SOIC-8L	300kHz	Yes
NX2114ACSTR	0 to 70° C	SOIC-8L	600kHz	Yes

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ABSOLUTE MAXIMUM RATINGS(NOTE1)

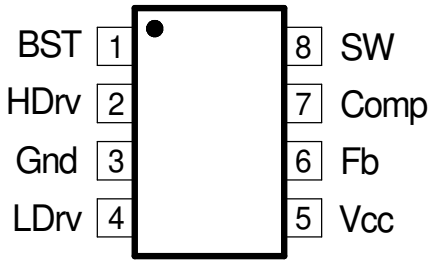
Vcc to GND & BST to SW voltage 6.5V
BST to GND Voltage 35V
Storage Temperature Range ..... -65°C to 150°C
Operating Junction Temperature Range ..... -40°C to 125°C

NOTE1: Stresses above those listed in "ABSOLUTE MAXIMUM RATINGS", may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

PACKAGE INFORMATION

8-PIN PLASTIC SOIC (S)

$\theta_{JA} \approx 130°C/W$



ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over Vcc = 5V, and T_A = 0 to 70°C. Typical values refer to T_A = 25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
Reference Voltage						
Ref Voltage	V_{REF}	4.5V<Vcc<5.5V		0.8		V
Ref Voltage line regulation				0.1		%
Supply Voltage(Vcc)						
V_{CC} Voltage Range	V_{CC}		4.5	5	5.5	V
V_{CC} Supply Current (Static)	I_{CC} (Static)	Outputs not switching		2.1		mA
V_{CC} Supply Current (Dynamic)	I_{CC} (Dynamic)	C_{LOAD}=3300pF F_S=300kHz		5		mA
Supply Voltage(V_{BST})						
V_{BST} Supply Current (Static)	I_{BST} (Static)	Outputs not switching		0.15		mA
V_{BST} Supply Current (Dynamic)	I_{BST} (Dynamic)	C_{LOAD}=3300pF F_S=300kHz		5		mA
Under Voltage Lockout						
V_{CC}-Threshold	V_{CC}_UVLO	V_{CC} Rising		4.2		V
V_{CC}-Hysteresis	V_{CC}_Hyst	V_{CC} Falling		0.22		V

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PARAMETER	SYM	Test Condition	Min	TYP	MAX	Units
SS						
Soft Start time	Tss	Fsw=300Khz, 2114		3.4		mS
Oscillator (Rt)						
Frequency	F_S	2114		300		kHz
		2114A		600		kHz
Ramp-Amplitude Voltage	V_{RAMP}			1.7		V
Max Duty Cycle				94		%
Min Duty Cycle					0	%
Error Amplifiers						
Transconductance				1900		umho
Input Bias Current	Ib			10		nA
Comp SD Threshold				0.3		V
FB Under Voltage Protection						
FB Under voltage threshold				0.4		V
High Side Driver(C_L=3300pF)						
Output Impedance , Sourcing Current	R_{source}(Hdrv)	I=200mA		1.1		ohm
Output Impedance , Sinking Current	R_{sink}(Hdrv)	I=200mA		0.8		ohm
Output Sourcing Current		V_{BST}-V_{HDRV}=5V		2		A
Output Sinking Current		V_{HDRV}-V_{SW}=5V		2		A
Rise Time	THdrv(Rise)	10% to 90%		50		ns
Fall Time	THdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(L to H)	Ldrv going Low to Hdrv going High, 10%-10%		30		ns
Low Side Driver (C_L=3300pF)						
Output Impedance, Sourcing Current	R_{source}(Ldrv)	I=200mA		1.1		ohm
Output Impedance, Sinking Current	R_{sink}(Ldrv)	I=200mA		0.5		ohm
Output Sourcing Current		V_{PVCC}-V_{LDRV}=5V		2		A
Output Sinking Current		V_{LDRV}-PGND=5V		4		A
Rise Time	TLdrv(Rise)	10% to 90%		50		ns
Fall Time	TLdrv(Fall)	90% to 10%		50		ns
Deadband Time	Tdead(H to L)	SW going Low to Ldrv going High, 10% to 10%		30		ns

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PIN DESCRIPTIONS

PIN #	PIN SYMBOL	PIN DESCRIPTION
1	BST	This pin supplies voltage to the high side driver. A high frequency ceramic capacitor of 0.1 to 1 uF must be connected from this pin to SW pin.
2	HDRV	High side MOSFET gate driver.
3	GND	Ground pin.
4	LDRV	Low side MOSFET gate driver.
5	Vcc	Voltage supply for the internal circuit as well as the low side MOSFET gate driver. A 1uF high frequency ceramic capacitor must be connected from this pin to GND pin.
6	FB	This pin is the error amplifier inverting input. This pin is also connected to the output UVLO comparator. When this pin falls below 0.4V, both HDRV and LDRV outputs are latched off.
7	COMP	This pin is the output of the error amplifier and together with FB pin is used to compensate the voltage control feedback loop. This pin is also used as a shut down pin. When this pin is pulled below 0.3V, both drivers are turned off and internal soft start is reset.
8	SW	This pin is connected to the source of the high side MOSFET and provides return path for the high side driver.

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BLOCK DIAGRAM

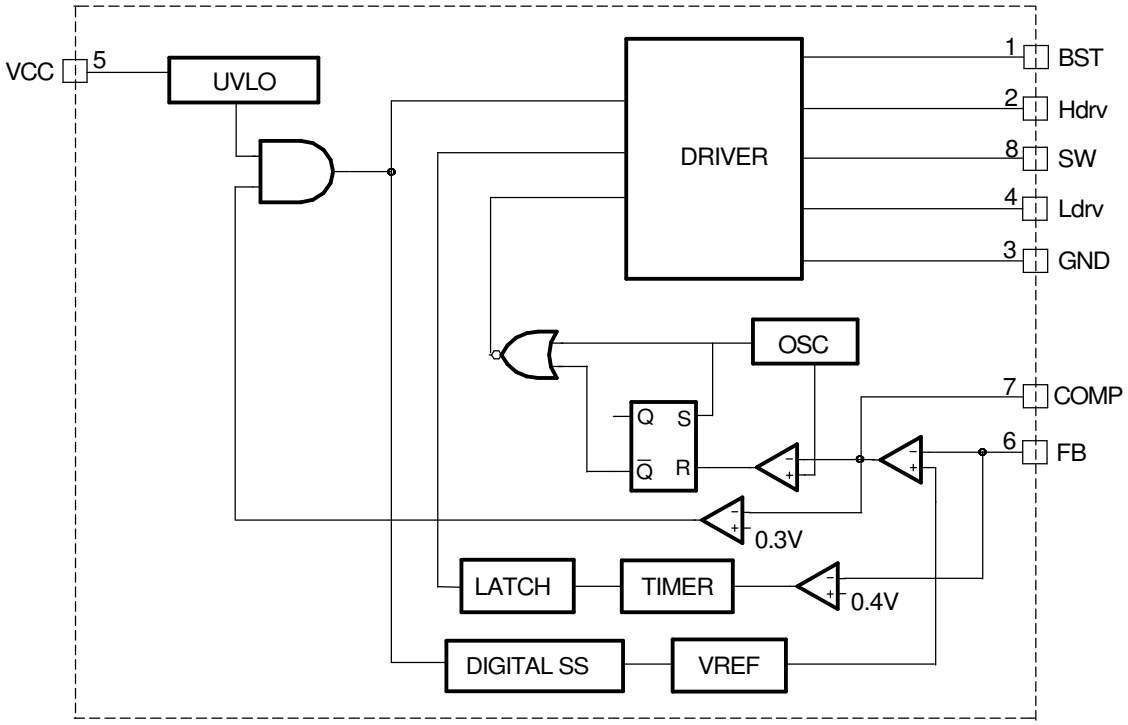

Figure 1 - Simplified block diagram of the NX2114

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Demoboard design and waveforms

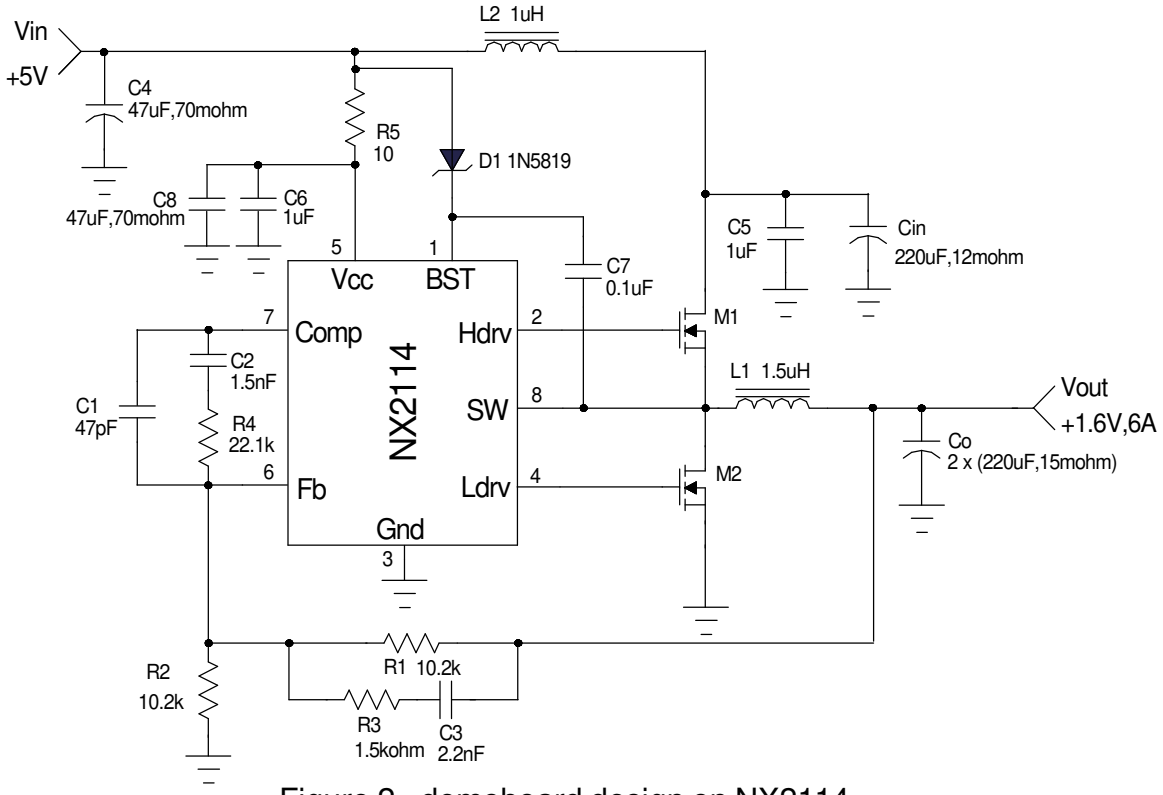

Figure 2 - demoboard design on NX2114

Bill of Material

Name	Component description	Vendor	Vendor P/N	Number
R1	10.2k 1% chip resistor			1
R2	10.2k 1% chip resistor			1
R3	1.5k 1% chip resistor			1
R4	22.1k 1% chip resistor			1
R5	10 chip resistor			1
C1	47pF ceramic			1
C2	1.5nF ceramic			1
C3	2.2nF ceramic			1
C4,C8	47uF,16V,70mohm,SMD	Sanyo	16TQC47M	1
C5,C6	1uF ceramic			1
C7	0.1uF ceramic			1
C_{IN}	220uF,6.3V,12mohm,SMD	Sanyo	6TPD220M	1
C_O	220uF,4V,15mohm,SMD	Sanyo	4TPE220MF	2
D1	Diode		D1N5819	1
M1,M2	MOSFET	Fairchild	FDS6294	1
L1	1.5uH,6.8A	Coilcraft	DO3316P-152	1
L2	1uH,6.4A	Coilcraft	DO3316P-102	1

Note: To make sure short circuit protection of device functions correctly, C8 and R5 are necessary for filtering noise in single power supply design.

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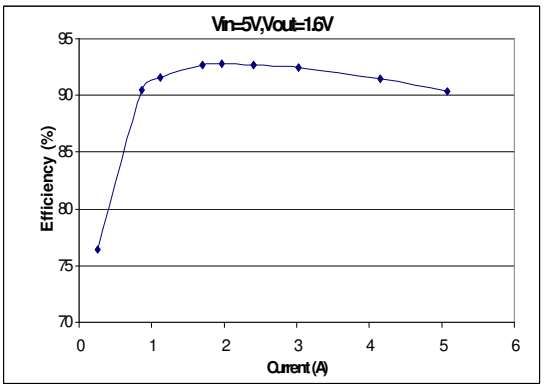

Figure 3: Output efficiency

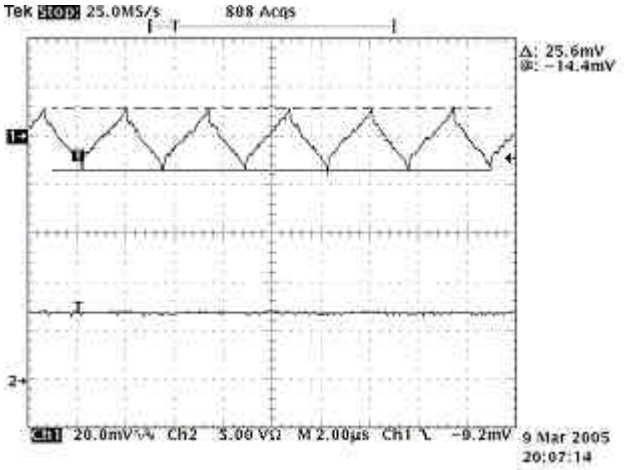

Figure 4: Voltage ripple @1.6 V output voltage, 7A output current

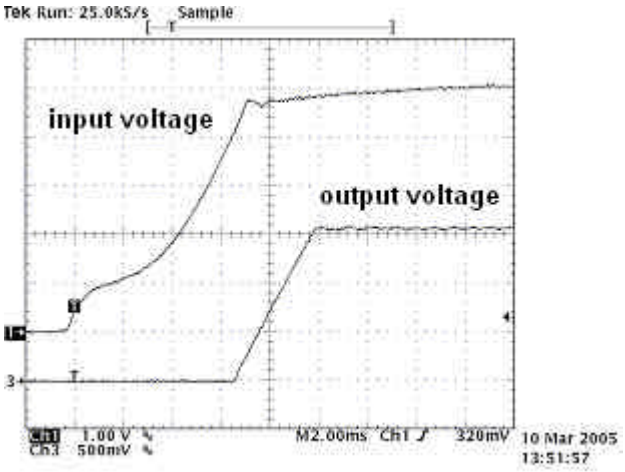

Figure 5: Start up time

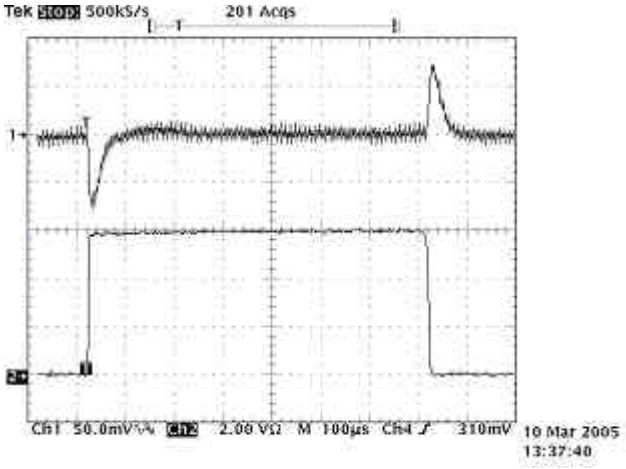

Figure 6: Output voltage transient response for load curent 0A-6A

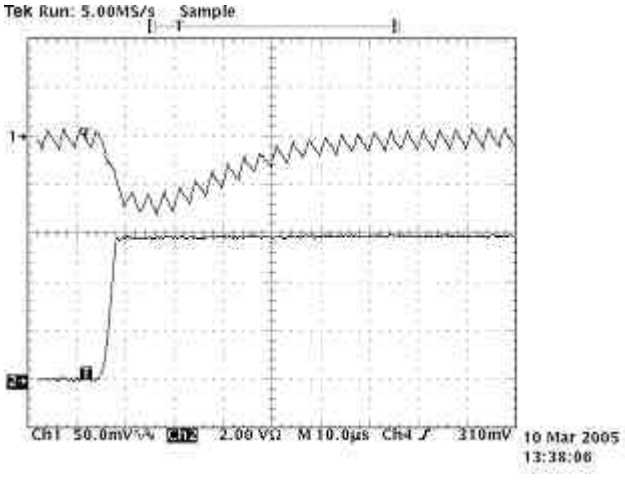

Figure 7: Output voltage droop during transient(0A-6A)

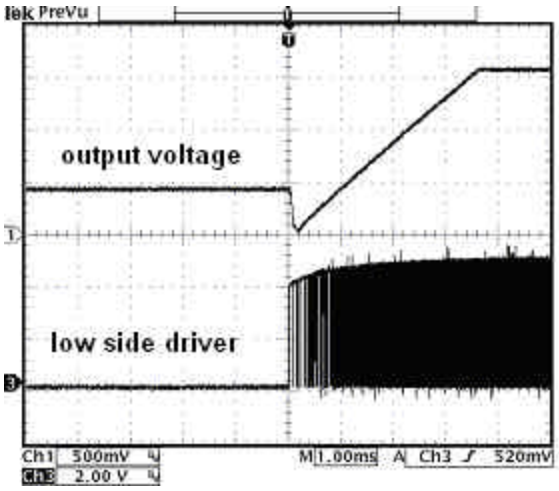

Figure 8: Startup operation waveform

APPLICATION INFORMATION

Symbol Used In Application Information:

V_{IN} - Input voltage
V_{OUT} - Output voltage
I_{OUT} - Output current
ΔV_{RIPPLE} - Output voltage ripple
F_S - Working frequency
ΔI_{RIPPLE} - Inductor current ripple

Design Example

The following is typical application for NX2114, the schematic is figure 2.

V_{IN} = 5V
V_{OUT}=1.6V
I_{OUT}=6A
ΔV_{RIPPLE} <=20mV
ΔV_{DROOP}<=60mV @ 6A step

Output Inductor Selection

The selection of inductor value is based on inductor ripple current, power rating, working frequency and efficiency. Larger inductor value normally means smaller ripple current. However if the inductance is chosen too large, it brings slow response and lower efficiency. Usually the ripple current ranges from 20% to 40% of the output current. This is a design freedom which can be decided by design engineer according to various application requirements. The inductor value can be calculated by using the following equations:

$$L_{OUT} = \frac{V_{IN} - V_{OUT}}{\Delta I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_S} \quad ...(1)$$

$$I_{RIPPLE} = k \times I_{OUTPUT}$$

where k is between 0.2 to 0.4.
Select k=0.4, then

$$L_{OUT} = \frac{5V-1.6V}{0.4 \times 6A} \times \frac{1.6V}{5V} \times \frac{1}{300kHz}$$

L_{OUT}=1.51uH

Choose inductor from COILCRAFT DO3316P-152 with L=1.5uH is a good choice.

Current Ripple is recalculated as

$$\Delta I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{L_{OUT}} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_S}$$

$$= \frac{5V-1.6V}{1.5uH} \times \frac{1.6v}{5v} \times \frac{1}{300kHz} = 2.4A \quad ...(2)$$

Output Capacitor Selection

Output capacitor is basically decided by the amount of the output voltage ripple allowed during steady state(DC) load condition as well as specification for the load transient. The optimum design may require a couple of iterations to satisfy both condition.

Based on DC Load Condition

The amount of voltage ripple during the DC load condition is determined by equation(3).

$$\Delta V_{RIPPLE} = ESR \times \Delta I_{RIPPLE} + \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \quad ...(3)$$

Where ESR is the output capacitors' equivalent series resistance,C_{OUT} is the value of output capacitors.

Typically when large value capacitors are selected such as Aluminum Electrolytic,POSCAP and OSCON types are used, the amount of the output voltage ripple is dominated by the first term in equation(3) and the second term can be neglected.

For this example, POSCAP are chosen as output capacitors, the ESR and inductor current typically determines the output voltage ripple.

$$ESR_{desire} = \frac{\Delta V_{RIPPLE}}{\Delta I_{RIPPLE}} = \frac{20mV}{2.3A} = 8.6m\Omega \quad ...(4)$$

If low ESR is required, for most applications, multiple capacitors in parallel are better than a big capacitor. For example, for 20mV output ripple, POSCAP 4TPE220MF with 15mΩ are chosen.

$$N = \frac{ESR_E \times \Delta I_{RIPPLE}}{\Delta V_{RIPPLE}} \quad ...(5)$$

Number of Capacitor is calculated as

$$N = \frac{15m\Omega \times 2.3A}{20mV}$$

N =1.8

The number of capacitor has to be round up to a integer. Choose N =2.

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If ceramic capacitors are chosen as output capacitors, both terms in equation (3) need to be evaluated to determine the overall ripple. Usually when this type of capacitors are selected, the amount of capacitance per single unit is not sufficient to meet the transient specification, which results in parallel configuration of multiple capacitors.

For example, one 100uF, X5R ceramic capacitor with 2mΩ ESR is used. The amount of output ripple is

$$\Delta V_{RIPPLE} = 2m\Omega \times 2.3A + \frac{2.3A}{8 \times 300kHz \times 100uF}$$
$$= 4.6mV + 9.6mV = 13.2mV$$

Although this meets DC ripple spec, however it needs to be studied for transient requirement.

Based On Transient Requirement

Typically, the output voltage droop during transient is specified as:

$\Delta V_{DROOP} < \Delta V_{TRAN}$ @ step load ΔI_{STEP}

During the transient, the voltage droop during the transient is composed of two sections. One Section is dependent on the ESR of capacitor, the other section is a function of the inductor, output capacitance as well as input, output voltage. For example, for the overshoot, when load from high load to light load with a ΔI_{STEP} transient load, if assuming the bandwidth of system is high enough, the overshoot can be estimated as the following equation.

$$\Delta V_{overshoot} = ESR \times \Delta I_{step} + \frac{V_{OUT}}{2 \times L \times C_{OUT}} \times \tau^2 \quad ...(6)$$

where τ is the a function of capacitor, etc.

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR \times C_{OUT} & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(7)$$

where

$$L_{crit} = \frac{ESR \times C_{OUT} \times V_{OUT}}{\Delta I_{step}} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} \quad ...(8)$$

where ESR_E and C_E represents ESR and capacitance of each capacitor if multiple capacitors are used in parallel.

The above equation shows that if the selected output inductor is smaller than the critical inductance, the voltage droop or overshoot is only dependent on the ESR of output capacitor. For low frequency capacitor such as electrolytic capacitor, the product of ESR and capacitance is high and $L \le L_{crit}$ is true. In that case, the transient spec is dependent on the ESR of capacitor.

In most cases, the output capacitors are multiple capacitors in parallel. The number of capacitors can be calculated by the following

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2 \quad ...(9)$$

where

$$\tau = \begin{cases} 0 & \text{if} \quad L \le L_{crit} \\ \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E & \text{if} \quad L \ge L_{crit} \end{cases} \quad ...(10)$$

For example, assume voltage droop during transient is 100mV for 6A load step.

If the POSCAP 2R5TPE220MC (220uF, 12mΩ) is used, the critical inductance is given as

$$L_{crit} = \frac{ESR_E \times C_E \times V_{OUT}}{\Delta I_{step}} =$$
$$\frac{15m\Omega \times 220\mu F \times 1.6V}{6A} = 0.88\mu H$$

The selected inductor is 1.5uH which is bigger than critical inductance. In that case, the output voltage transient not only dependent on the ESR, but also capacitance.

number of capacitors is

$$\tau = \frac{L \times \Delta I_{step}}{V_{OUT}} - ESR_E \times C_E$$
$$= \frac{1.5\mu H \times 6A}{1.6V} - 15m\Omega \times 220\mu F = 2.3us$$

$$N = \frac{ESR_E \times \Delta I_{step}}{\Delta V_{tran}} + \frac{V_{OUT}}{2 \times L \times C_E \times \Delta V_{tran}} \times \tau^2$$
$$= \frac{15m\Omega \times 6A}{60mV} +$$
$$\frac{1.6V}{2 \times 1.5\mu H \times 220\mu F \times 60mV} \times 2.3us^2$$
$$= 1.7$$

The number of capacitors has to satisfied both ripple and transient requirement. Overall, we can choose N=2.

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It should be considered that the proposed equation is based on ideal case, in reality, the droop or overshoot is typically more than the calculation. The equation gives a good start. For more margin, more capacitors have to be chosen after the test. Typically, for high frequency capacitor such as high quality POSCAP especially ceramic capacitor, 20% to 100% (for ceramic) more capacitors have to be chosen since the ESR of capacitors is so low that the PCB parasitic can affect the results tremendously. More capacitors have to be selected to compensate these parasitic parameters.

Compensator Design

Due to the double pole generated by LC filter of the power stage, the power system has 180° phase shift , and therefore, is unstable by itself. In order to achieve accurate output voltage and fast transient response, compensator is employed to provide highest possible bandwidth and enough phase margin. Ideally, the Bode plot of the closed loop system has crossover frequency between 1/10 and 1/5 of the switching frequency, phase margin greater than 50° and the gain crossing 0dB with -20dB/decade. Power stage output capacitors usually decide the compensator type. If electrolytic capacitors are chosen as output capacitors, type II compensator can be used to compensate the system, because the zero caused by output capacitor ESR is lower than crossover frequency. Otherwise type III compensator should be chosen.

A. Type III compensator design

For low ESR output capacitors, typically such as Sanyo oscap and poscap, the frequency of ESR zero caused by output capacitors is higher than the crossover frequency. In this case, it is necessary to compensate the system with type III compensator. The following figures and equations show how to realize the type III compensator by transconductance amplifier.

$$F_{Z1} = \frac{1}{2\times\pi\times R_4\times C_2} \quad ...(11)$$

$$F_{Z2} = \frac{1}{2\times\pi\times(R_2+R_3)\times C_3} \quad ...(12)$$

$$F_{P1} = \frac{1}{2\times\pi\times R_3\times C_3} \quad ...(13)$$

$$F_{P2} = \frac{1}{2\times\pi\times R_4\times\frac{C_1\times C_2}{C_1+C_2}} \quad ...(14)$$

where F_{Z1},F_{Z2},F_{P1} and F_{P2} are poles and zeros in the compensator. Their locations are shown in figure 10.

The transfer function of type III compensator for transconductance amplifier is given by:

$$\frac{V_e}{V_{OUT}} = \frac{1-g_m\times Z_f}{1+g_m\times Z_{in}+Z_{in}/R_1}$$

For the voltage amplifier, the transfer function of compensator is

$$\frac{V_e}{V_{OUT}} = \frac{-Z_f}{Z_{in}}$$

To achieve the same effect as voltage amplifier, the compensator of transconductance amplifier must satisfy this condition: R4>>2/gm. R1||R2||R3>>1/gm is desirable.

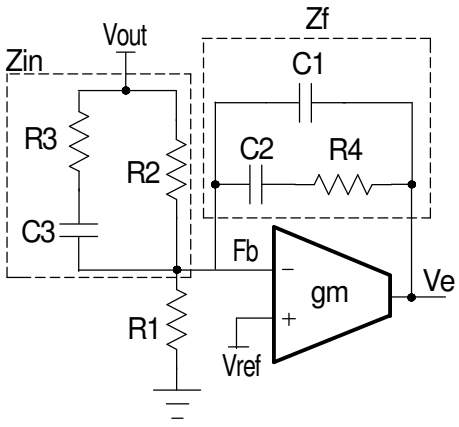

Figure 9 - Type III compensator using transconductance amplifier

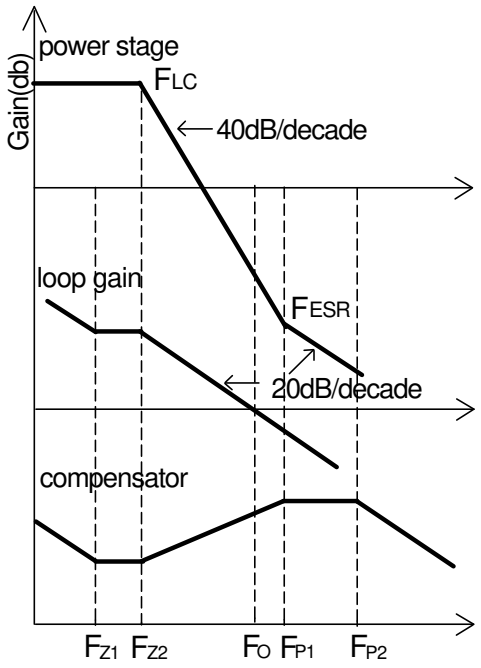

Figure 10 - Bode plot of Type III compensator

Design example for type III compensator are in order. The crossover frequency has to be selected as $F_{LC}<F_O<F_{ESR,}$ and $F_O<=1/10\sim1/5F_{s.}$

1. Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC}=\frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}}=\frac{1}{2\times\pi\times\sqrt{1.5uH\times 440uF}}=6.2kHz$$

$$F_{ESR}=\frac{1}{2\times\pi\times ESR\times C_{OUT}}=\frac{1}{2\times\pi\times 7.5m\Omega\times 440uF}=48kHz$$

2. Set R_2 equal to10.2kΩ, then R_1= 10.2kΩ.

3. Set zero $F_{Z2} = F_{LC}$ and $F_{p1} = F_{ESR}$.

4. Calculate R_4 and C_3 with the crossover frequency at 1/10~ 1/5 of the switching frequency. Set F_O=30kHz.

$$C_3=\frac{1}{2\times\pi\times R_2}\times\left(\frac{1}{F_{z2}}-\frac{1}{F_{p1}}\right)=\frac{1}{2\times\pi\times 10k\Omega}\times\left(\frac{1}{6.2kHz}-\frac{1}{48kHz}\right)=2.2nF$$

$$R_4=\frac{V_{OSC}}{V_{in}}\times\frac{2\times\pi\times F_O\times L}{C_3}\times C_{out}=\frac{1.7V}{5V}\times\frac{2\times\pi\times 30kHz\times 1.5uH}{2.2nF}\times 440uF=19.2k\Omega$$

Choose C_3=2.2nF, R_4=22.1kΩ.

5. Calculate C_2 with zero F_{z1} at 75% of the LC double pole by equation (11).

$$C_2=\frac{1}{2\times\pi\times F_{Z1}\times R_4}=\frac{1}{2\times\pi\times 0.75\times 6.2kHz\times 22.1k\Omega}=1.55nF$$

Choose C_2=1.5nF.

6. Calculate C_1 by equation (14) with pole F_{p2} at half the switching frequency.

$$C_1=\frac{1}{2\times\pi\times R_4\times F_{P2}}=\frac{1}{2\times\pi\times 22.1k\Omega\times 150kHz}=48pF$$

Choose C_1=47pF.

7. Calculate R_3 by equation (13).

$$R_3=\frac{1}{2\times\pi\times F_{P1}\times C_3}=\frac{1}{2\times\pi\times 48kHz\times 2.2nF}=1.5k\Omega$$

Choose R_3=1.5kΩ.

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B. Type II compensator design

If the electrolytic capacitors are chosen as power stage output capacitors, usually the Type II compensator can be used to compensate the system.

Type II compensator can be realized by simple RC circuit without feedback as shown in figure 12. R3 and C1 introduce a zero to cancel the double pole effect. C2 introduces a pole to suppress the switching noise. The following equations show the compensator pole zero location and constant gain.

$$Gain = g_m \times \frac{R_1}{R_1+R_2} \times R_3 \quad \text{... (15)}$$

$$F_z = \frac{1}{2\times\pi\times R_3\times C_1} \quad \text{... (16)}$$

$$F_p \approx \frac{1}{2\times\pi\times R_3\times C_2} \quad \text{... (17)}$$

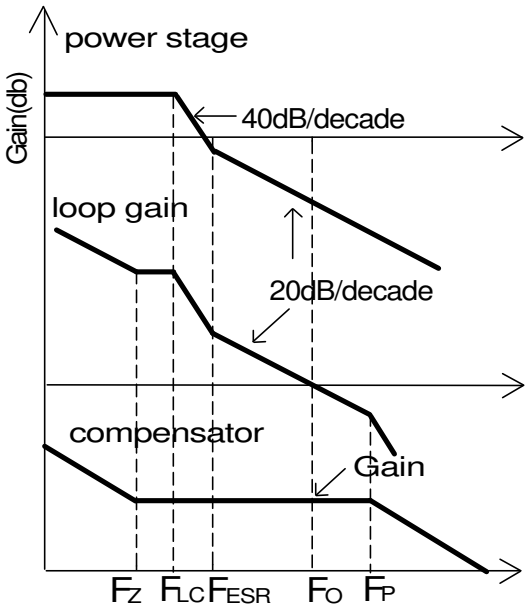

Figure 11- Bode plot of Type II compensator

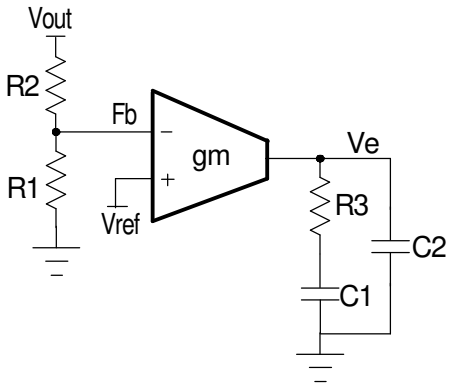

Figure 12 - Type II compensator with transconductance amplifier

For this type of compensator, F_O has to satisfy $F_{LC}<F_{ESR}<<F_O<=1/10\sim1/5F_s$.

The following uses typical design in figure 19 as an example for type II compensator design, two 680uF with 41mΩ electrolytic capacitors are used.

1.Calculate the location of LC double pole F_{LC} and ESR zero F_{ESR}.

$$F_{LC} = \frac{1}{2\times\pi\times\sqrt{L_{OUT}\times C_{OUT}}} = \frac{1}{2\times\pi\times\sqrt{1.5uH\times1360uF}} = 3.5kHz$$

$$F_{ESR} = \frac{1}{2\times\pi\times ESR\times C_{OUT}} = \frac{1}{2\times\pi\times20.5m\Omega\times1360uF} = 5.7kHz$$

2.Set R_2 equal to10.2kΩ. Using equation 18, the final selection of R_1 is 3.24kΩ.

3. Set crossover frequency at 1/10~ 1/5 of the swithing frequency, here F_O=30kHz.

4.Calculate R_3 value by the following equation.

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$$R_3 = \frac{V_{OSC}}{V_{in}} \times \frac{2 \times \pi \times F_O \times L}{R_{ESR}} \times \frac{1}{g_m} \times \frac{R_1 + R_2}{R_1}$$
$$= \frac{1.7V}{12} \times \frac{2 \times \pi \times 30kHz \times 1.5uH}{20.5\Omega} \times \frac{1}{1.9mA/V} \times \frac{10.2k\Omega + 3.24k\Omega}{3.24k\Omega}$$
$$= 4.23k\Omega$$

Choose R_3 =4.53kΩ.

5. Calculate C_1 by setting compensator zero F_Z at 75% of the LC double pole.

$$C_1 = \frac{1}{2 \times \pi \times R_3 \times F_z}$$
$$= \frac{1}{2 \times \pi \times 4.51k\Omega \times 0.75 \times 3.5kHz}$$
$$= 13.3nF$$

Choose C_1=12nF.

6. Calculate C_2 by setting compensator pole F_p at half the swithing frequency.

$$C_2 = \frac{1}{p \times R_3 \times F_s}$$
$$= \frac{1}{p \times 3.74k\Omega \times 300kHz}$$
$$= 235pF$$

Choose C_2=220pF.

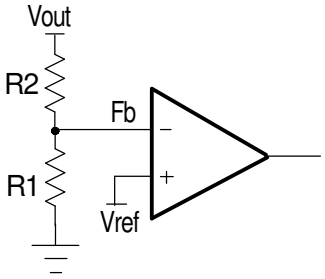
Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the Fb pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between V_{OUT} , V_{REF} and voltage divider.

$$R_1 = \frac{R_2 \times V_{REF}}{V_{OUT} - V_{REF}} \quad ...(18)$$

where R_2 is part of the compensator, and the value of R_1 value can be set by voltage divider.

Choose R_2=10kΩ, to set the output voltage at 1.6V, the result of R_1 is 10kΩ.



Voltage divider

Figure 13 - Voltage divider

In general, the minimum output load impedance including the resistor divider should be less than 5kΩ to prevent overcharge the output voltage by leakage current (e.g. Error Amplifier feedback pin bias current). A minimum load for 5kΩ less (<1/16w for most of application) is recommended to put at the output. For example, in this application,

Vout=1.6V

The power loss is 1/16W less

$R_{LOAD} = 1.6V \times 1.6V / (1/16W) = 40\Omega$

Select minimum load, 1kΩ should be good enough.

Input Capacitor Selection

Input capacitors are usually a mix of high frequency ceramic capacitors and bulk capacitors. Ceramic capacitors bypass the high frequency noise, and bulk capacitors supply current to the MOSFETs. Usually 1uF ceramic capacitor is chosen to decouple the high frequency noise. The bulk input capacitors are decided by voltage rating and RMS current rating. The RMS current in the input capacitors can be calculated as:

$$I_{RMS} = I_{OUT} \times \sqrt{D} \times \sqrt{1 - D}$$
$$D = \frac{V_{OUT}}{V_{IN}} \quad ...(19)$$

V_{IN} = 5V, V_{OUT}=1.6V, I_{OUT}=6A, using equation (19), the result of input RMS current is 2.80A.

For higher efficiency, low ESR capacitors are recommended. One Sanyo TPD series POSCAP 6TPD220M 6V 220uF with 12mΩ is chosen as input bulk capacitor.

Power MOSFETs Selection

The NX2114 requires two N-Channel power MOSFETs. The selection of MOSFETs is based on maximum drain source voltage, gate source voltage, maximum current rating, MOSFET on resistance and power dissipation. The main consideration is the power loss contribution of MOSFETs to the overall converter efficiency. In this design example, two Fairchild FDS6294 are used. They have the following parameters: V_{DS}=30V, I_D=13A, R_{DSON}=14.4mΩ,Q_{GATE}=10nC.

There are three factors causing the MOSFET power loss: conduction loss, switching loss and gate driver loss.

Gate driver loss is the loss generated by discharging the gate capacitor and is dissipated in driver circuits. It is proportional to frequency and is defined as:

$$P_{gate} = (Q_{HGATE} \times V_{HGS} + Q_{LGATE} \times V_{LGS}) \times F_S \quad ...(20)$$

where Q_{HGATE} is the high side MOSFETs gate charge, Q_{LGATE} is the low side MOSFETs gate charge, V_{HGS} is the high side gate source voltage, and V_{LGS} is the low side gate source voltage.

According to equation (20), P_{GATE} =0.03W. This power dissipation should not exceed maximum power dissipation of the driver device.

Conduction loss is simply defined as:

$$P_{HCON} = I_{OUT}^2 \times D \times R_{DS(ON)} \times K$$
$$P_{LCON} = I_{OUT}^2 \times (1 - D) \times R_{DS(ON)} \times K$$
$$P_{TOTAL} = P_{HCON} + P_{LCON} \quad ...(21)$$

where the $R_{DS(ON)}$ will increases as MOSFET junction temperature increases, K is $R_{DS(ON)}$ temperature dependency. As a result, $R_{DS(ON)}$ should be selected for the worst case, in which K equals to 1.43 at 125°C according to FDS6294 datasheet. Using equation (21), the result of P_{TOTAL} is 0.75W. Conduction loss should not exceed package rating or overall system thermal budget.

Switching loss is mainly caused by crossover conduction at the switching transition. The total switching loss can be approximated.

$$P_{SW} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times T_{SW} \times F_S \quad ...(22)$$

where I_{OUT} is output current, T_{SW} is swithing time,and F_S is switching frequency. Swithing loss P_{SW} is frequency dependent.

Soft Start, Enable and shut Down

The NX2114 has a digital start up. It is based on digital counter with 1024 cycles. For NX2114 with 300kHz operation, the start up time is about 3.5ms. For NX2114A with 600kHz operation, the start up time is about half of NX2114, 1.75mS.

NX2114/NX2114A can be enabled or disabled by pulling COMP pin below 0.3V. The function is illustrated in the following diagram. During the normal operation, the lowest COMP voltage is clamped to be about 700mV , the COMP voltage is higher than 0.3V. If external switch with 10Ω R_{dson} or less to pull down COMP pin, when COMP is below 0.3V, the digital soft start will be reset to zero. All the drivers will be off. The synchronous buck is shut off. When external switch is released, and COMP is above 0.3V, a soft start will initiates and system starts from the beginning.

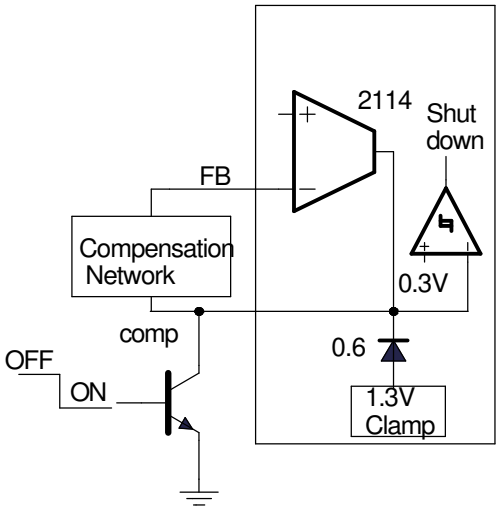


Figure 14 - Enable and Shut down NX2114 by pulling down COMP pin.

Feedback Under Voltage Shut Down

NX2114 relies on the Feedback Under Voltage Lock Out (FB UVLO) to provide short circuit protection. Basically, NX2114 has a comparator compare the feedback voltage with the FB UVLO threshold 0.4V.

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During the normal operation, if the output is short, the feedback voltage will be lower than 0.4V and comparator will change the state. After certain internal delay, both high side and low side driver will be turned off. The output will be latched. The normal operation should be achieved by removing the short and recycle the VCC.

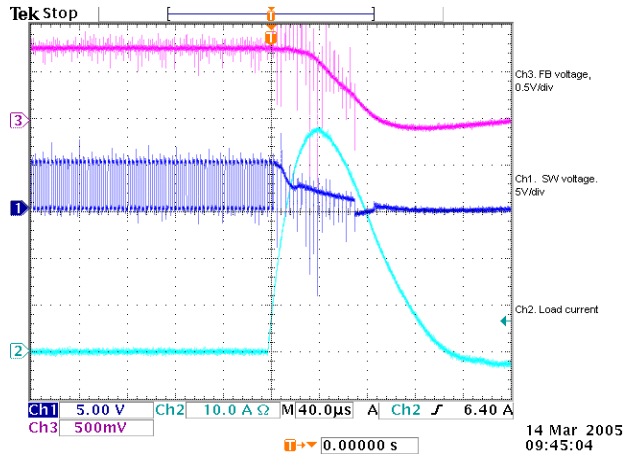

Figure 15 - Operation waveforms during short condition.

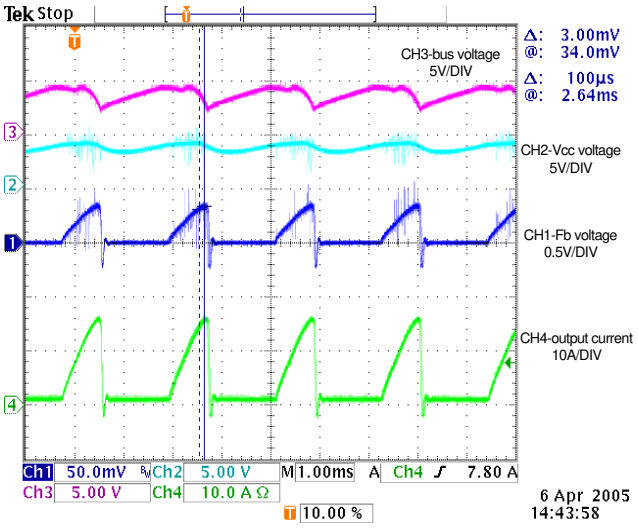

Figure 16 - Operation waveform with start up at short.

During the start up, the output voltage is discharged to zero by the synchronous FET. FB voltage starts increase from zero when digital start block operates. Before half of the start up time, the Feedback Under Voltage Lock Out comparator is disabled. After half of start up time, the Feedback UVLO comparator is enabled. The FB UVLO threshold is set to be half of voltage at the positive input of error amplifier. With this set up, if the output is short before soft start, the Feedback UVLO comparator can catch it and turn off the driver. The short circuit operation waveform during normal operation and during the soft start are shown as follows.

During the normal operation, Feedback UVLO will take the role. But during the soft start, due to the input voltage dropping, UVLO Vcc will take the role, hiccup happens.

The Feedback UVLO can provide short circuit protection under certain conditions. However, since feedback does not have accurate information of current, this protection only provides certain level of over current protection. MOSFET should design such that it can survive with high pulse current for a short period of time.

Layout Considerations

The layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results.

There are two sets of components considered in the layout which are power components and small signal components. Power components usually consist of input capacitors, high-side MOSFET, low-side MOSFET, inductor and output capacitors. A noisy environment is generated by the power components due to the switching power. Small signal components are connected to sensitive pins or nodes. A multilayer layout which includes power plane, ground plane and signal plane is recommended .

Layout guidelines:

1. First put all the power components in the top layer connected by wide, copper filled areas. The input capacitor, inductor, output capacitor and the MOSFETs should be close to each other as possible. This helps to reduce the EMI radiated by the power loop due to the high switching currents through them.

2. Low ESR capacitor which can handle input RMS ripple current and a high frequency decoupling ceramic

cap which usually is 1uF need to be practically touching the drain pin of the upper MOSFET, a plane connection is a must.

3. The output capacitors should be placed as close as to the load as possible and plane connection is required.

4. Drain of the low-side MOSFET and source of the high-side MOSFET need to be connected thru a plane ans as close as possible. A snubber nedds to be placed as close to this junction as possible.

5. Source of the lower MOSFET needs to be connected to the GND plane with multiple vias. One is not enough. This is very important. The same applies to the output capacitors and input capacitors.

6. Hdrv and Ldrv pins should be as close to MOSFET gate as possible. The gate traces should be wide and short. A place for gate drv resistors is needed to fine tune noise if needed.

7. Vcc capacitor, BST capacitor or any other bypassing capacitor needs to be placed first around the IC and as close as possible. The capacitor on comp to GND or comp back to FB needs to be place as close to the pin as well as resistor divider.

8. The output sense line which is sensing output back to the resistor divider should not go through high frequency signals.

9. All GNDs need to go directly thru via to GND plane.

10. The feedback part of the system should be kept away from the inductor and other noise sources, and be placed close to the IC.

11. In multilayer PCB, separate power ground and analog ground. These two grounds must be connected together on the PC board layout at a single point. The goal is to localize the high current path to a separate loop that does not interfere with the more sensitive analog control function.

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TYPICAL APPLICATION

Single Supply 5V Input

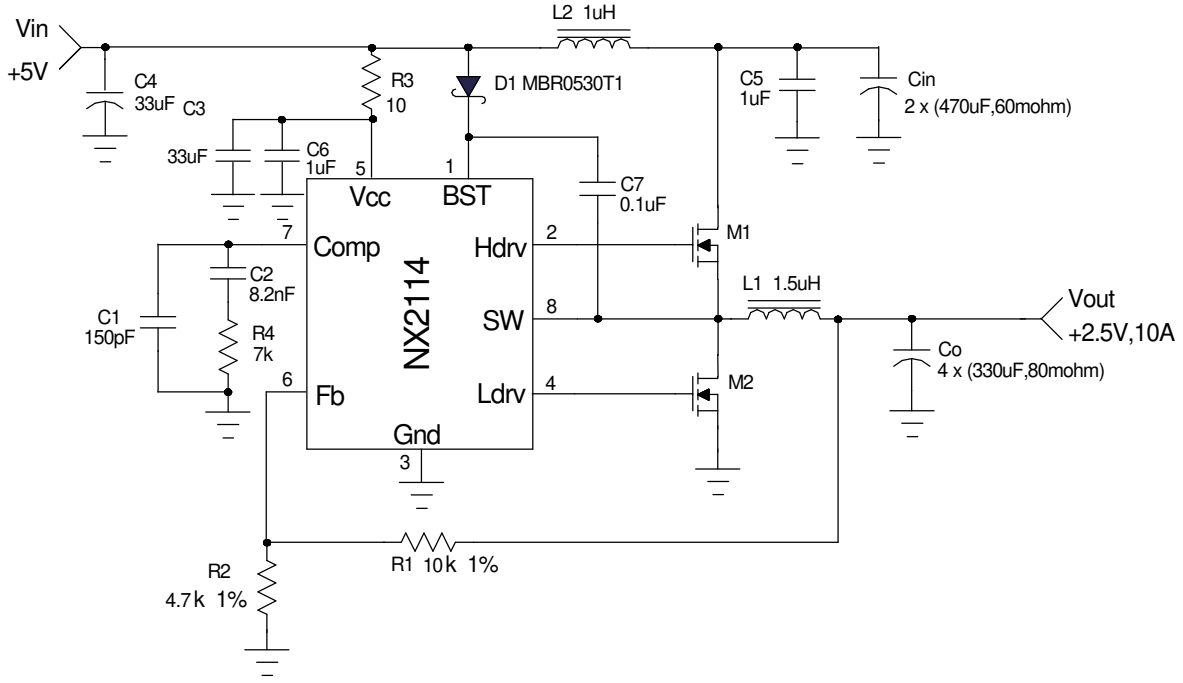

Figure 17 - Application of NX2114 for 5V input and 2.5V output with electrolytic capacitors

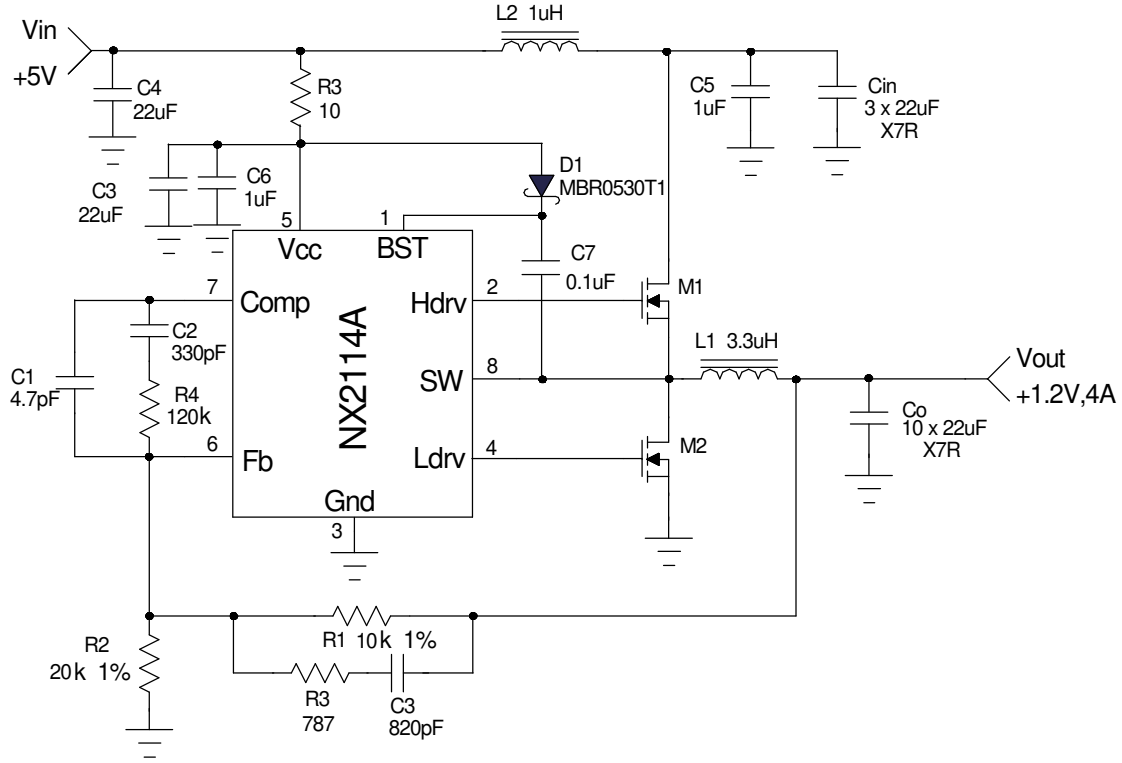

Figure 18 - Application of NX2114A for 5V input and 1.2V output with ceramic output capacitors

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TYPICAL APPLICATIONS(CONT')

Dual power supply (+5V BIAS,+12V BUS)

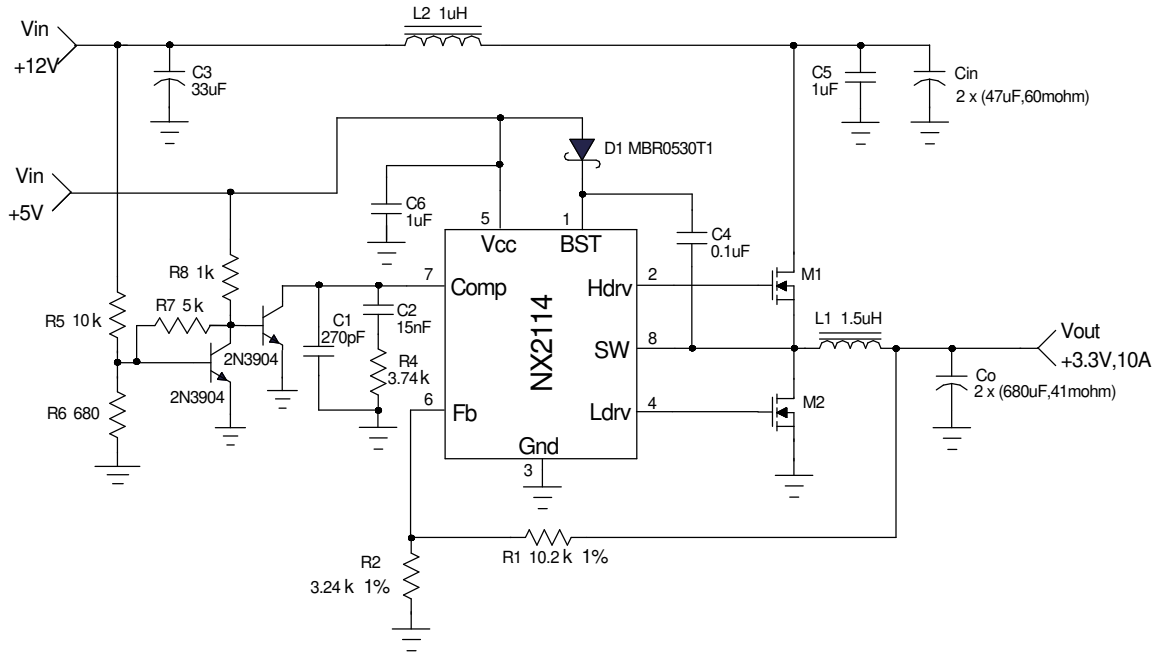

Figure 19 -Application of NX2114 for 5V bias and 12V input bus

Single power supply (+11V to +24V BUS)

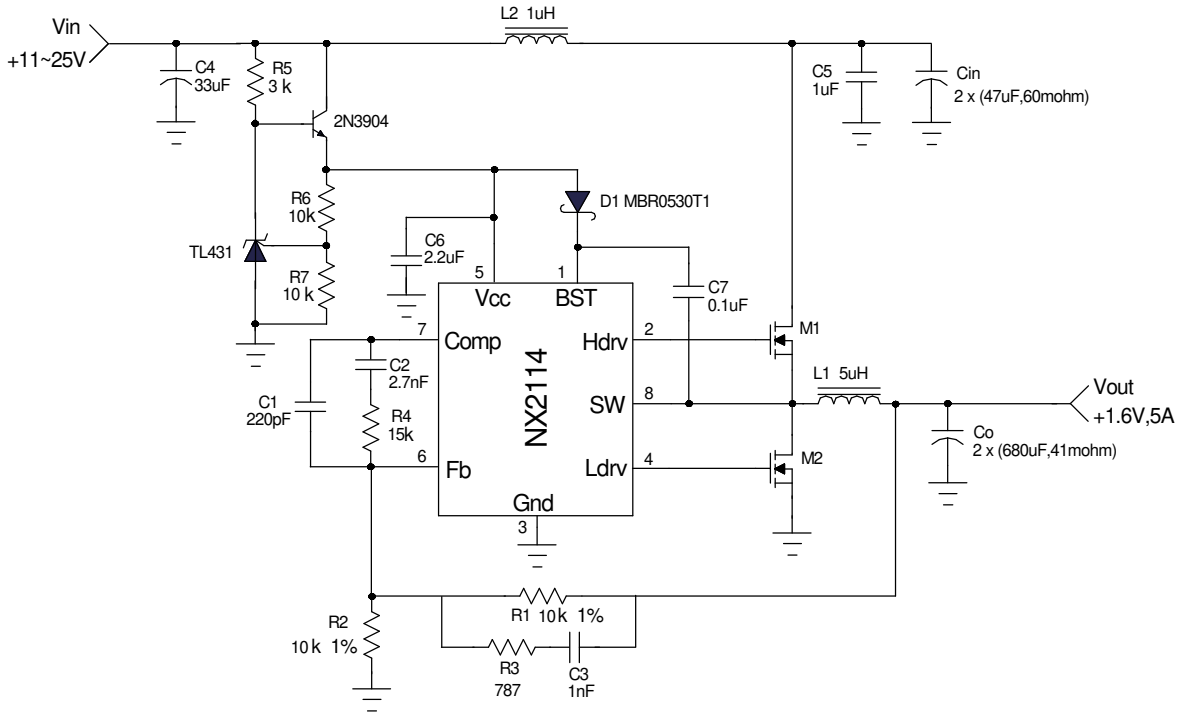

Figure 20 -Application of NX2114 for high input bus application

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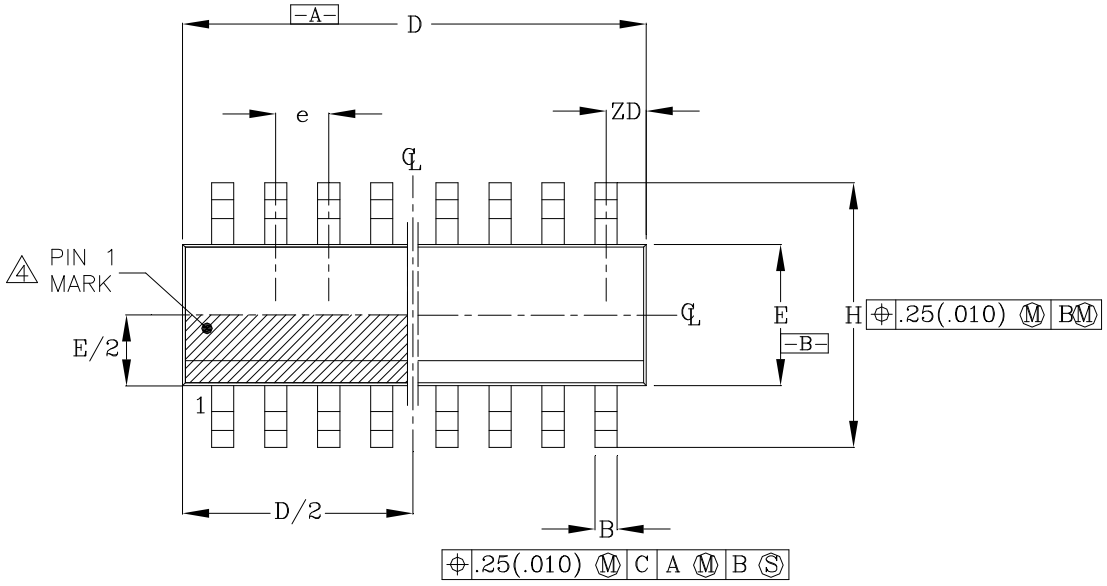
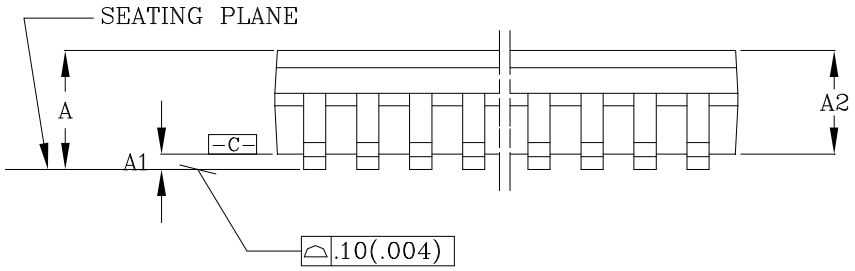
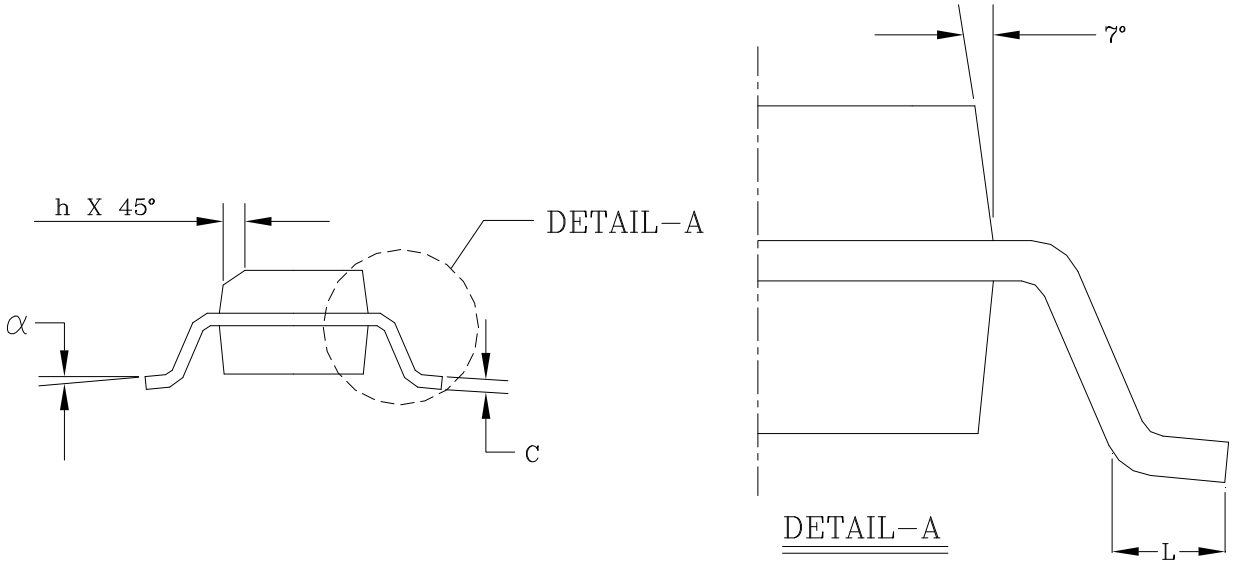
SOIC8 PACKAGE OUTLINE DIMENSIONS







SYMBOL	SOIC-8LD MILLIMETERS	
	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
α	0°	8°
ZD	0.53 REF	
A2	1.37	1.57

SYMBOL	SOIC-8LD INCHES	
	MIN	MAX
A1	.0040	.0098
B	.014	.018
C	.0075	.0098
D	.189	.196
E	.150	.157
e	.050 BSC	
H	.2284	.2440
h	.0099	.0196
L	.016	.050
A	.060	.068
α	0°	8°
ZD	.021 REF	
A2	.054	.062

NOTES :

1. LEAD COPLANARITY SHOULD BE 0 TO 0.10MM (.004") MAX.
2. PACKAGE SURFACE FINISHING :
   (2.1) TOP : MATTE (CHARMILLES #18~30).
   (2.2) ALL SIDES : MATTE (CHARMILLES #18~30).
   (2.3) BOTTOM : SMOOTH OR MATTE (CHARMILLES #18~30).
3. ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM (.010") PER SIDE(D).

⚠4 DETAIL OF PIN #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

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