DLP4501 .45 WXGA S311 DMD

1 Features

- 0.45-Inch (11.43-mm) Diagonal Micromirror Array
  - 912 × 1140 Array of Aluminum Micrometer-Sized Mirrors, in a diamond layout for an effective display resolution of 1280 × 800 (WXGA)
  - 7.6 Micron Micromirror Pitch
  - ±12° Micromirror Tilt (Relative to Flat Surface)
  - Side Illumination for Optimal Efficiency and Optical Engine Size
  - Polarization Independent Aluminum Micromirror Surface
- 21.3-mm × 11-mm × 3.33-mm Package Size
- Dedicated DLP6401 Display Controller for Reliable Operation

2 Applications

- Battery Powered Mobile Accessory HD Projector
- Battery Powered Smart HD Accessory
- Screenless Display – Interactive Display
- Gaming Display
- Mobile Cinema

3 Description

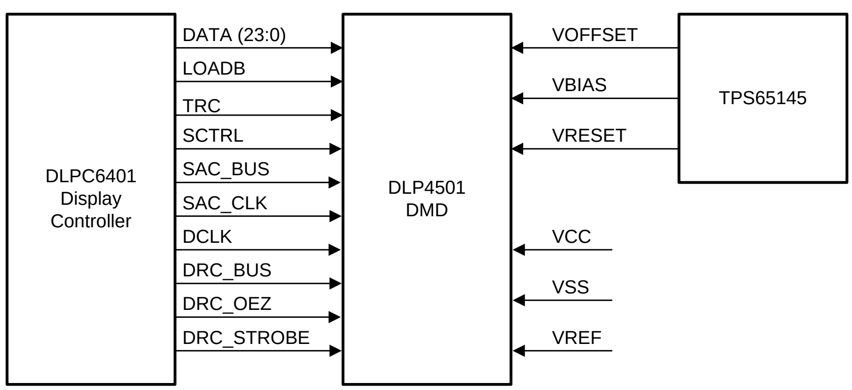
The DLP4501 digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MOEMS) spatial light modulator (SLM). When coupled to an appropriate optical system, the DLP4501 DMD displays a very crisp and high quality image or video. DLP4501 is part of the chipset comprising of the DLP4501 DMD and DLPC6401 display controller. The compact physical size of the DLP4501 is well-suited for portable equipment where a small form factor is important.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP4501	CLGA (80)	21.3 mm × 11 mm × 3.33 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DLP® DLP4501 (.45 WXGA S311) Chipset



System signal routing omitted for clarity

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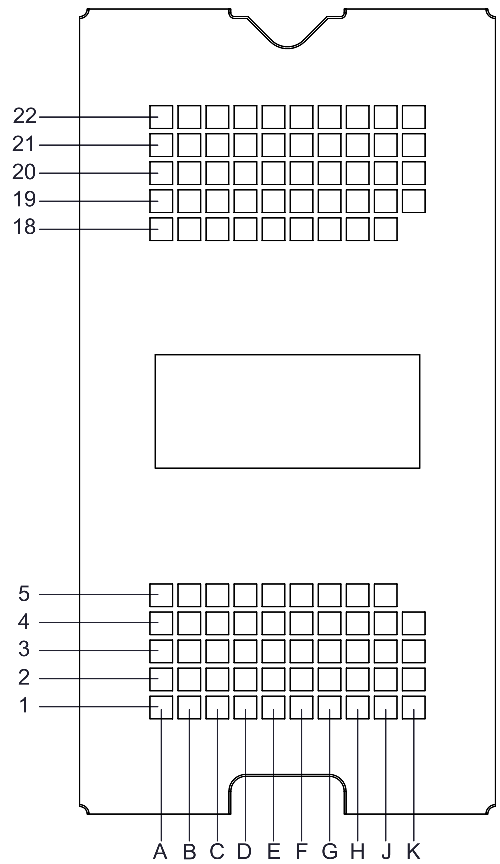
4 Revision History

DATE	REVISION	NOTES
November 2018	*	Initial release.

5 Pin Configuration and Functions

FQG Package
80-Pin CLGA
Bottom View



Pin Functions – Connector Pins

PIN		TYPE	SIGNAL	CLOCKED BY	DATA RATE	DESCRIPTION
NAME	NO.					
DATA INPUTS						
DATA(0)	A1	I	LVCMOS	DCLK	DDR	Input data bus
DATA(1)	A2	I	LVCMOS	DCLK	DDR	
DATA(2)	A3	I	LVCMOS	DCLK	DDR	
DATA(3)	A4	I	LVCMOS	DCLK	DDR	
DATA(4)	B1	I	LVCMOS	DCLK	DDR	
DATA(5)	B3	I	LVCMOS	DCLK	DDR	
DATA(6)	C1	I	LVCMOS	DCLK	DDR	
DATA(7)	C3	I	LVCMOS	DCLK	DDR	
DATA(8)	C4	I	LVCMOS	DCLK	DDR	
DATA(9)	D1	I	LVCMOS	DCLK	DDR	
DATA(10)	D4	I	LVCMOS	DCLK	DDR	
DATA(11)	E1	I	LVCMOS	DCLK	DDR	
DATA(12)	E4	I	LVCMOS	DCLK	DDR	
DATA(13)	F1	I	LVCMOS	DCLK	DDR	
DATA(14)	F3	I	LVCMOS	DCLK	DDR	
DATA(15)	G1	I	LVCMOS	DCLK	DDR	
DATA(16)	G2	I	LVCMOS	DCLK	DDR	
DATA(17)	G4	I	LVCMOS	DCLK	DDR	
DATA(18)	H1	I	LVCMOS	DCLK	DDR	
DATA(19)	H2	I	LVCMOS	DCLK	DDR	
DATA(20)	H4	I	LVCMOS	DCLK	DDR	
DATA(21)	J1	I	LVCMOS	DCLK	DDR	
DATA(22)	J3	I	LVCMOS	DCLK	DDR	
DATA(23)	J4	I	LVCMOS	DCLK	DDR	
DCLK	K1	I	LVCMOS	—	—	Input data bus clock
CONTROL INPUTS						
LOADB	K2	I	LVCMOS	DCLK	DDR	Parallel data load enable
TRC	K4	I	LVCMOS	DCLK	DDR	Input data toggle rate control
SCTRL	K3	I	LVCMOS	DCLK	DDR	Serial control bus
SAC_BUS	C20	I	LVCMOS	SAC_CLK	—	Stepped address control serial data
SAC_CLK	C22	I	LVCMOS	—	—	Stepped address control serial clock
MIRROR RESET CONTROL INPUTS						
DRC_BUS	B21	I	LVCMOS	SAC_CLK		DMD reset-control serial bus
DRC_OEZ	A20	I	LVCMOS	—	—	Active-low output enable signal for internal DMD Reset driver circuitry
DRC_STROBE	A22	I	LVCMOS	SAC_CLK		Strobe signal for DMD reset control inputs
POWER						
VBIAS (1)	C19, D19	Power	Analog			Mirror Reset Bias Voltage
VOFFSET (1)	A19, K19	Power	Analog			Mirror Reset Offset Voltage
VRESET (1)	E19, F19	Power	Analog			Mirror reset voltage
VREF (1)	B19, J19	Power	Analog			Power supply for low voltage CMOS double-data-rate (DDR) interface

(1) The following power supplies are all required to operate the DMD: VSS, VCC, VREF, VOFFSET, VBIAS, VRESET.

Pin Functions – Connector Pins (continued)

PIN		TYPE	SIGNAL	CLOCKED BY	DATA RATE	DESCRIPTION
NAME	NO.					
VCC [(1)]	B22, C2, D21, E2, E20, E22, F21, G3, G19, G20, G22, H19, H21, J20, J22, K21	Power	Analog			Power Supply for LVCMOS Logic
VSS [(1)]	A21, B2, B4, B20, C21, D2, D3, D20, D22, E3, E21, F2, F4, F20, F22, G21, H3, H20, H22, J2, J21, K20	GND	Analog			Ground. Common return for all power inputs

Pin Functions – Test Pads

NUMBER	SYSTEM BOARD	NUMBER	SYSTEM BOARD
A5	Do not connect	F5	Do not connect
A18	Do not connect	F18	Do not connect
B5	Do not connect	G5	Do not connect
B18	Do not connect	G18	Do not connect
C5	Do not connect	H5	Do not connect
C18	Do not connect	H18	Do not connect
D5	Do not connect	J5	Do not connect
D18	Do not connect	J18	Do not connect
E5	Do not connect		
E18	Do not connect		

6 Specifications

6.1 Absolute Maximum Ratings

see [1]

			MIN	MAX	UNIT
Supply voltage	VCC	Supply voltage for LVCMOS logic [2]	–0.5	4	V
	VREF	Supply voltage for LVCMOS logic [2]	–0.5	4	V
	VOFFSET	Supply voltage for HVCMOS and micromirror electrode [2]	–0.5	8.75	V
	VBIAS	Supply voltage for micromirror electrode [2]	–0.5	17	V
	VRESET	Supply voltage for micromirror electrode [2]	–11	0.5	V
	| VBIAS–VOFFSET |	Supply voltage delta [3]		8.75	V
Input voltage		Input voltage for other inputs [2]	–0.5	VREF + 0.5	V
Clock frequency	f_{DLCK}	DCLK clock frequency [4]	80	120	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational [5]	–20	90	°C
		Temperature – non-operational [5]	–40	90	°C
	T_{DP}	Dew Point - operating and non-operating		81	°C
	$\|T_{DELTA}\|$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1 [6]		30	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure above or below the *Recommended Operating Conditions* for extended periods may affect device reliability.
(2) All voltage values are with respect to ground terminals (VSS). The following power supplies are all required to operate the DMD: VSS, VCC, VREF, VOFFSET, VBIAS and VRESET.
(3) To prevent excess current, the supply voltage delta |VBIAS - VOFFSET| must be less than specified limit.
(4) BSA to Reset Timing specifications are synchronous and guaranteed for DCLK between specified limits.
(5) The highest temperature of the active array (as calculated by the *Micromirror Array Temperature Calculation*), or of any point along the Window Edge as defined in Figure 8. The location of the thermal test point TP2 in Figure 8 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(6) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 8. The window test point TP2 shown in Figure 8 is intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable before the DMD is installed in the final product.

		MIN	NOM	MAX	UNIT
T_{stg}	DMD storage temperature	-40		85	°C
T_{DP}	Storage dew point - long-term average [1] [2]		18	24	°C
	Storage dew point - short-term [3]			28	°C

(1) Long-term is defined as the usable life of the device.
(2) Contact a TI representative for further information regarding nominal versus maximum values.
(3) Dew points beyond the specified long-term dew point are for short-term conditions only, where short-term is defined as less than 60 cumulative days over the usable life of the device (operating, non-operating, or storage).

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE (2)					
VREF	Supply voltage for LVCMOS interface (3)	1.6	1.8	2.0	V
VCC	Supply voltage for LVCMOS logic (3)	2.375	2.5	2.625	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode (3)	8.25	8.5	8.75	V
VBIAS	Supply voltage for micromirror electrode (3)	15.5	16	16.5	V
VRESET	Supply voltage for micromirror electrode (3)	–9.5	–10	–10.5	V
|VBIAS–VOFFSET|	Supply voltage delta (absolute value)			8.75	V
Vp	Positive-going threshold voltage	0.4×VREF		0.7×VREF	V
Vn	Negative-going threshold voltage	0.3×VREF		0.6×VREF	V
Vh	Hysteresis voltage (Vp - Vn)	0.1×VREF		0.4×VREF	V
$V_{ih(DC)}$	DC High level input voltage	0.7×VREF		VREF+0.5	V
$V_{il(DC)}$	DC Low level input voltage	–0.3		0.3×VREF	V
$V_{ih(AC)}$	AC High level input voltage	0.8×VREF		VREF+0.5	V
$V_{il(AC)}$	AC Low level input voltage	–0.3		0.2×VREF	V

(1) The functional performance of the device specified in this datasheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
(2) All voltage values are with respect to the ground pins (VSS).
(3) The following power supplies are all required to operate the DMD: VCC, VREF, VOFFSET, VBIAS and VRESET.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array Temperature – long-term operational (4) (5) (6) (7)	0		40 to 70 (6)	°C
	Array Temperature – short-term operational (5) (8)	–20		75	°C
T_{WINDOW}	Window temperature – operational (4) (9)			90	°C
$\|T_{DELTA}\|$	Absolute Temperature difference between any point on the window edge and the ceramic test point TP1 (10)			30	°C
T_{DP}	Dew Point – long - term average (operational and non-operational) (7) (11)		18	24	°C
	Dew Point – short - term (operational and non-operational) (12)			28	°C
ILL_{UV}	Illumination wavelengths < 395 nm (4)		0.68	2.00	mW/cm²
ILL_{VIS}	Illumination wavelengths between 395 nm and 800 nm			Thermally limited	
ILL_{IR}	Illumination wavelengths >800 nm			10	mW/cm²

(4) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(5) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 8 and the **Package Thermal Resistance** using *Micromirror Array Temperature Calculation*
(6) Per Figure 1 the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experience in the end application. Refer to **Micromirror Landed-On/Landed-OFF Duty Cycle** for a definition of micromirror landed duty cycle.
(7) Long-term is defined as the usable life of the device
(8) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(9) Window temperature is the highest temperature on the window edge shown in Figure 8. The location of the thermal test point TP2 in Figure 8 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(10) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in Figure 8 . The window test point TP2 shown in Figure 8 is intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used
(11) Contact a TI representative for further information regarding nominal versus maximum values.
(12) Dew points beyond the specified long-term dew point are for short-term conditions only, where short-term is defined as less than 60 cumulative days over the usable life of the device (operating, non-operating, or storage).

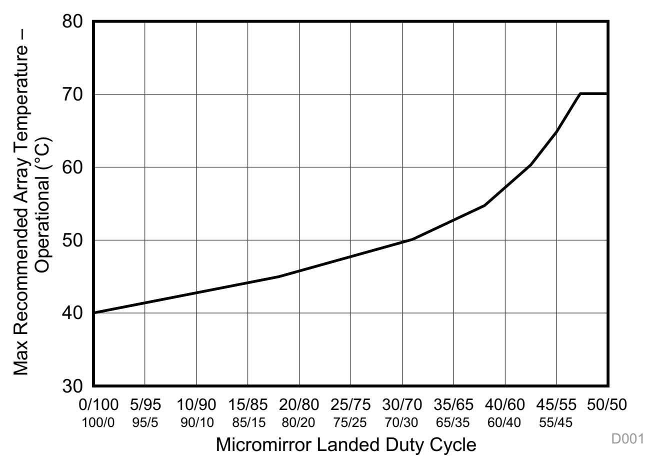


Figure 1. Maximum Recommended Array Temperature Derating Curve

6.5 Thermal Information

THERMAL METRIC (1)		DLP4501 FQG Package			UNIT
		MIN	TYP	MAX	
Thermal resistance	Active area to test point 1 (TP1)			2.00	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the **Recommended Operating Conditions** . The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	VCC= 2.50 V I_{OH}= -21 mA	1.70			V
V_{OL}	High-level output voltage	VCC= 2.50 V I_{OH}= 15 mA			0.40	V
I_{IL}	Low -level input current (3)	VREF= 2.00 V V_I= 0.00 V	-50			nA
I_{IH}	High -level input current (3)	VREF= 2.00 V V_I= V_{REF}			50	nA
SUPPLY CURRENT						
I_{REF}	Supply current: V_{VREF}	VREF = 2.00 V f_{DCLK}= 120 MHz			2.75	mA
I_{REF}	Supply current: V_{VREF}	VREF = 1.80 V f_{DCLK}= 120 MHz		2.15		mA
I_{CC}	Supply current: V_{VCC}	VCC = 2.75 V f_{DCLK}= 120 MHz			160	mA
I_{CC}	Supply current: V_{VCC}	VCC = 2.5 V f_{DCLK}= 120 MHz		125		mA
I_{OFFSET}	Supply current: $V_{VOFFSET}$ (4) (5)	VOFFSET = 8.75 V			3.3	mA
I_{OFFSET}	Supply current: $V_{VOFFSET}$ (4) (5)	VOFFSET = 8.5 V		3		mA
I_{BIAS}	Supply current: V_{BIAS} (4) (6) (5)	VBIAS = 16.5 V			3.55	mA
I_{BIAS}	Supply current: V_{VBIAS} (4) (6) (5)	VBIAS = 16.0 V		2.55		mA
I_{RESET}	Supply current: V_{RESET} (5)	VRESET = –10.5 V			3.1	mA
I_{RESET}	Supply current: V_{RESET} (5)	VRESET = –10.0 V		2.45		mA

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (VSS).
(3) Applies to LVCMOS pins only. LVCMOS pins do not have pull-up or pull-down configurations.
(4) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit.
(5) Supply power dissipation based on 3 global resets in 200 µs.
(6) When DRC_OEZ = High, the internal Reset Drivers are Tri-Stated and I_{BIAS} standby current is 6.5mA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
POWER (7)						
P_{REF}	Supply power dissipation: V_{VREF}	VREF = 2.00 V			5.5	mW
P_{REF}	Supply power dissipation: V_{VREF}	VREF = 1.80 V		3.87		mW
P_{CC}	Supply power dissipation: V_{VCC}	VCC= 2.75 V			440	mW
P_{CC}	Supply power dissipation: V_{VCC}	VCC= 2.5 V		312.5		mW
P_{OFFSET}	Supply power dissipation: $V_{VOFFSET}$	VOFFSET = 8.75 V			28.9	mW
P_{OFFSET}	Supply power dissipation: $V_{VOFFSET}$	VOFFSET= 8.5 V		25.5		mW
P_{BIAS}	Supply power dissipation: V_{VBIAS} (5)	VBIAS = 16.5 V			58.6	mW
P_{BIAS}	Supply power dissipation: V_{VBIAS} (5)	VBIAS = 16.0 V		40.8		mW
P_{RESET}	Supply power dissipation: V_{VRESET} (5)	VRESET = –10.5 V			32.6	mW
P_{RESET}	Supply power dissipation: V_{VRESET} (5)	VRESET = –10.0 V		24.5		mW
CAPACITANCE						
C_{IN}	Input capacitance	f = 1 MHz			10	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF

(7) The following power supplies are all required to operate the DMD: VSS, VCC, VREF, VOFFSET, VBIAS, VRESET.

6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
t_{su}	Setup time	DATA before DCLK↑ or DCLK↓ [1] [2]	30.7			ns
t_h	Hold time	DATA after DCLK↑ or DCLK↓ [2]	0.7			ns
t_{su}	Setup time	SCTRL before DCLK↑ or DCLK↓ [1] [2]	0.7			ns
t_h	Hold time	SCTRL after DCLK↑ or DCLK↓ [2]	0.7			ns
t_{su}	Setup time	TRC before DCLK↑ or DCLK↓ [1] [2]	0.7			ns
t_h	Hold time	TRC after DCLK↑ or DCLK↓ [2]	0.7			ns
t_{su}	Setup time	LOADB low before DCLK↑ [1] [2]	0.7			ns
t_h	Hold time	LOADB low after DCLK↓ [2]	0.7			ns
t_{su}	Setup time	SAC_BUS before SAC_CLK↑ [1] [2]	1.0			ns
t_{h4}	Hold time	SAC_BUS after SAC_CLK↑ [2]	1.0			ns
t_{su}	Setup time	DRC_BUS before SAC_CLK↑ [1] [2]	1.0			ns
t_h	Hold time	DRC_BUS after SAC_CLK↑ [2]	1.0			ns
t_{su}	Setup time	DRC_STROBE high before DCLK↑ [1] [2]	1.0			ns
t_h	Hold time	DRC_STROBE high after DCLK↑ [2]	1.0			ns
t_c	Cycle time	DCLK	8.33	10.0	12.5	ns
t_c	Cycle time	SAC_CLK	12.5	13.33	14.3	ns
t_w	Pulse duration	50% to 50% reference points: DCLK high or low	3.33			ns
t_w	Pulse duration	50% to 50% reference points: SAC_CLK high or low	5.0			ns
$t_{w(L)}$	Pulse duration	50% to 50% reference points: LOADB low	4.73			ns
$t_{w(H)}$	Pulse duration	50% to 50% reference points: DRC_STROBE high	7.0			ns
t_R	Rise time	20% to 80% reference points [3] [4]			1.08	ns
t_F	Fall time	80% to 20% reference points [3] [4]			1.08	ns
	Slew rate	Fast input [5]	1.0			V/ns
	Slew rate	Slow input [5]	0.5		1.0	V/ns

(1) ↑ = transition from low to high level. ↓ = transition from high to low level.
(2) Assumes fast input slew rate > 1.0 V/ns. For slower slew rate (0.5 V/ns < slew rate > 1.0 V/ns) the setup and hold times we be longer. 150 picoseconds should be added on setup and hold for every 0.10 V/ns decrease in slew rate (from 1.0 V/ns). The numbers are assuming all the slew rates for all the inputs and the clock are the same.
(3) Rise time and Fall time specifications apply to terminals DCLK, DATA, SCTRL, TRC, LOADB, SAC_CLK.
(4) Assumes VREF = 1.8 V
(5) Fast/ slow slew rates affect setup and hold times. See [2] .

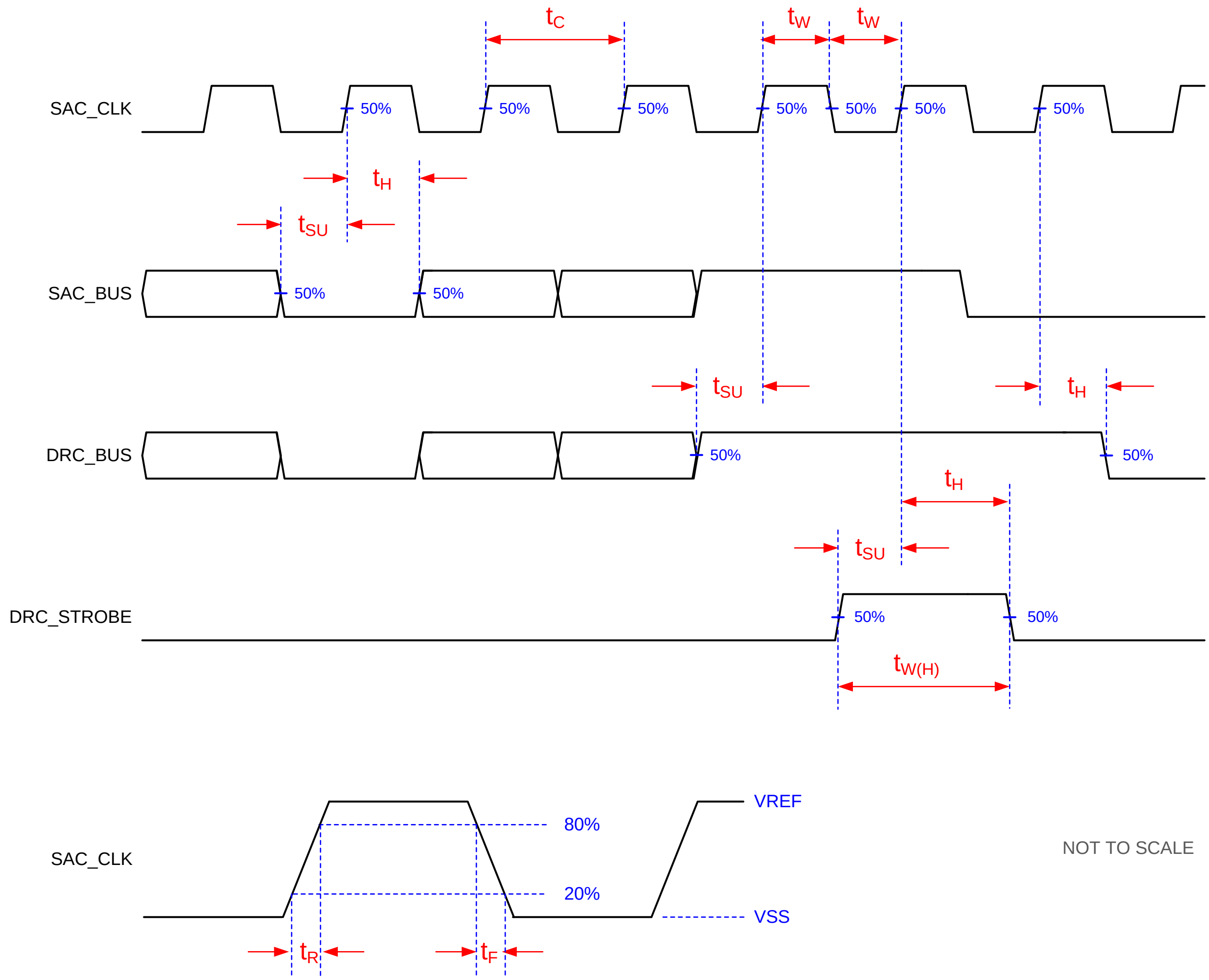


Figure 2. Timing Requirements 1

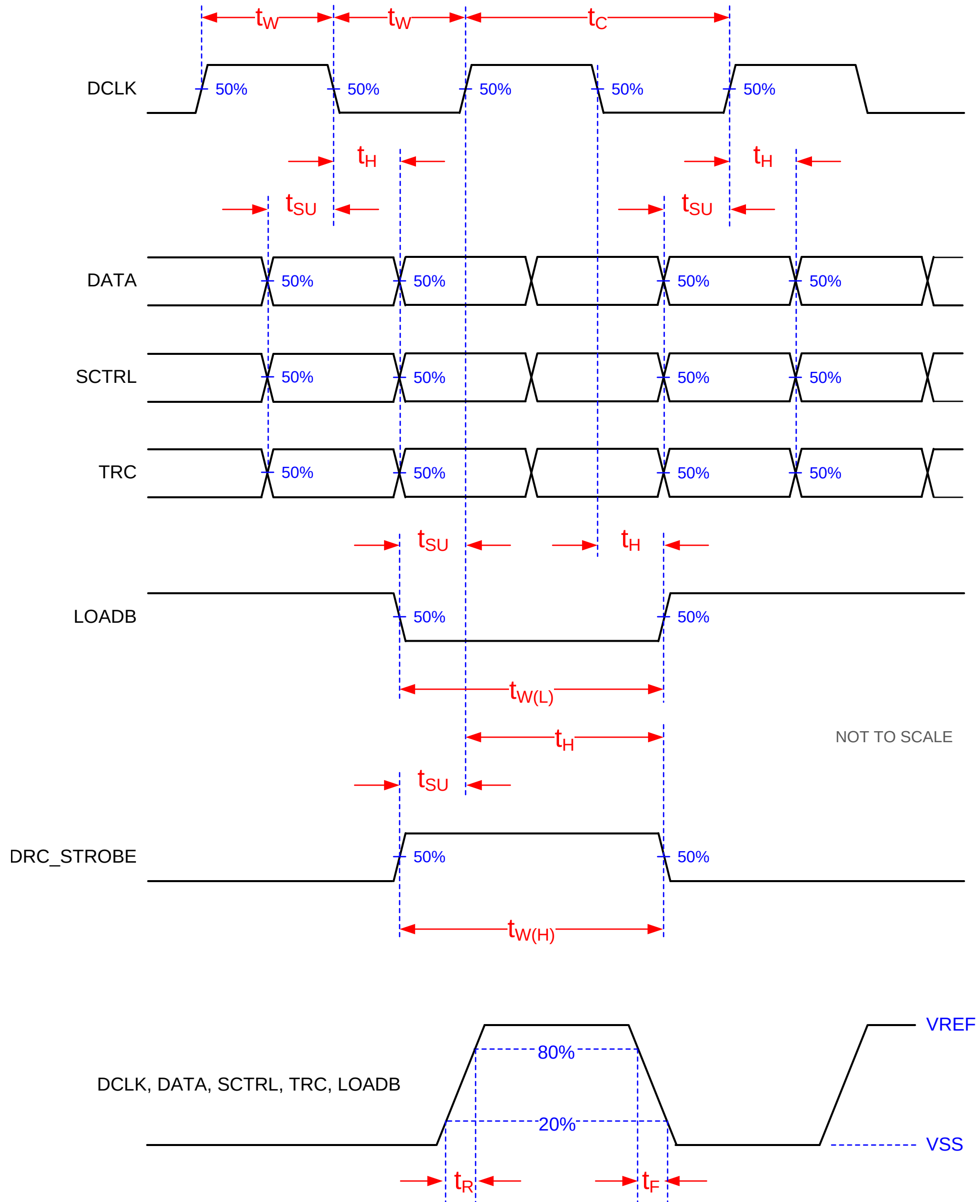
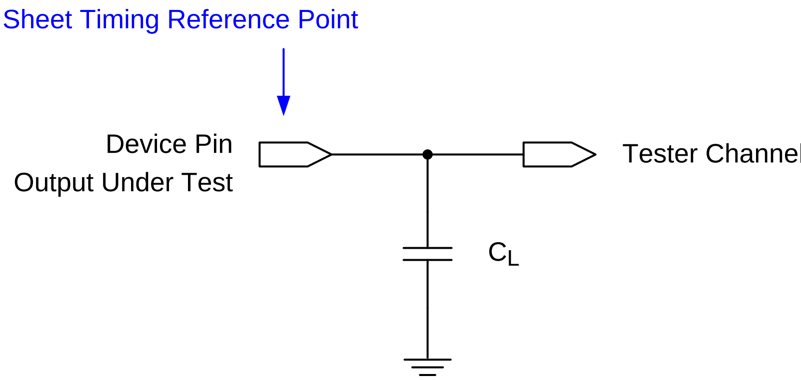


Figure 3. Timing Requirements 2



A. See *Timing* for more information.

Figure 4. Test Load Circuit for AC Timing Measurement

6.8 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:				
• Thermal Interface area (see Figure 5)			79	N
• Electrical Interface area uniformly distributed over each of the areas (Area #1 and Area #2) (see Figure 5)			55	N
• Wire Bond Cover Interface Area (see Figure 5)			60	N

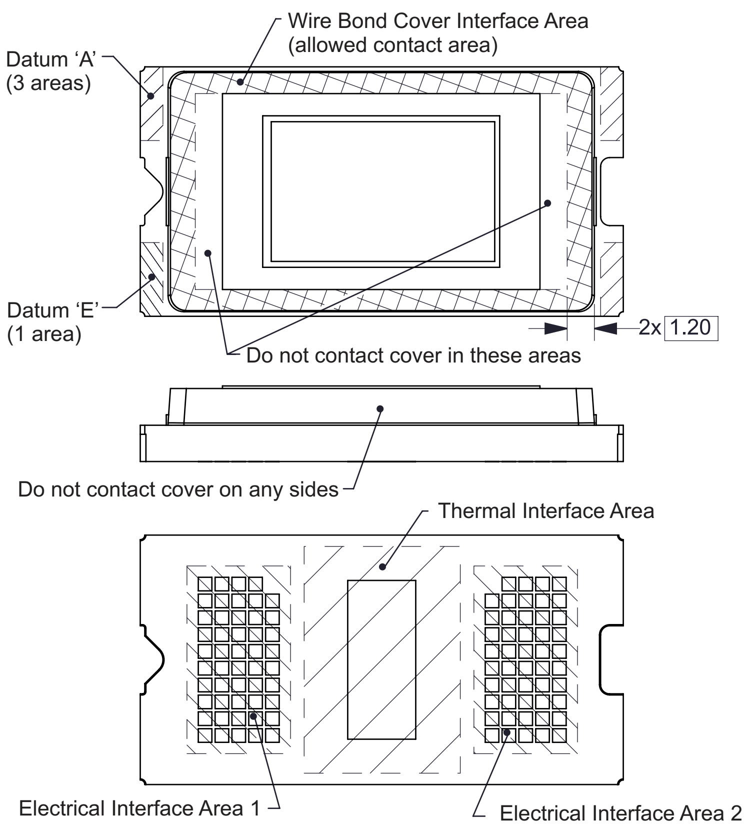


Figure 5. System Interface Loads

6.9 Micromirror Array Physical Characteristics

PARAMETER			VALUE	UNIT
	Number of active columns		(1) 1140	micromirrors
	Number of active rows	(1)	912	micromirrors
D	Micromirror (pixel) dimension	(1)	7.637	µm
P	Micromirror (pixel) pitch	(1)	10.8	µm
	Micromirror active array height	(1)	6.1614	mm
	Micromirror active array width	(1)	9.855	mm
	Micromirror active border	Pond of micromirror (POM)	10	micromirrors/side

(1) See Figure 6 and Figure 7 .

Pond of Micromirrors (POM) and other details omitted for clarity. Not to scale.

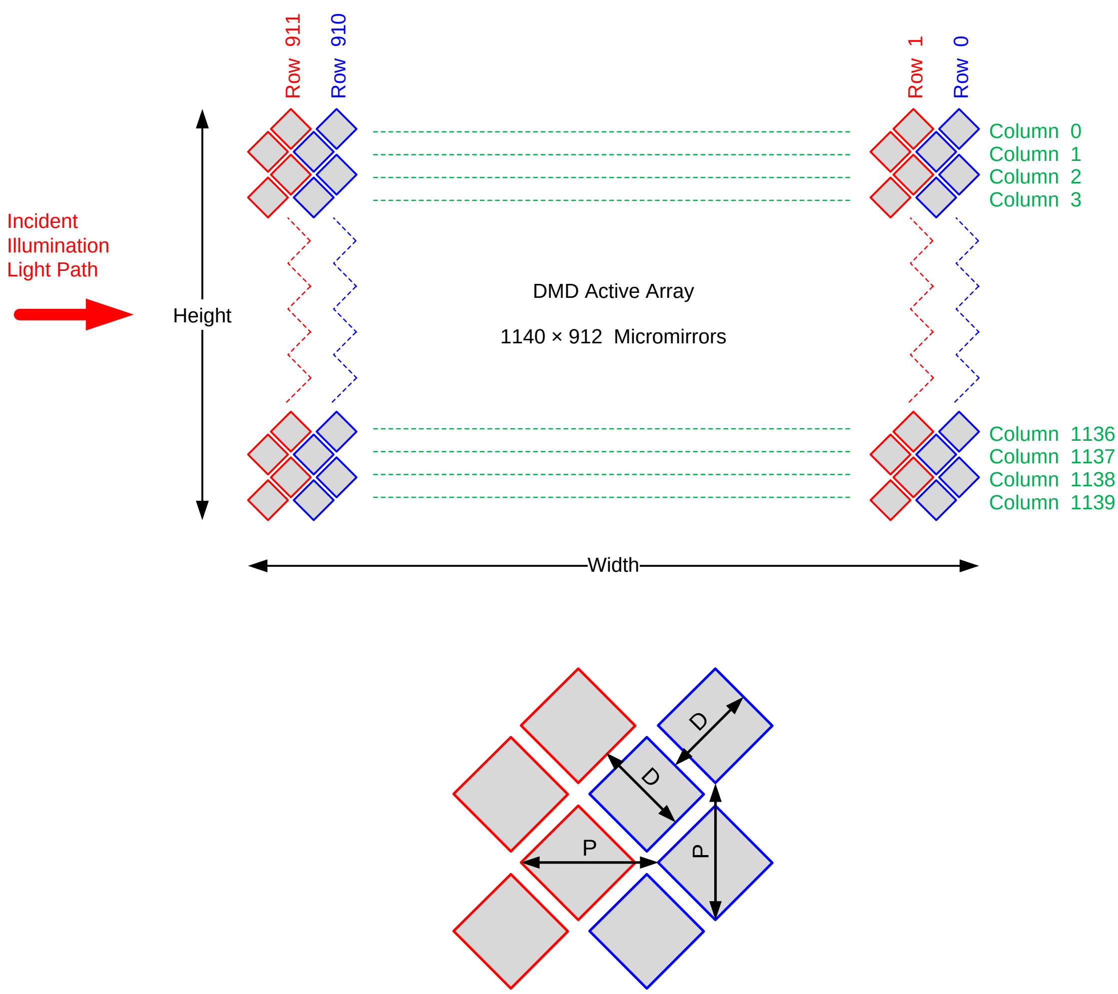


Figure 6. Micromirror Array Physical Characteristics

1. Refer to *Micromirror Array Physical Characteristics* for D and P specifications

6.10 Micromirror Array Optical Characteristics

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle (1)	DMD landed state	11	12	13	°
Orientation of the micromirror axis-of-rotation		89	90	91	°
Micromirror crossover time (2) (3)			5		μs
Micromirror switching time (2)			16		μs
Micromirror array optical efficiency (420nm - 680nm) (4)			66%		

(1) *Mirror Tilt*: Limits on variability of mirror tilt are critical in the design of the accompanying optical system. Variations in tilt angle within a device may result in apparent non-uniformities, such as line pairing and image mottling, across the projected image. Variations in the average tilt angle between devices may result in colorimetry, brightness, and system contrast variations. The specified limits represent the tolerances of the tilt angles within a device.
(2) Micromirror crossover time is primarily a function of the natural response time of the micromirrors.
(3) Performance as measured at the start of life.
(4) *DMD Efficiency* : Efficiency numbers assume 24-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. The efficiency is a photopically-weighted number corresponding to 12 degree tilt angle. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.

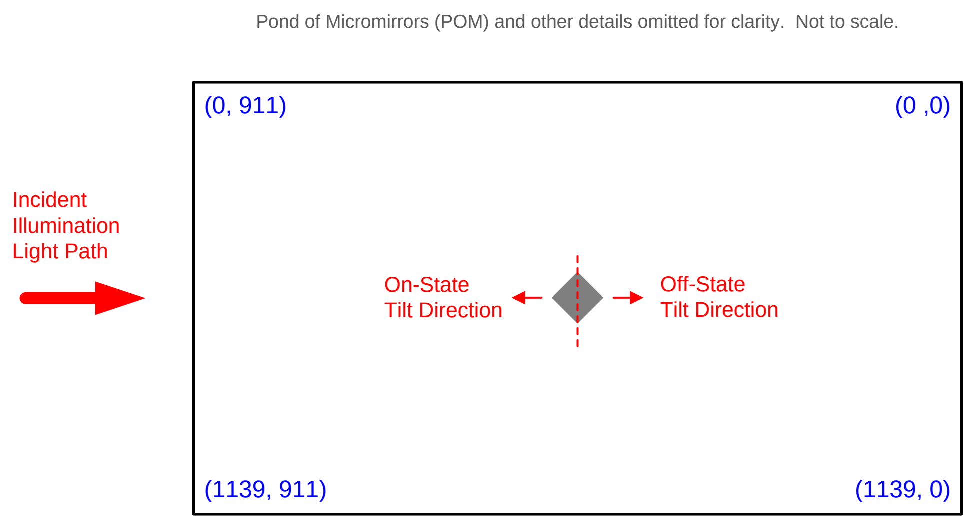


Figure 7. Array Coordinates and Micromirror Tilt Axis Orientation

6.11 Window Characteristics

PARAMETER (1)		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture (2)				See (2)	
Illumination overfill (3)				See (3)	
Window Transmittance, single-pass through both surfaces and glass (4)	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window Transmittance, single-pass through both surfaces and glass (4)	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

(1) See *Window Characteristics and Optics* for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the .45 WXGA device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.
(4) Single-pass through both surfaces and glass

6.12 Chipset Component Usage Specification

The DLP4501 DMD is a component of one or more DLP chipsets. Reliable function and operation of the DLP4501 DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

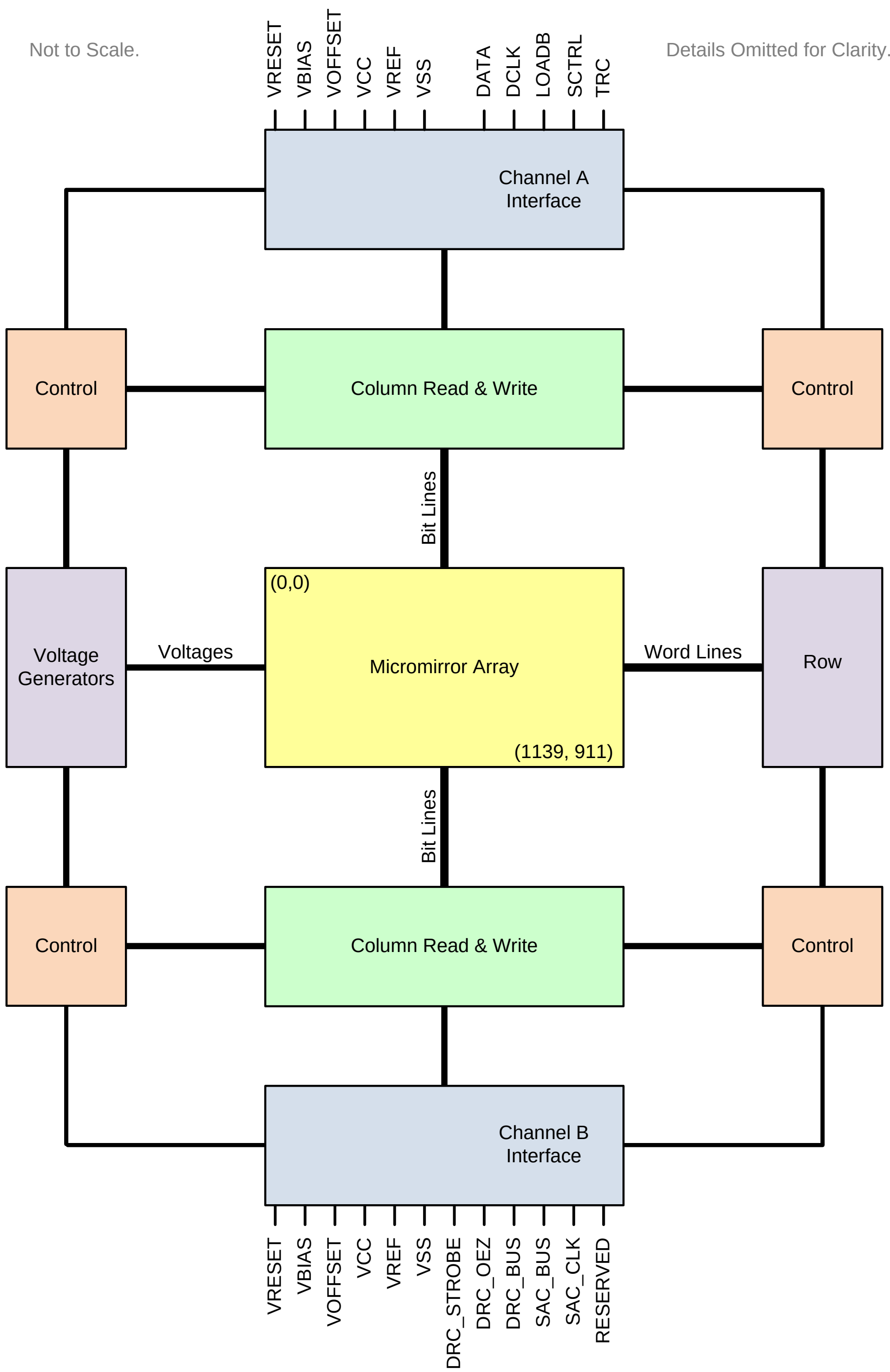
7 Detailed Description

7.1 Overview

The DLP4501 is a 0.45 inch diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1140 columns by 912 rows in a diagonal pixel arrangement.

DLP4501 is part of the chipset comprising of the DLP4501 DMD and DLPC6401 display controller. To ensure reliable operation, DLP4501 DMD must always be used with DLPC6401 display controller.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC6401 display controller. See the DLPC6401 display controller data sheet or contact a TI applications engineer.

7.5 Window Characteristics and Optics

NOTE

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections:

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the ON optical path from any other light path, including undesirable flat–state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

7.5.1.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

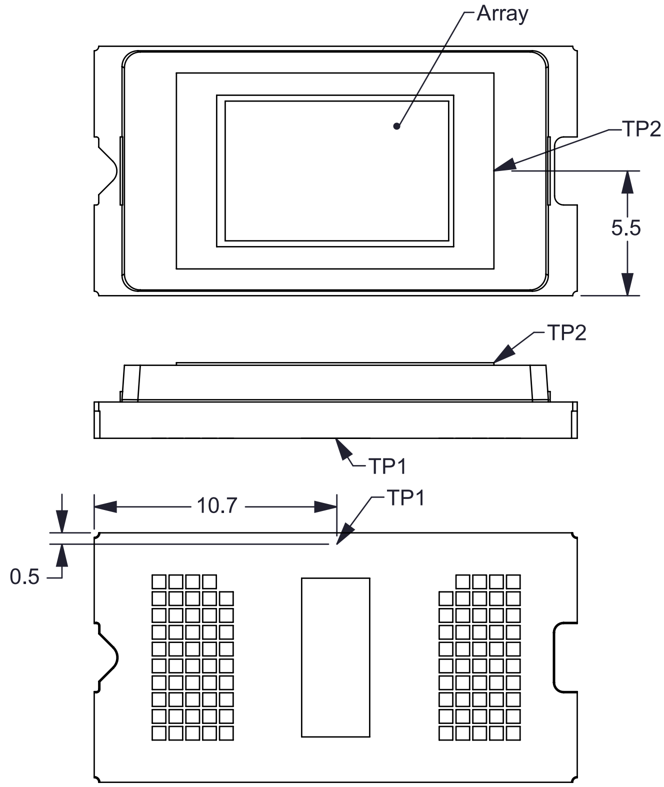


Figure 8. DMD Thermal Test Points

Active Array Temperature cannot be measured directly. Therefore it must be computed analytically from measurement points on the outside of the Series 311 package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature is provided by the following equations:

$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC})$

$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$

$Q_{ILLUMINATION} = (C_{L2W} \times SL)$

where

- T_{ARRAY} = Computed DMD array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in Figure 8
- $R_{ARRAY-TO-CERAMIC}$ = DMD package thermal resistance from array to outside ceramic (°C/W) specified in *Thermal Information*
- Q_{ARRAY} = Total DMD power; electrical, specified in *Electrical Characteristics* , plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W)
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

The Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. Refer to the specifications in *Electrical Characteristics* . A nominal electrical power dissipation to use when calculating array temperature is 0.25 Watts. The absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

Micromirror Array Temperature Calculation (continued)

The conversion constant CL2W is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00293 W/lm.

Sample Calculation for typical projection application:

$T_{CERAMIC}$ = 55°C, assumed system measurement; see *Recommended Operating Conditions* for specification limits

SL = 1000 lm

$Q_{ELECTRICAL}$ = 0.25 W

CL2W = 0.00293 W/lm

$Q_{ARRAY} = 0.025 + (0.00293 \times 1000) = 3.18$ W

T_{ARRAY} = 55°C + (3.18 W × 2.0 °C/W) = 61.4 °C

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the On state 75% of the time (and in the Off state 25% of the time), whereas 25/75 would indicate that the pixel is in the On state 25% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a give long-term average Landed Duty Cycle.

Micromirror Landed-On/Landed-Off Duty Cycle (continued)

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 1.

Table 1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	NOMINAL LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point. (1)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 2.

Table 2. Example Landed Duty Cycle for Full-Color Pixels

RED CYCLE PERCENTAGE	GREEN CYCLE PERCENTAGE	BLUE CYCLE PERCENTAGE
50%	20%	30%

RED SCALE VALUE	GREEN SCALE VALUE	BLUE SCALE VALUE	NOMINAL LANDED DUTY CYCLE
0%	0%	0%	0/100
100%	0%	0%	50/50

RED SCALE VALUE	GREEN SCALE VALUE	BLUE SCALE VALUE	NOMINAL LANDED DUTY CYCLE
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the Landed Duty Cycle is any applied image processing. Within the DLPC6401 display controller, the two functions which affect Landed Duty Cycle are Gamma and IntelliBright™.

Gamma is a power function of the form Output_Level = A × $Input\_Level^{Gamma}$, where A is a scaling factor that is typically set to 1.

In the DLPC6401 display controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in Figure 9.

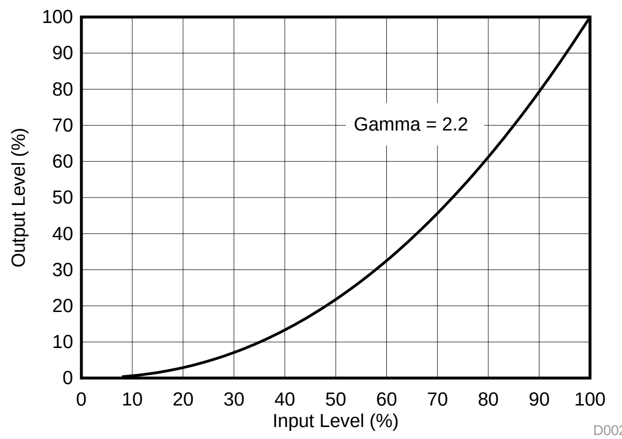


Figure 9. Example of Gamma = 2.2

From Figure 9, if the gray scale value of a given input pixel is 40% (before gamma is applied), then gray scale value will be 13% after gamma is applied. Therefore, it can be seen that since gamma has a direct impact displayed gray scale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithms content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

But while amount of gamma applied to every pixel (of every frame) is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame.

Consideration must also be given to any image processing which occurs before the DLPC6401 display controller.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each optical architecture is derived primarily from the application of the system and the format of the data coming into the DLPC6401 display controller. Applications of interest include accessory projectors, smart projectors, screenless display, embedded in display devices like notebooks, laptops and hot spots.

TI supports the reliability of the DLP4501 DMD only when it is used with DLPC6401 display controller.

8.2 Typical Application

A common application for the DLP4501 chipset is the creation of a pico-projector that can be used as an accessory to a smartphone, tablet or a laptop. The DLPC6401 display controller in the pico-projector embedded module typically receives images/video from a host processor within the product. DLPC6401 display controller then drives the DLP4501 DMD synchronized with the R, G, B LEDs in the optical engine to display the image/video as output of the optical engine.

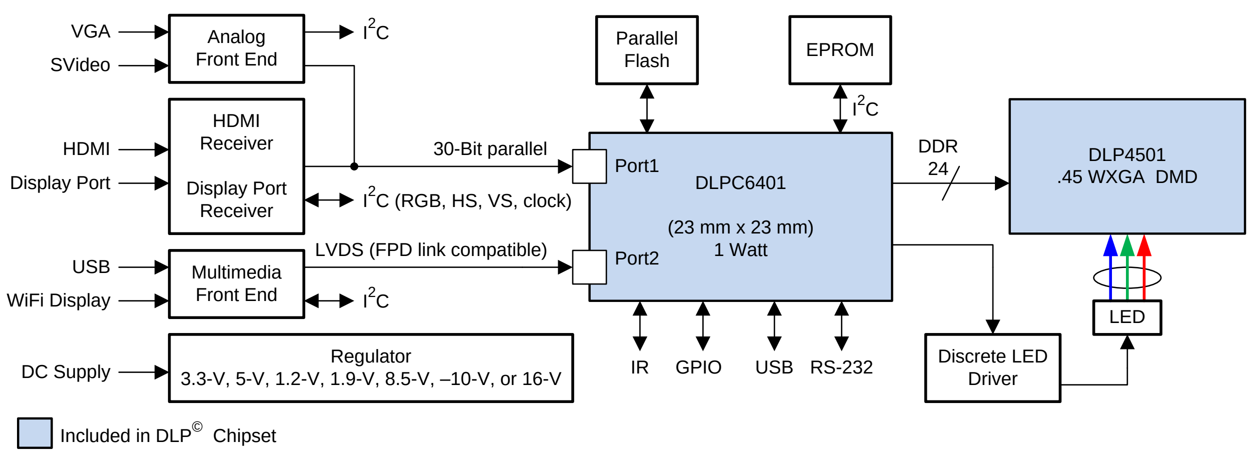


Figure 10. Typical Application Diagram

8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised of a DLP4501 DMD and a DLPC6401 display controller. DLPC6401 display controller controls the digital image processing and DLP4501 DMD is the display device for producing the projected image.

In addition to the two DLP chips in the chip set, other chips may be needed. Typically a Flash part is needed to store the software and firmware. Also a discrete LED driver solution is required to provide the LED driver functionality for LED illumination. The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector. DLPC6401 display controller provides either parallel or LVDS interface to connect the DLPC6401 display controller to the multimedia front end for receiving images and video.

Typical Application (continued)

8.2.2 Detailed Design Procedure

For connecting together the DLPC6401 display controller and the DLP4501 DMD, see the reference design schematic. Layout guidelines should be followed to achieve a reliable projector. To complete the DLP system an optical module or light engine is required that contains the DLP4501 DMD, associated illumination sources, optical elements, and necessary mechanical components.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is non-linear, and the curve for typical relative output changes with LED currents is shown in Figure 11. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue.

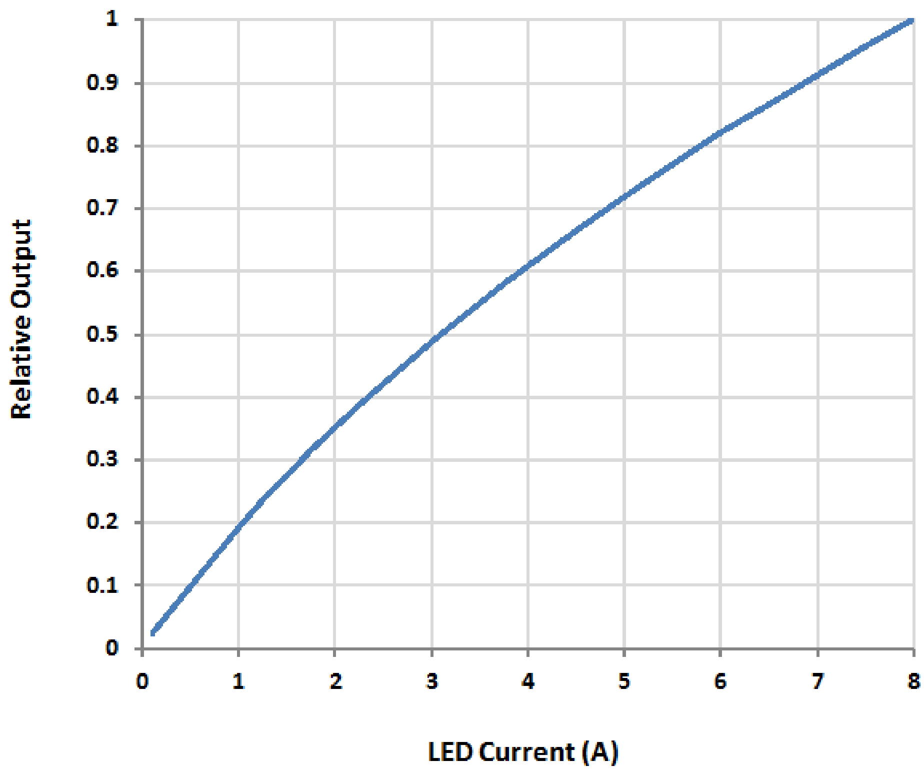


Figure 11. Relative Output vs Current

9 Power Supply Recommendations

The DLP4501 requires VBIAS, VCC, VREF, VOFFSET, and VRESET power supplies . Common ground VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC6401 display controller.

Previous DMDs using external reset waveform drivers have required VCC, VREF, and VOFFSET (sometimes referred to as VCC2) power supplies. Because the DLP4501 generates its own reset waveforms, the additional power supplies VBIAS and VRESET must also be supplied to the DMD. VBIAS, VCC, VREF, VOFFSET, and VRESET power supplies must be coordinated during power-up and power-down operations. Common ground VSS must also be connected.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

VCC, VREF, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. VSS must also be connected.

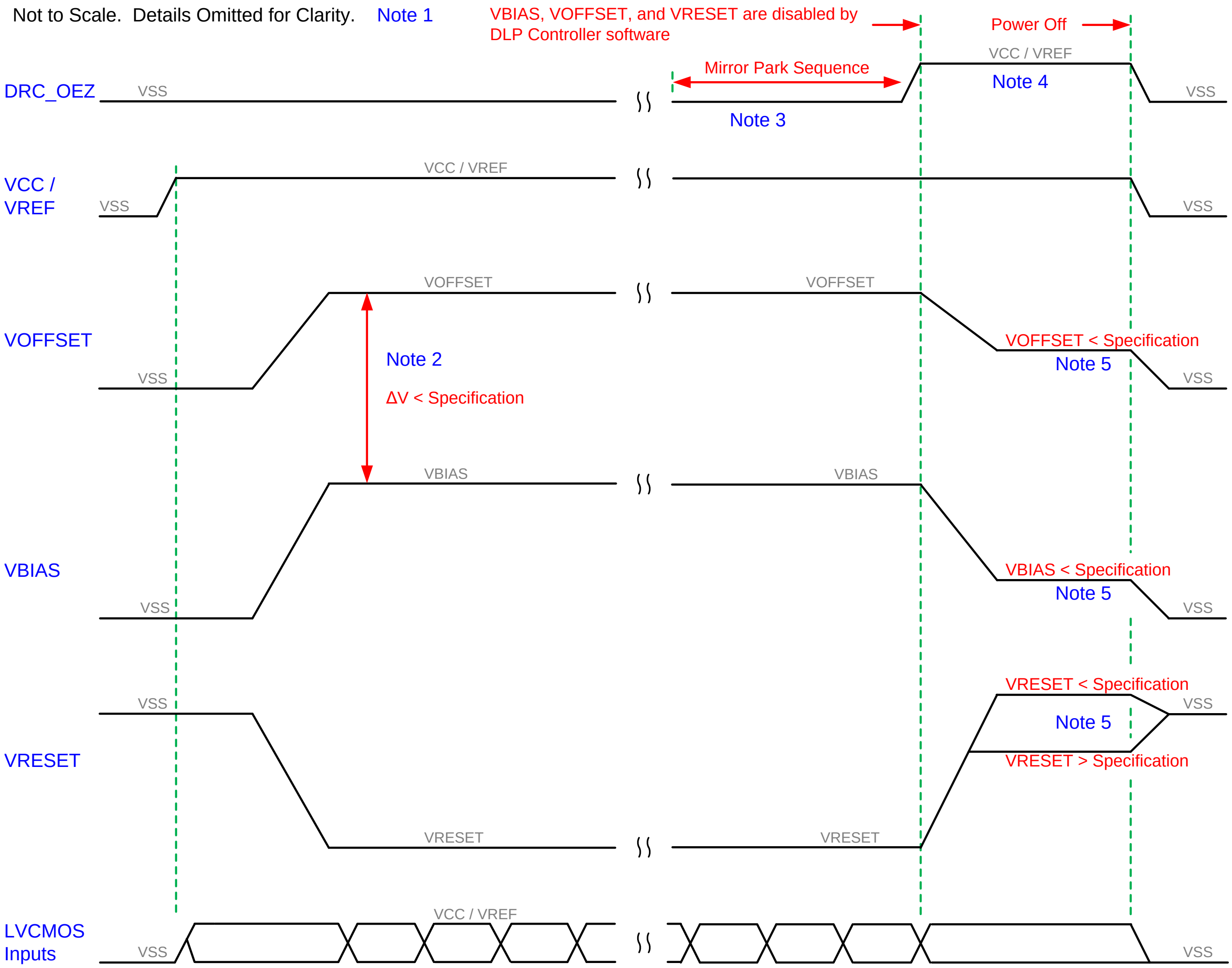
9.1 Power Supply Power-Up Procedure

- During power-up, VCC and VREF must always start and settle before VOFFSET specified in Table 3, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions*. Refer to Table 3 and the *Layout Example* for power-up delay requirements.
- During power-up, LVCMOS input pins shall not be driven high until after VCC and VREF have settled at operating voltages listed in *Recommended Operating Conditions*
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in *Absolute Maximum Ratings* , in *Recommended Operating Conditions* and in Figure 12.

9.2 Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence. VCC and VREF must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions* (Refer to Note 2 for Figure 12).
- During power-down, LVCMOS input pins must be less than specified in *Recommended Operating Conditions*.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in *Absolute Maximum Ratings*, in *Recommended Operating Conditions* and in Figure 12.

9.3 Power Supply Sequencing Requirements



(1) See *Absolute Maximum Ratings*, *Recommended Operating Conditions*, and *Package Pin Functions*. Figure 12 is not to scale and details have been omitted for clarity.

(2) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in *Recommended Operating Conditions*. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down..

(3) During the mirror parking process, VBIAS, VRESET, VOFFSET, VCC, VREF, and VSS power supplies are all required to be within specifications listed in Recommended Operating Conditions. Once the mirrors are parked, VBIAS, VRESET, and VOFFSET may be turned off. Then, VCC, VREF, and VSS power supplies may remain enabled or be turned off.

(4) When system power is interrupted, the DLP Controller initiates hardware power-down that disables VBIAS, VRESET and VOFFSET after the micromirror park sequence. VBIAS, VRESET and VOFFSET are disabled after the mirror park sequence through software control.

(5) Refer to the DMD *Power-Down Sequence Requirements* table for specifications.

Figure 12. Power Supply Sequencing Requirements (Power Up and Power Down)

Table 3. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
V_{BIAS}	Supply voltage level during power–down sequence		4.0	V
V_{OFFSET}	Supply voltage level during power–down sequence		4.0	V
V_{RESET}	Supply voltage level during power–down sequence	–4.0	0.5	V

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board to board connector to a flex cable. Flex cable provides the interface of data and Ctrl signals between the DLPC6401 display controller and the DLP4501 DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Minimum of 100-nF decoupling capacitor close to VBIAS. Capacitor C5 in Figure 13.
- Minimum of 100-nF decoupling capacitor close to VRST. Capacitor C4 in Figure 13.
- Minimum of 100-nF decoupling capacitor close to VOFS. Capacitor C3 in Figure 13.
- Minimum of 100-nF decoupling capacitor close to both groups of VCC pins, for a total of 200-nF for VCC. Capacitor C1/C6 in Figure 13.
- Minimum of 100-nF decoupling capacitor close to VREF. Capacitor C2 in Figure 13.

10.2 Layout Example

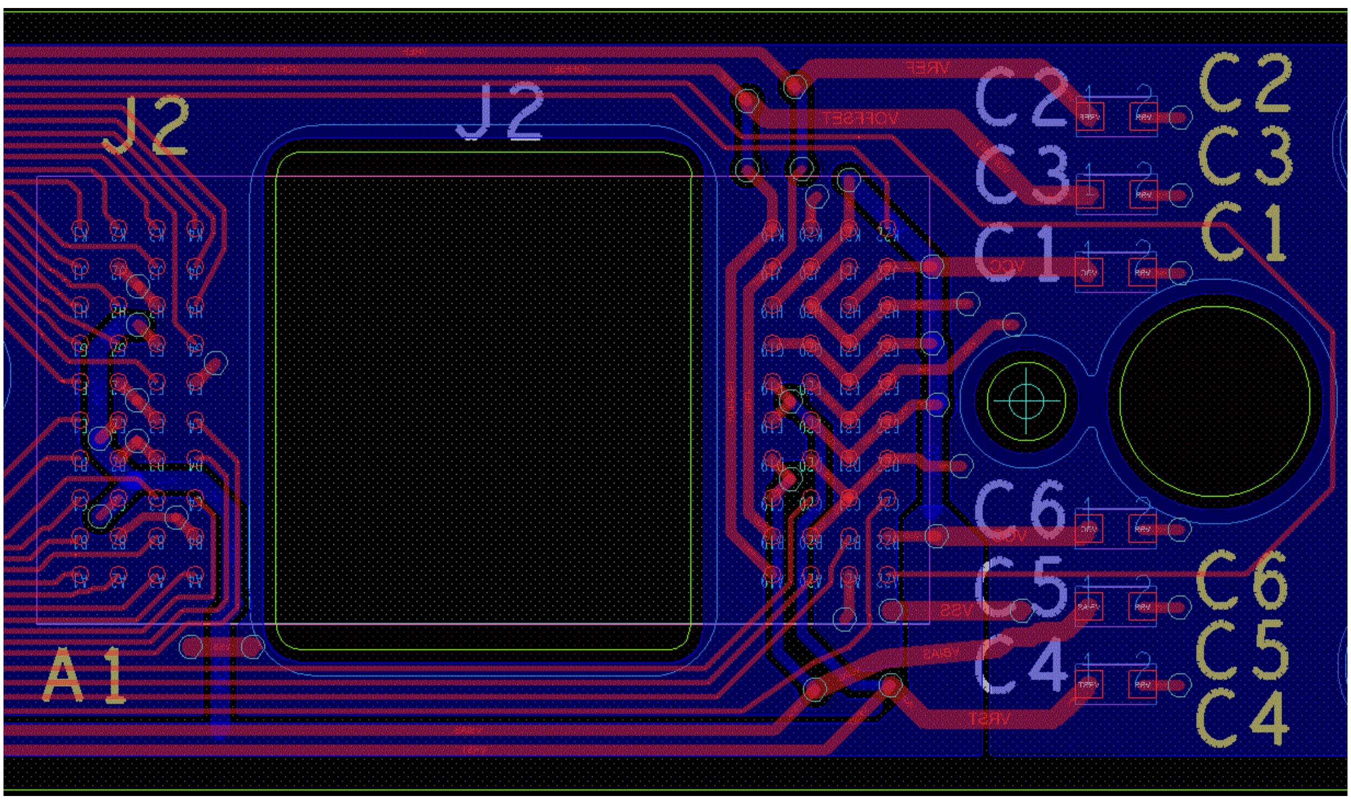


Figure 13. Power Supply Connections

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

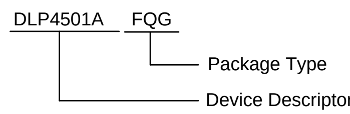


Figure 14. Part Number Description

Device Status:

A lead alpha character of “X” implies the device has been released for restricted sales only.

When no lead alpha character (*) is present, the device has been released for unrestricted sales.

11.1.2 Device Markings

Device Marking will include the human–readable character string GHJJJJK 1191-413BF. GHJJJJK is the lot trace code. 1191-413BF is the device part number.

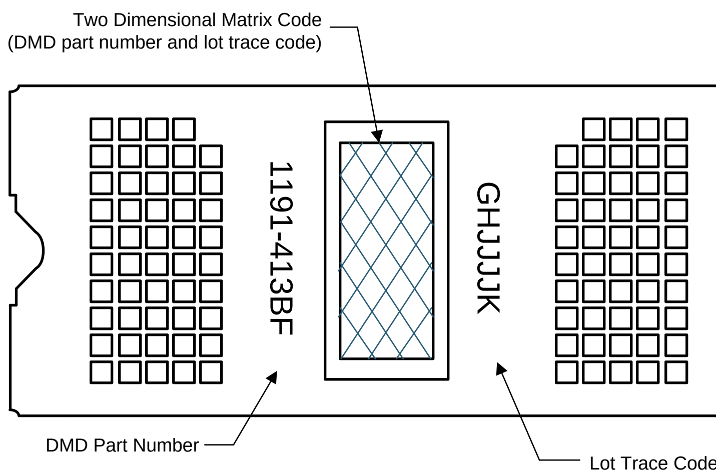


Figure 15. DMD Marking

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLP4501	Click here	Click here	Click here	Click here	Click here
DLPC6401	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

IntelliBright, E2E are trademarks of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP4501AFQG	ACTIVE	CLGA	FQG	80	70	RoHS & non-Green	Call TI	Call TI			Samples
DLP4501FQG	ACTIVE	CLGA	FQG	80	70	TBD	Call TI	Call TI	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

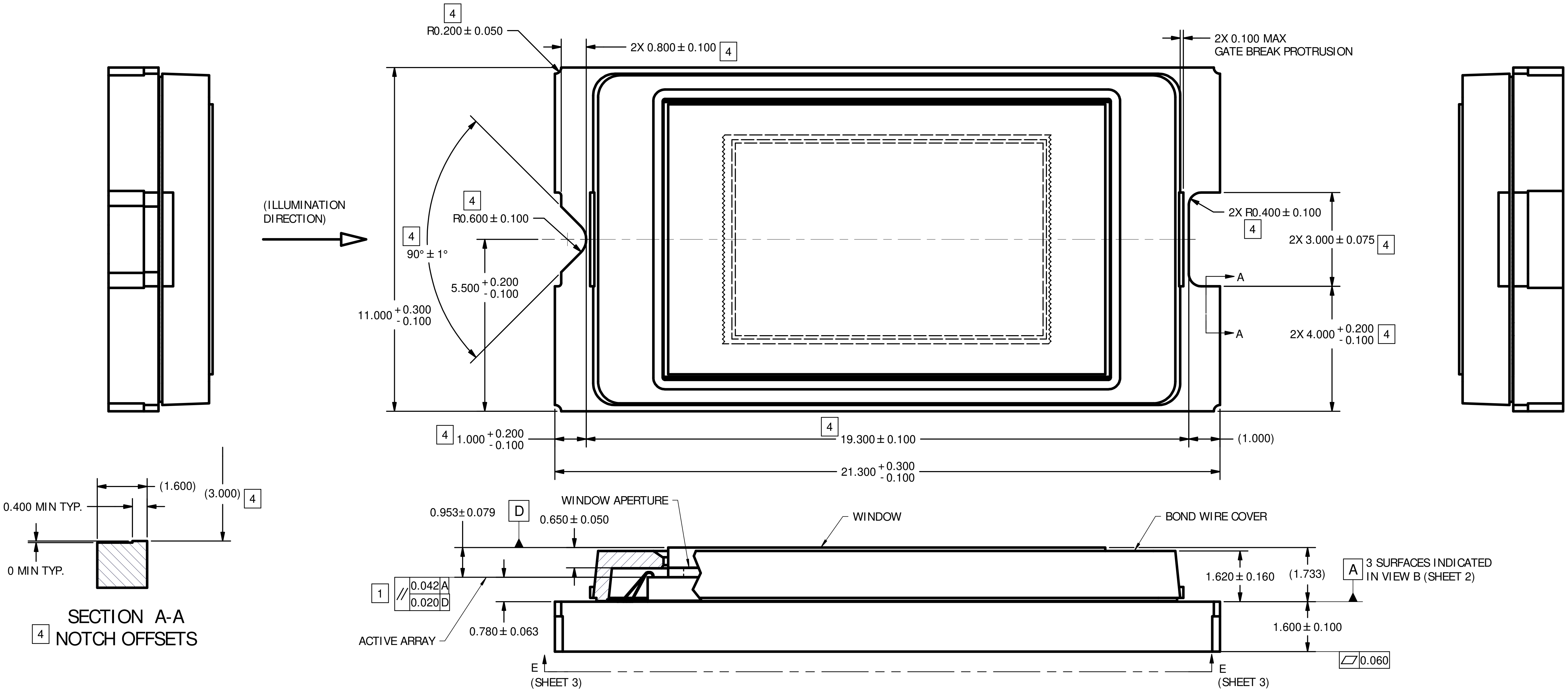
DWG NO. 2512084 SH 1

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
5. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, WHEN MOUNTING IN SYSTEM.

REVISIONS

REV	DESCRIPTION	DATE	BY
A	ECO 2121536: INITIAL RELEASE	1/9/2012	BMH
B	ECO 2125510: RELAX BOND WIRE COVER HEIGHT TOL	6/20/2012	BMH
C	ECO 2125965: TIGHTEN DIE HEIGHT TOL, WAS +/-0.080	7/11/2012	BMH



NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

	NAME	DATE
DRAWN	B. HASKETT	1/9/2012
ENGINEER	B. HASKETT	1/9/2012
QA/CE	C. BEARD	1/12/2012
CM	F. ARMSTRONG	1/13/2012
	J. HALL	1/9/2012
APPROVED	M. DORAK	1/10/2012

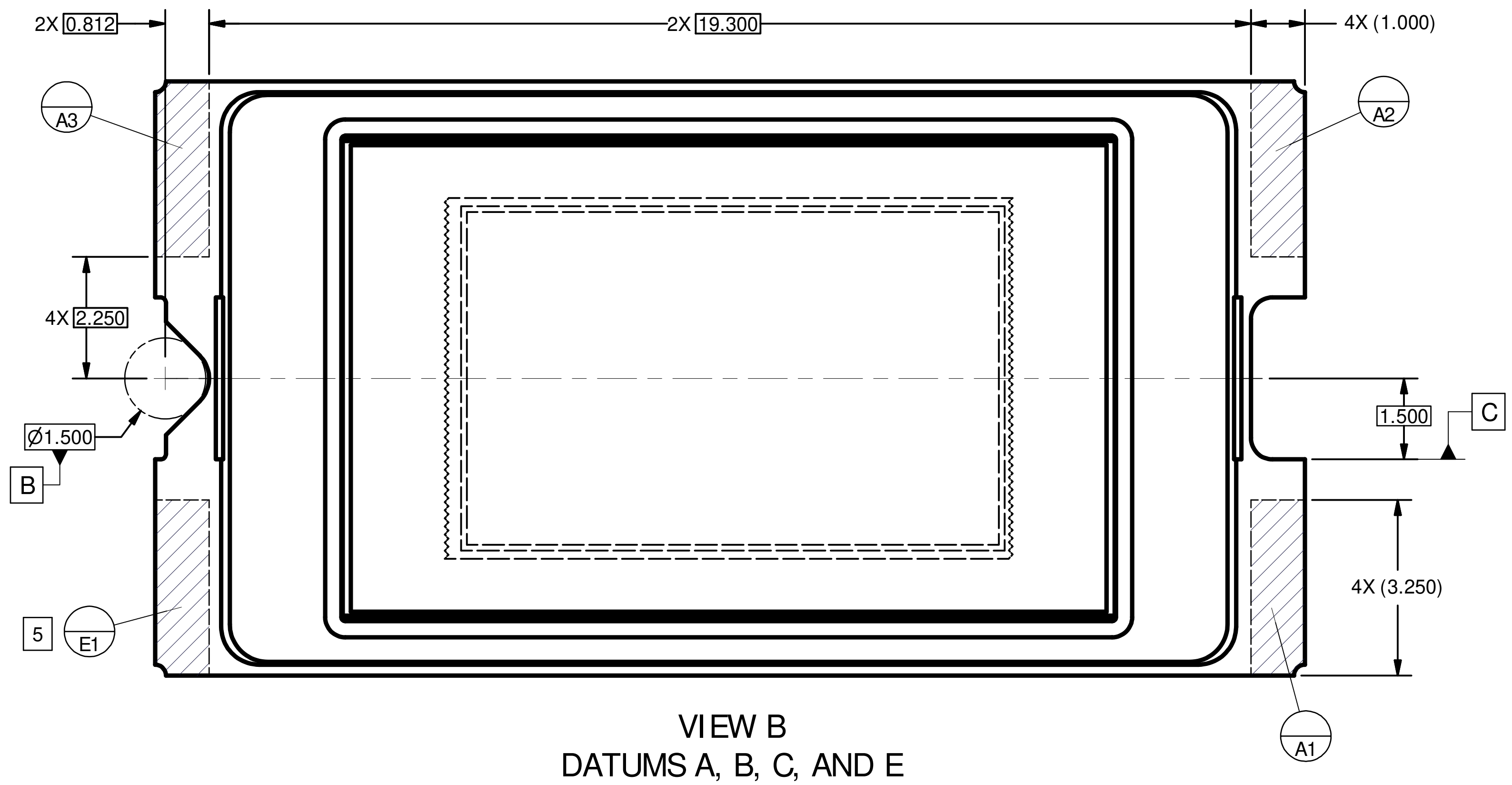
TEXAS INSTRUMENTS
Dallas Texas

TITLE
ICD, MECHANICAL, DMD, .45 WXGA-800 DDR SERIES 311

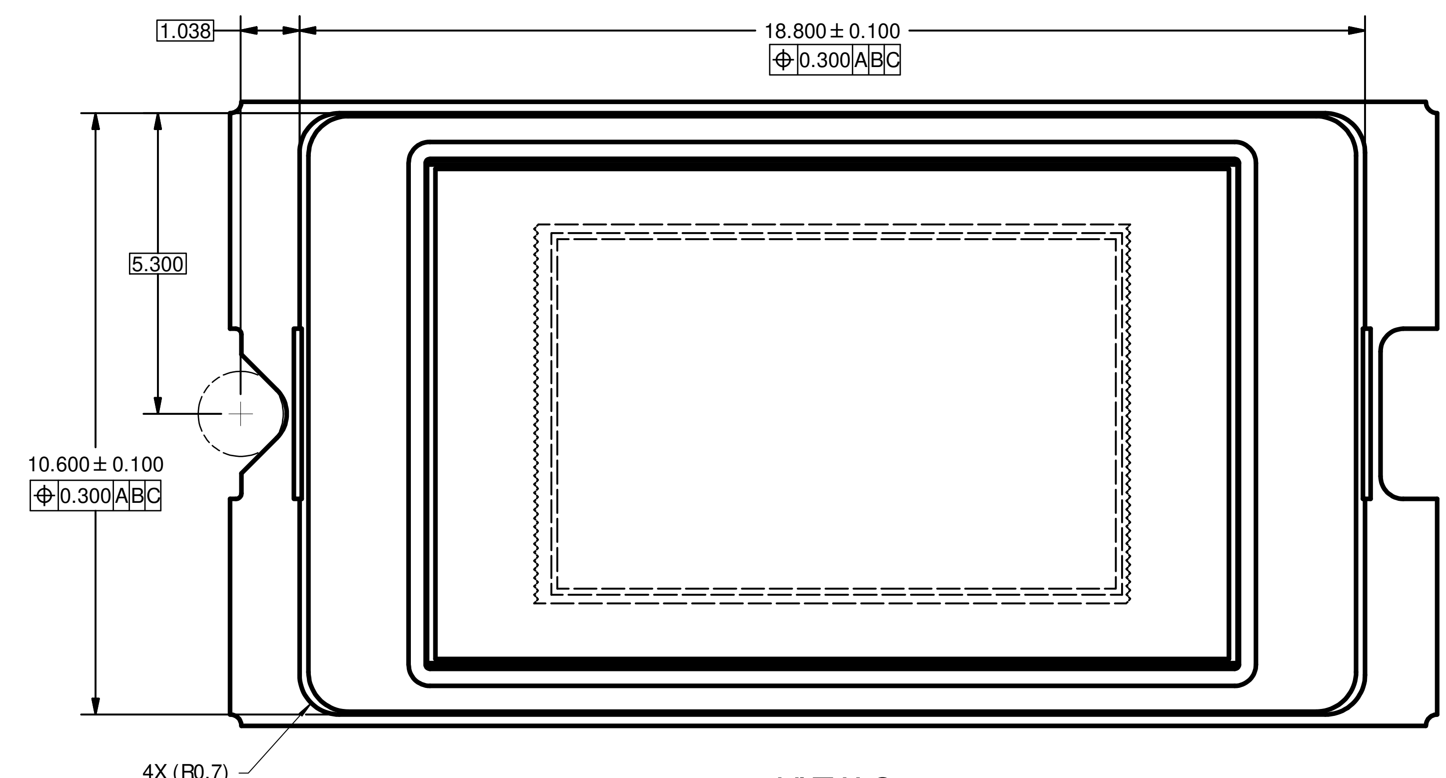
SIZE D | DWG NO 2512084 | REV C

SCALE 15:1 | SHEET 1 OF 3

INV11-2006a

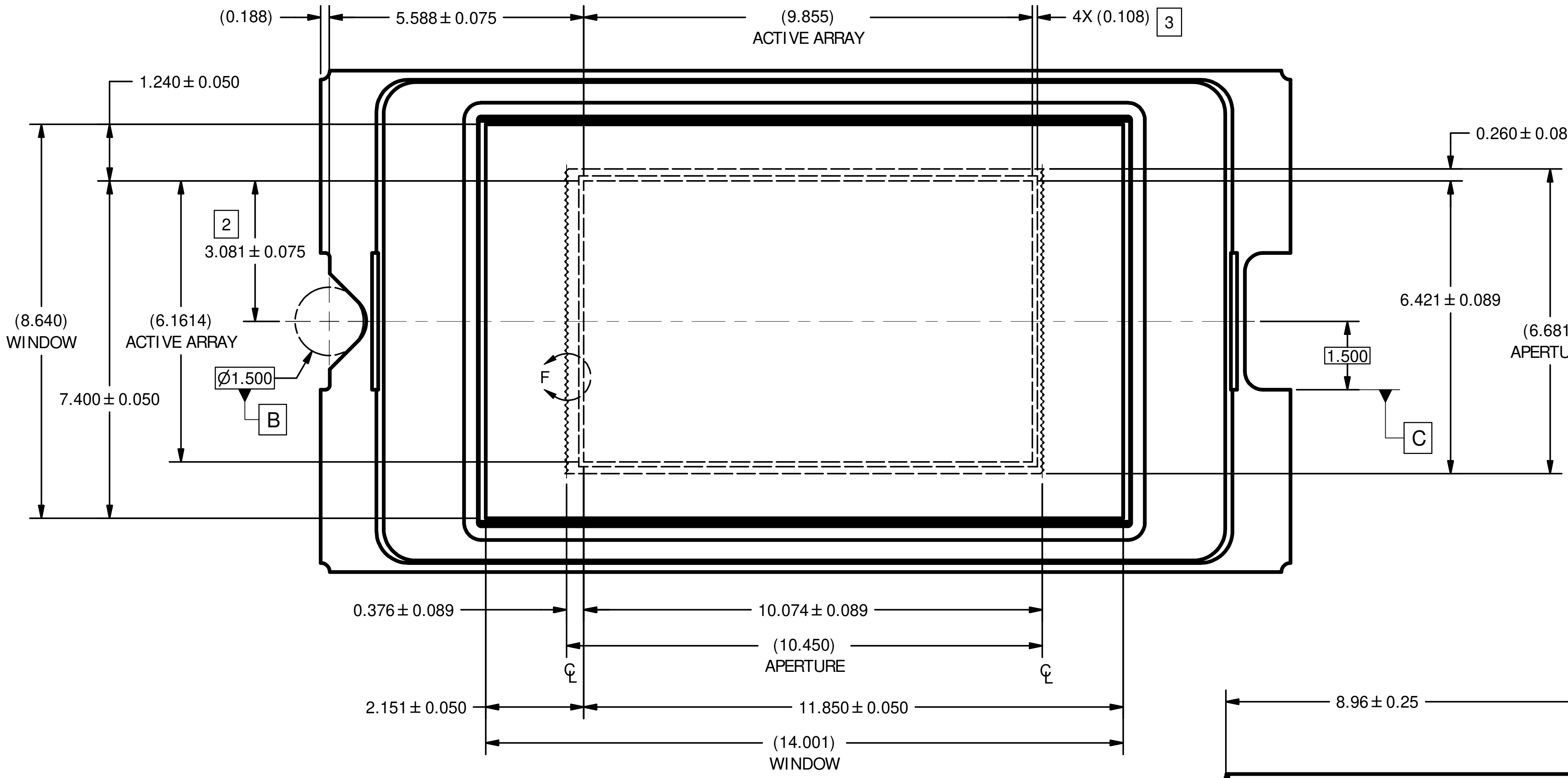


VIEW B
DATUMS A, B, C, AND E
SCALE 15 : 1
(FROM SHEET 1)

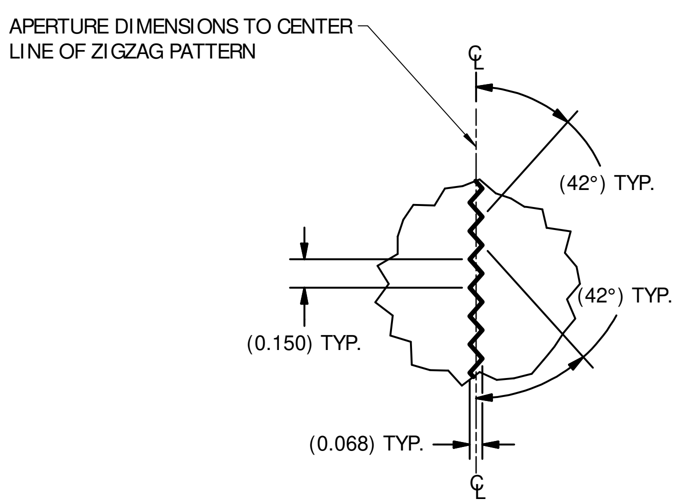


VIEW C
BOND WIRE COVER X/Y DIMENSIONS
SCALE 15 : 1
(FROM SHEET 1)

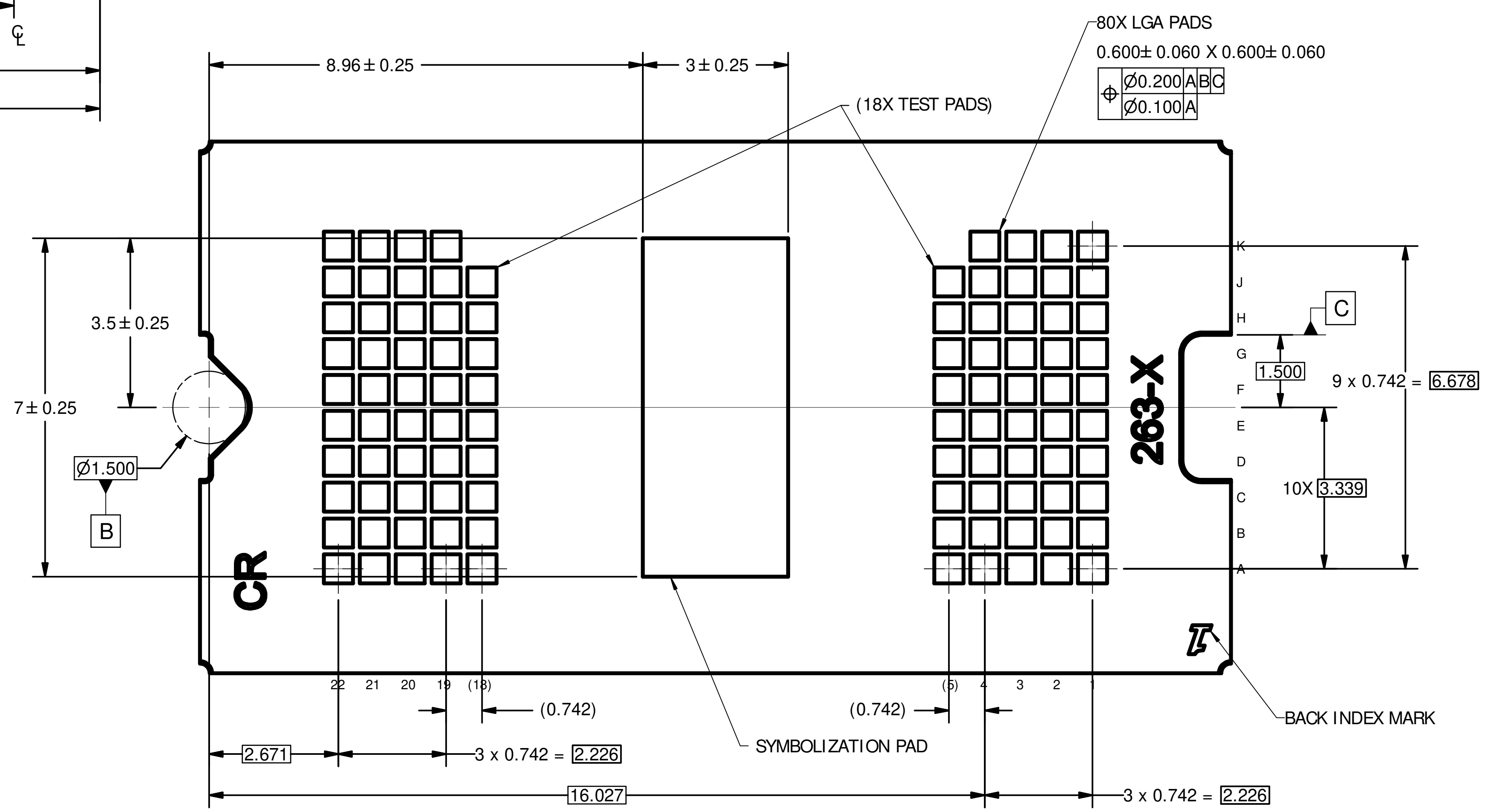
TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 1/9/2012	SIZE D	DWG NO 2512084	REV C
			SCALE	SHEET 2 OF 3	



VIEW D
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE SHORT EDGES
SCALE 50 : 1



VIEW E-E
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 1/9/2012	SIZE D	DWG NO 2512084	REV C
			SCALE	SHEET 3 OF 3	

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265