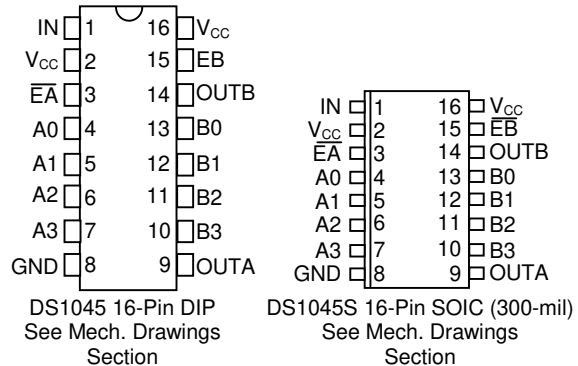# DS1045
4-Bit Dual Programmable Delay Line

FEATURES

- All-silicon time delay
- Two programmable outputs from a single input produce output-to-output delays between 9ns and 84ns depending on device type
- Programmable via four input pins
- Programmable increments of 3ns to 5ns with a minimum of 9ns and a maximum of 84ns
- Output pulse is a reproduction of input pulse after
- Delay with both leading and trailing edge accuracy
- Standard 16-pin DIP or surface mount 16-pin SOIC
- Auto-insertable
- Low-power CMOS design is TTL-compatible

PIN ASSIGNMENT

IN	1		16	V_{CC}
V_{CC}	2		15	EB
$\overline{EA}$	3		14	OUTB
A0	4		13	B0
A1	5		12	B1
A2	6		11	B2
A3	7		10	B3
GND	8		9	OUTA

DS1045 16-Pin DIP
See Mech. Drawings Section

IN	1		16	V_{CC}
V_{CC}	2		15	$\overline{EB}$
$\overline{EA}$	3		14	OUTB
A0	4		13	B0
A1	5		12	B1
A2	6		11	B2
A3	7		10	B3
GND	8		9	OUTA

DS1045S 16-Pin SOIC (300-mil)
See Mech. Drawings Section

PIN DESCRIPTION

IN	- Delay Line Input
OUTA, OUTB	- Delay Line Outputs
A0-A3	- Parallel Program Inputs for OUT1
B0-B3	- Parallel Program Inputs for OUT2
$\overline{EA}$, $\overline{EB}$	- Enable A and B Inputs
V_{CC}	- +5V Input
GND	- Ground

DESCRIPTION

The DS1045 is a programmable silicon delay line having one input and two 4-bit programmable delay outputs. Each 4-bit programmable output offers the user 16 possible delay values to select from, starting with a minimum inherent DS1045 delay of 9ns and a maximum achievable delay in the standard DS1045 family of 84ns. The standard DS1045 product line provides the user with three devices having uniform delay increments of 3ns, 4ns, and 5ns, depending on the device. Table 1 presents standard device family and delay capability. Additionally, custom delay increments are available for special order through Dallas Semiconductor.

The DS1045 is TTL and CMOS-compatible and capable of driving ten 74LS-type loads. The output produced by the DS1045 is both rising and falling edge precise. The DS1045 programmable silicon delay line has been designed as a reliable, economic alternative to hybrid programmable delay lines. It is offered in a standard 16-pin auto-insertable DIP and a space-saving surface mount 16-pin SOIC package.

PARALLEL PROGRAMMING

Parallel programming of the DS1045 is accomplished via the set of parallel inputs A0-A3 and B0-B3 as shown in Figure 1. Parallel input A0-A3 and B0-B3 accept TTL levels and are used to set the delay values of outputs OUTA and OUTB, respectively. Sixteen possible delay values between the minimum 9ns delay and the maximum delay of the DS1045-x device version can be selected using the parallel programming inputs A0-A3 or B0-B3 (see Table 2, "Delay vs. Programmed Input"). For example, the DS1045-3 outputs OUTA or OUTB and can be programmed to produce 16 possible delays between the 9ns (minimum) and the 54ns (maximum) in 3ns increment levels.

For applications that do not require frequent reprogramming, the parallel inputs can be set using fixed logic levels, as would be produced by jumpers, DIP switches, or TTL levels as produced by computer systems. Maximum flexibility in parallel programming can be achieved when inputs are set by computer-generated data. By using the enable input pins for each respective programmed output and observing the input setup (t_{DSE}) and hold time (t_{DHE}) requirements, data can be latched on an 8-bit bus. If the enable pins, $\overline{EA}$ and $\overline{EB}$, are not used to latch data, they should be set to a logic level 1. After each change in the programmed delay value, a settling time (t_{EDV}) or (t_{PDV}) is required before the delayed output signal is reliably produced. Since the DS1045 is a CMOS design, undefined input pins should be connected to well defined logic levels and not left floating.
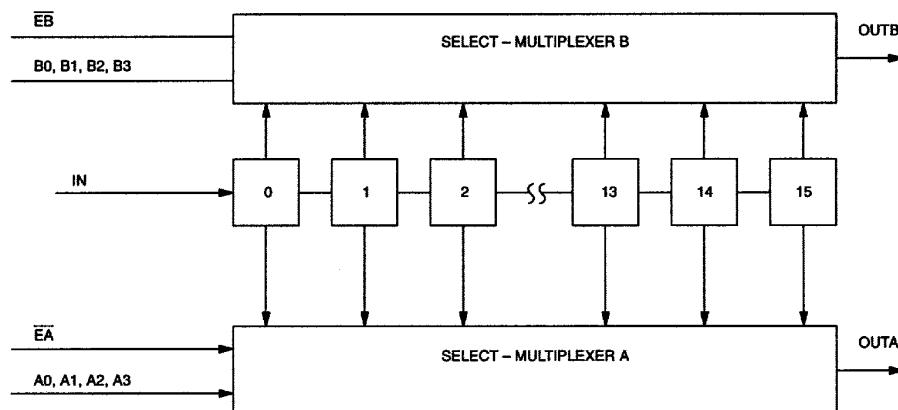
PART NUMBER TABLE Table 1

PART NUMBER	STEP ZERO DELAY	MAX DELAY TIME	MAX DELAY TOLERANCE
DS1045-3	9 ± 1ns	54ns	±2.5ns
DS1045-4	9 ± 1ns	69ns	±3.3ns
DS1045-5	9 ± 1ns	84ns	±4.1ns

NOTE:

Additional delay step times are available from Dallas Semiconductor by special order. Consult factory for availability.

BLOCK DIAGRAM Figure 1

DELAY VS. PROGRAMMED VALUE Table 2

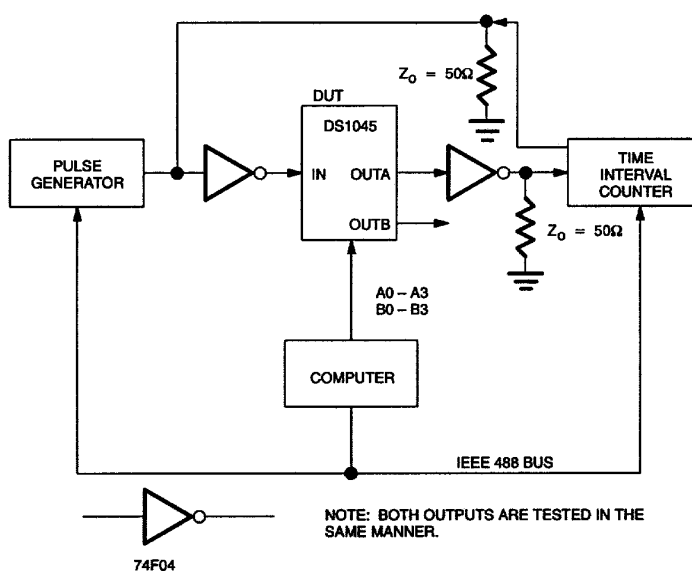| PART NUMBER	OUTPUT DELAY VALUE															
DS1045-3	9	12	15	18	21	24	27	30	33	36	39	42	45	48	51	54
DS1045-4	9	13	17	21	25	29	33	37	41	45	49	53	57	61	65	69
DS1045-5	9	14	19	24	29	34	39	44	49	54	59	64	69	74	79	84
PROGRAM VALUES FOR EACH DELAY VALUE																
A0 OR B0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
A1 OR B1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
A2 OR B2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A3 OR B3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

DS1045 TEST CIRCUIT Figure 2

TEST SETUP DESCRIPTION

Figure 2 illustrates the hardware configuration used for measuring the timing parameters of the DS1045. The input waveform is produced by a precision pulse generator under software control. Time delays are measured by a time interval counter (20 ps resolution) connected to the output. The DS1045 parallel inputs are controlled by an interface to a central computer. All measurements are fully automated with each instrument controlled by the computer over an IEEE 488 bus.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A specification
Short Circuit Output Current	50mA for 1 second

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS   (0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}		4.75	5.0	5.25	V	1
Input Logic 1	V_{IH}		2.2		V_{CC} +0.5	V	1
Input Logic 0	V_{IL}		-0.5		0.8	µA	1
Input Leakage	I_I	$0 \leq V_I \leq V_{CC}$	-1.0		+1.0	µA	
Active Current	I_{CC}	V_{CC}=5.25V PERIOD=1 µs			35.0	mA	
Logic 1 Output Current	I_{OH}	V_{CC}= 4.75V V_{OH}= 4.0V			-1.0	mA	
Logic 0 Output Current	I_{OL}	V_{CC}= 4.75V V_{OL}= 0.5V	8			mA	

AC ELECTRICAL CHARACTERISTICS   (0°C to 70°C; V_{CC} 5V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Period	t_{PERIOD}	4 x t_{WI}			ns	
Pulse Width	t_{WI}	100% of output delay			ns	
Input to Output Delay	t_{PLH}, t_{PHL}		Table 1		ns	2
Parallel Input Change to Delay Invalid	t_{PDX}	0			ns	
Parallel Input Valid to Delay Valid	t_{PDV}		10		ns	
Enable Width	t_{EW}	15			ns	
Data Setup to Enable	t_{DSE}	10			ns	
Data Hold from Enable	t_{DHE}	0			ns	
Enable to Delay Invalid	t_{EDX}		5		ns	
Enable to Delay Valid	t_{EDV}		15		ns	

CAPACITANCE $(T_A = 25°C)$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			10	pF	

TEST CONDITIONS

T_A=25°C ± 3°C

V_{CC}= 5.0V ± 0.1V

Input Pulse = 3.0V high to 0.0V low ± 0.1V

Input Source Impedance = 50Ω maximum

Rise and fall times = 3.0ns max. between 0.6V and 2.4V
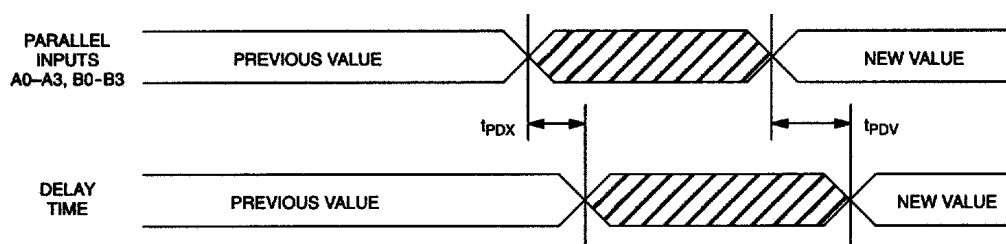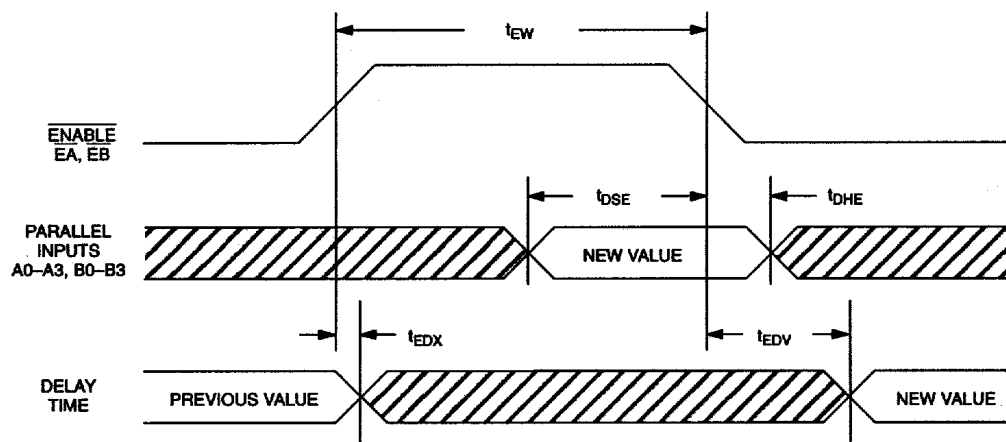
Pulse Width = 250ns

Period = 500ns

Output Load = 74F04
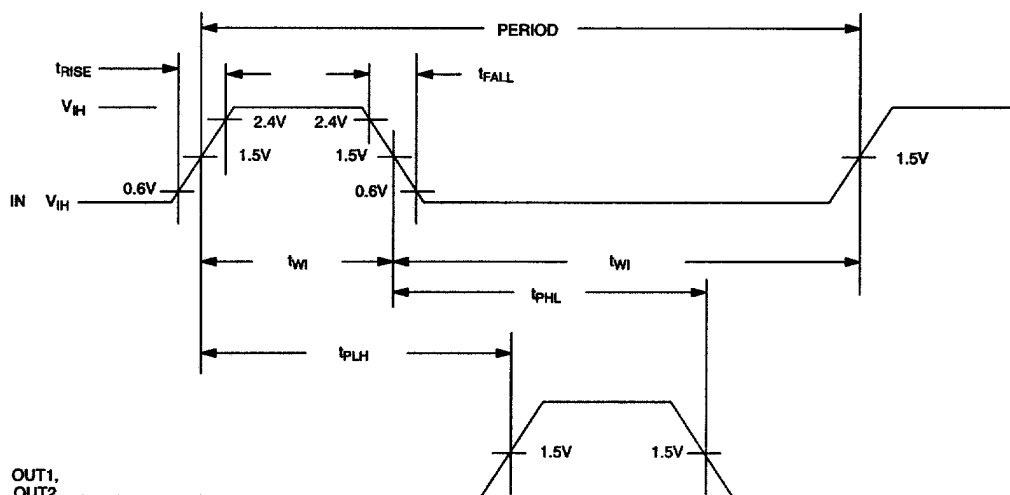
Measurement Point = 1.5V on inputs and outputs

Output Load Capacitance = 15pF

NOTE:

Above conditions are for test only and do not restrict the operation of the device under other data sheet conditions.

TIMING DIAGRAM: NON-LATCHED PARALLEL MODE, $\overline{EA}$, $\overline{EB}$ = V_{IH}

TIMING DIAGRAM: LATCHED PARALLEL MODE

TIMING DIAGRAM: DS1045 INPUTS TO OUTPUTS

TERMINOLOGY

PERIOD: The time elapsed between the leading edge of the first pulse and the leading edge of the following pulse.

t$_{WI}$ (Pulse Width): The elapsed time on the pulse between the 1.5V point on the leading edge and the 1.5V point on the trailing edge, or the 1.5V point on the trailing edge and the 1.5V on the leading edge.

t$_{RISE}$ (Input Rise Time): The elapsed time between the 20% and the 80% point on the leading edge of the input pulse.

t$_{FALL}$ (Input Fall Time): The elapsed time between the 80% and the 20% point on the trailing edge of the input pulse.

t$_{PLH}$ (Time Delay, Rising): The elapsed time between the 1.5V point on the leading edge of the input pulse and the 1.5V point on the leading edge of the output pulse.

t$_{PHL}$ (Time Delay, Falling): The elapsed time between the 1.5V point on the trailing edge of the input pulse and the 1.5V point on the trailing edge of the output pulse.

NOTES:
1. All voltages are referenced to ground.

2. @ V$_{CC}$ = 5V and 25°C. Delay accurate on both rising and falling edges within tolerances given in Table 1.