

Automotive-grade N-channel 40 V, 0.8 mΩ typ., 200 A STripFET™ F7 Power MOSFETs in H²PAK-2 and H²PAK-6 packages

Datasheet - production data

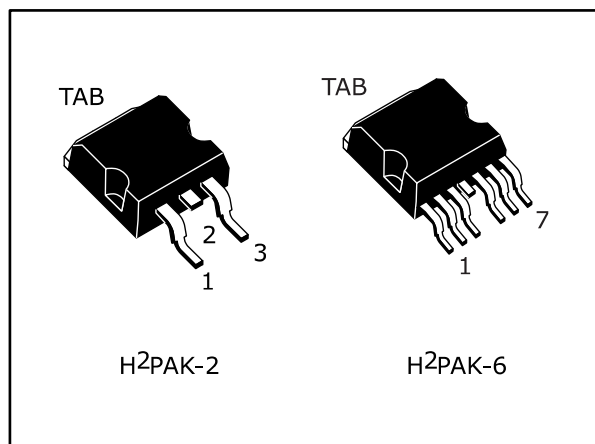
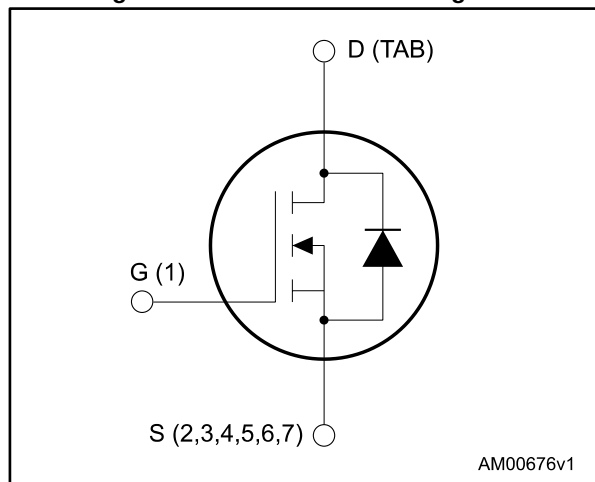


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STH410N4F7-2AG	40 V	1.1 mΩ	200 A	365 W
STH410N4F7-6AG				

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest R_{DS(on)} on the market
- Excellent figure of merit (FoM)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STH410N4F7-2AG	410N4F7	H ² PAK-2	Tape And Reel
STH410N4F7-6AG		H ² PAK-6	

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package information	9
	4.1 H ² PAK-2 package information.....	10
	4.2 H ² PAK-6 package information.....	13
	4.3 H ² PAK packing information	16
5	Revision history	18

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	200	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	200	
$I_{DM}^{(2)}$	Drain current (pulsed)	800	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ °C}$	365	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	1.9	J
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		

Notes:

⁽¹⁾ Current is limited by package, the current capability of the silicon is 420 A at 25 °C.

⁽²⁾ Pulse width is limited by safe operating area.

⁽³⁾ $T_j \leq 175\text{ °C}$, $I_{av}=80A$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.41	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	

Notes:

⁽¹⁾ When mounted on a 1-inch² FR-4 board, 2oz Cu.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	40			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 40\text{ V}$			10	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 40\text{ V}$, $T_{\text{case}} = 125\text{ °C}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = 20\text{ V}$			200	nA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 90\text{ A}$		0.8	1.1	$\text{m}\Omega$

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	11500	-	pF
C_{oss}	Output capacitance		-	3500	-	
C_{rss}	Reverse transfer capacitance		-	390	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 20\text{ V}$, $I_{\text{D}} = 180\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	141	-	nC
Q_{gs}	Gate-source charge		-	65	-	
Q_{gd}	Gate-drain charge		-	27	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{DD}} = 20\text{ V}$, $I_{\text{D}} = 90\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	35	-	ns
t_{r}	Rise time		-	198	-	
$t_{\text{d}(\text{off})}$	Turn-off delay time		-	108	-	
t_{f}	Fall time		-	44.2	-	

Table 7: Source-drain diode

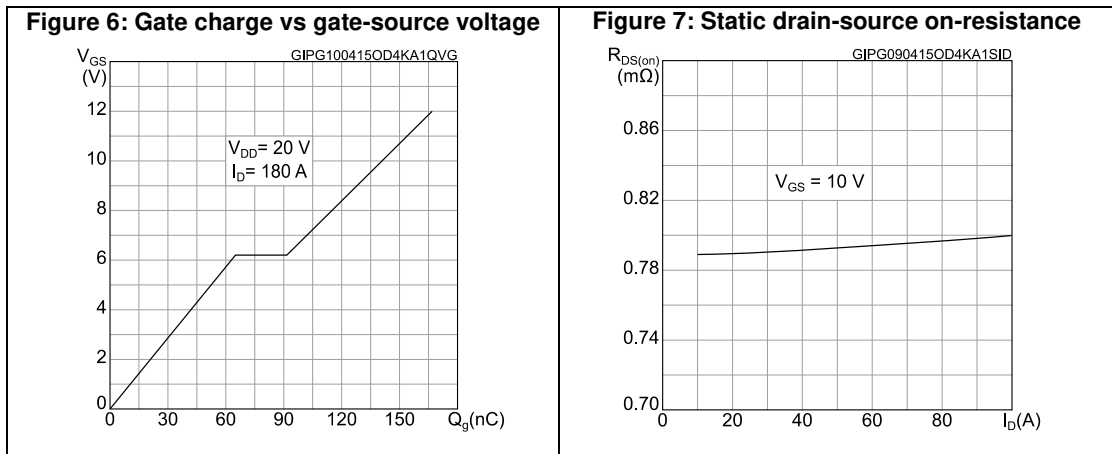
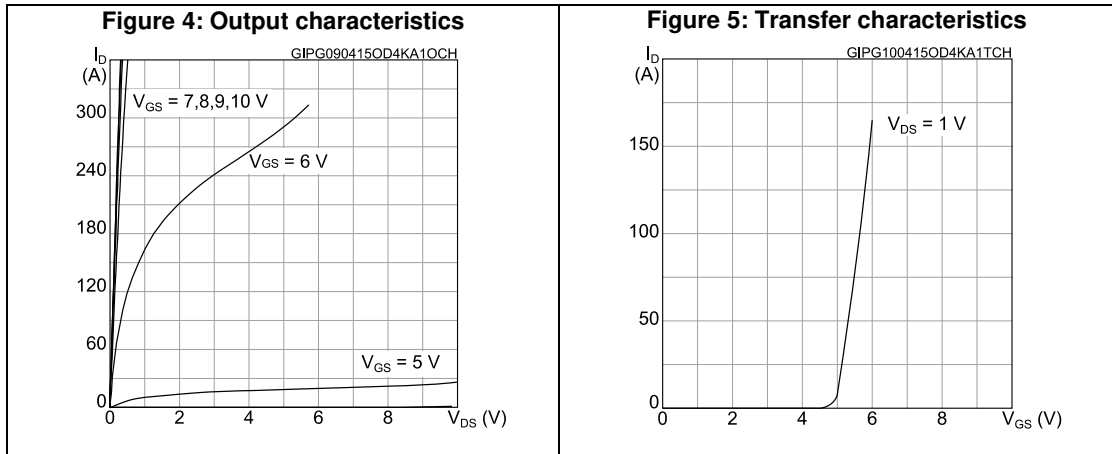
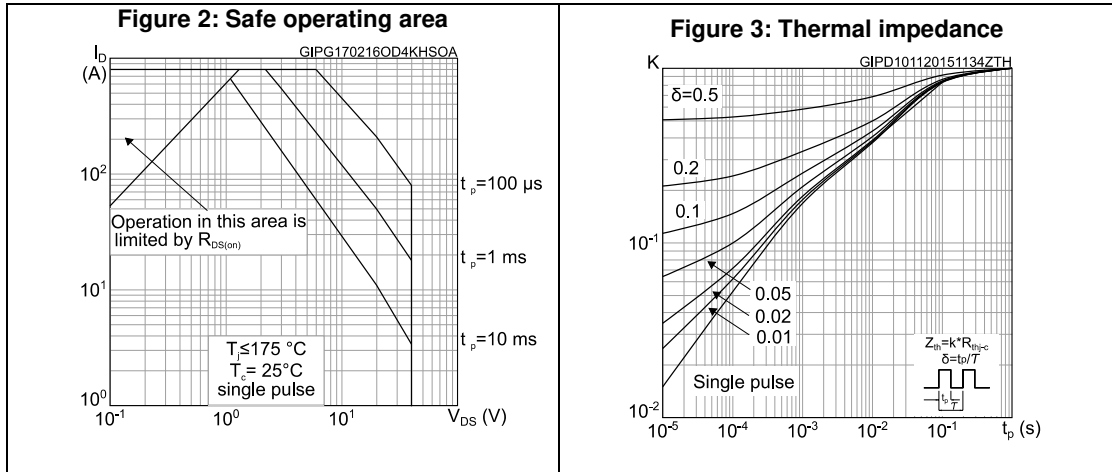
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		200	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 90\text{ A}$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 180\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 32\text{ V}$, $T_j = 25\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	74.4		ns
Q_{rr}	Reverse recovery charge		-	115		nC
I_{RRM}	Reverse recovery current		-	3.1		A

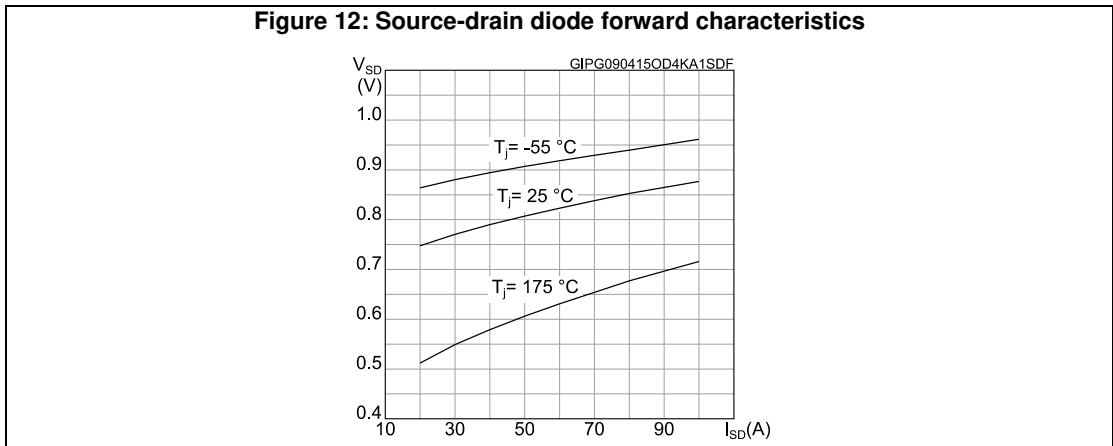
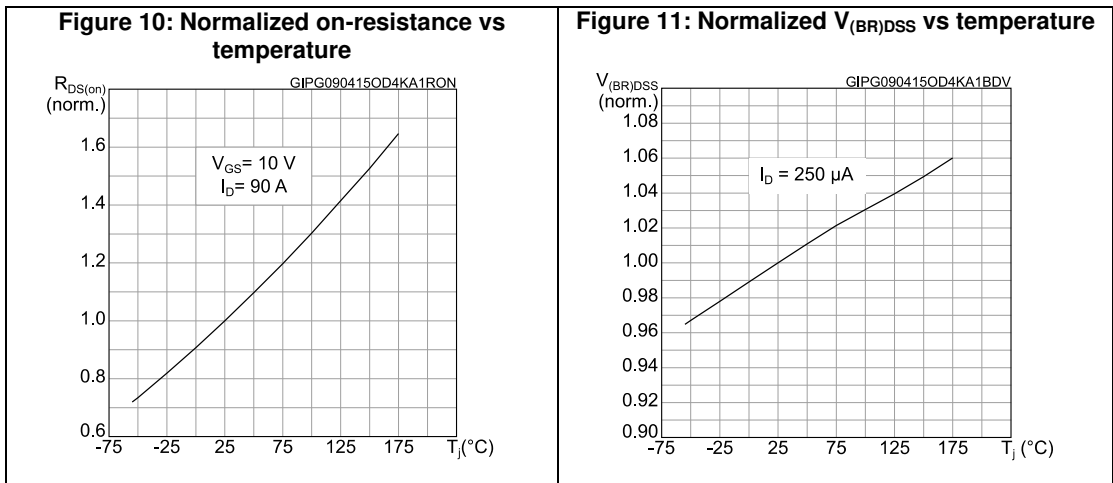
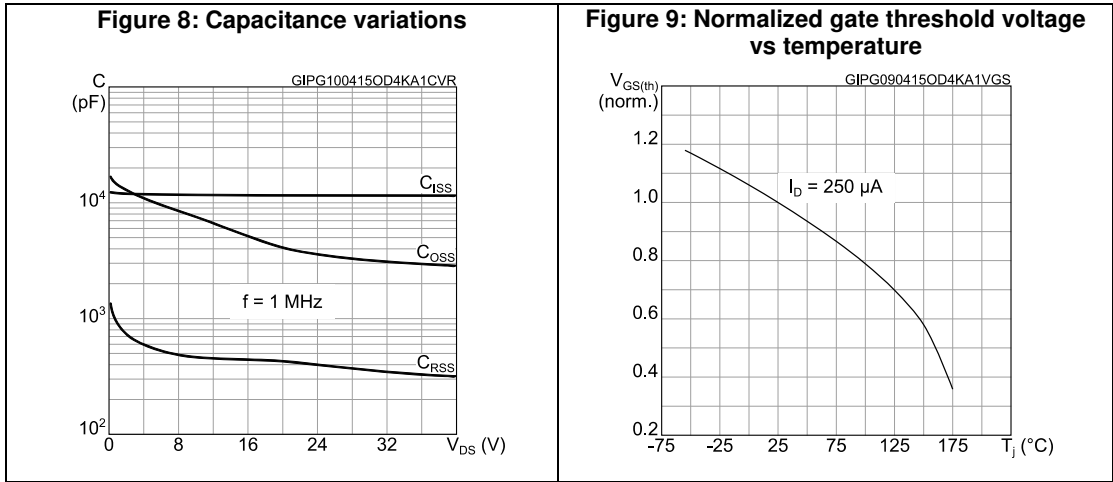
Notes:

⁽¹⁾ Limited by package, 420 A current allowed by silicon.

⁽²⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

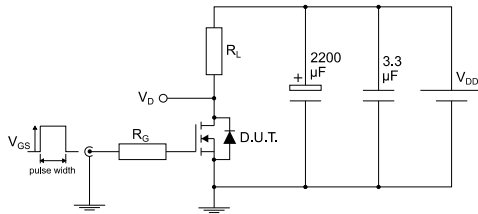
2.2 Electrical characteristics (curves)





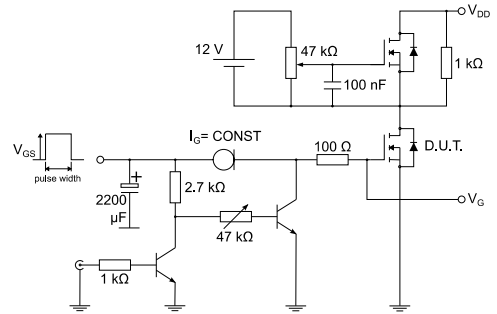
3 Test circuits

Figure 13: Test circuit for resistive load switching times



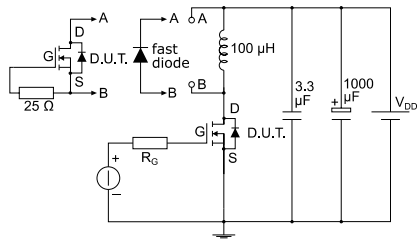
AM01468v1

Figure 14: Test circuit for gate charge behavior



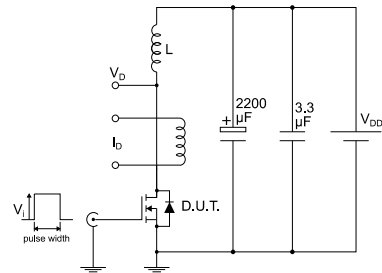
AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



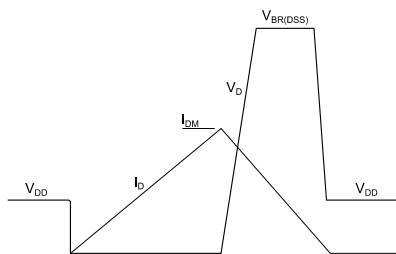
AM01470v1

Figure 16: Unclamped inductive load test circuit



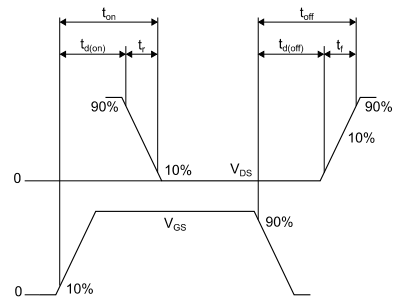
AM01471v1

Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 H²PAK-2 package information

Figure 19: H²PAK-2 package outline

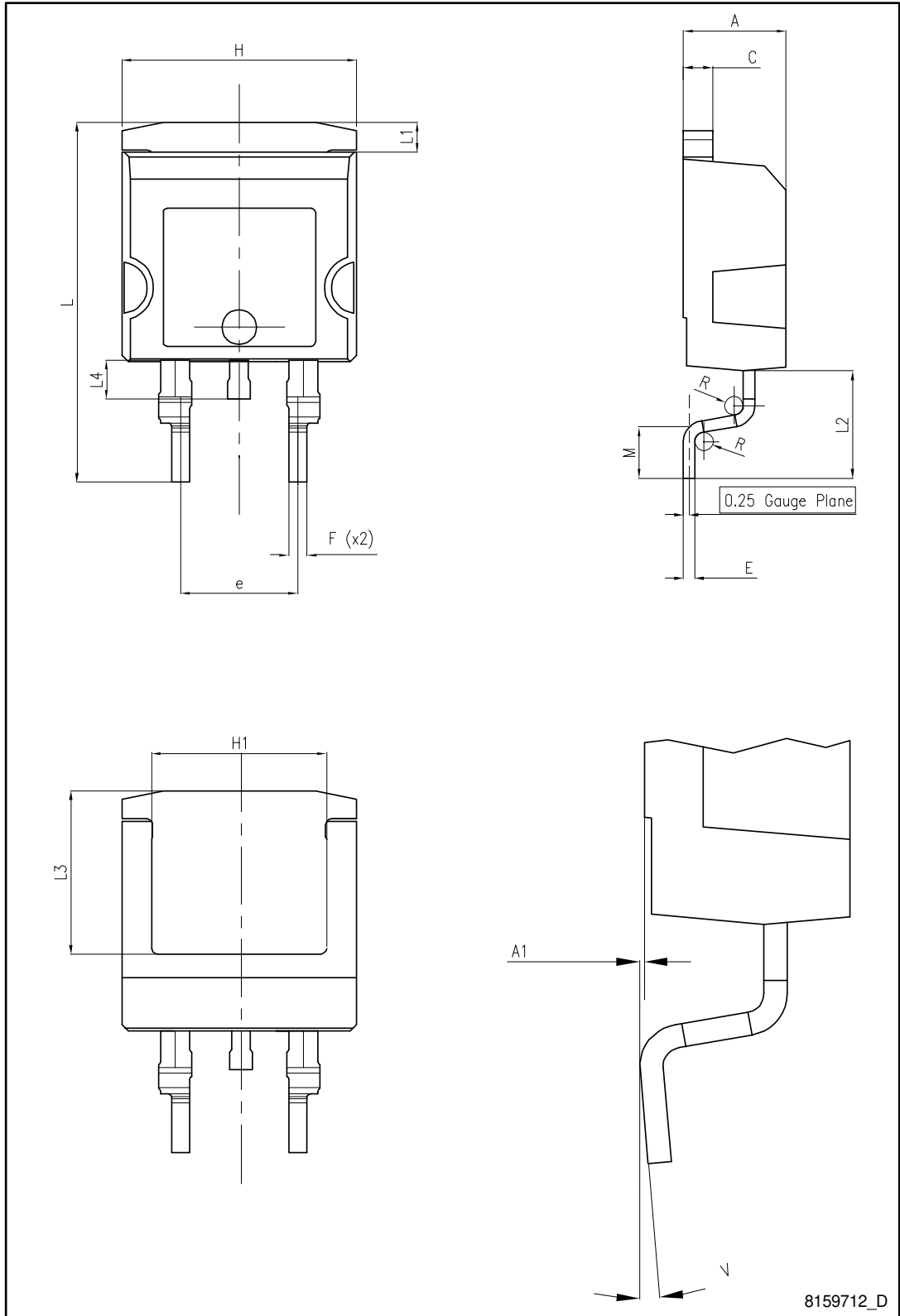
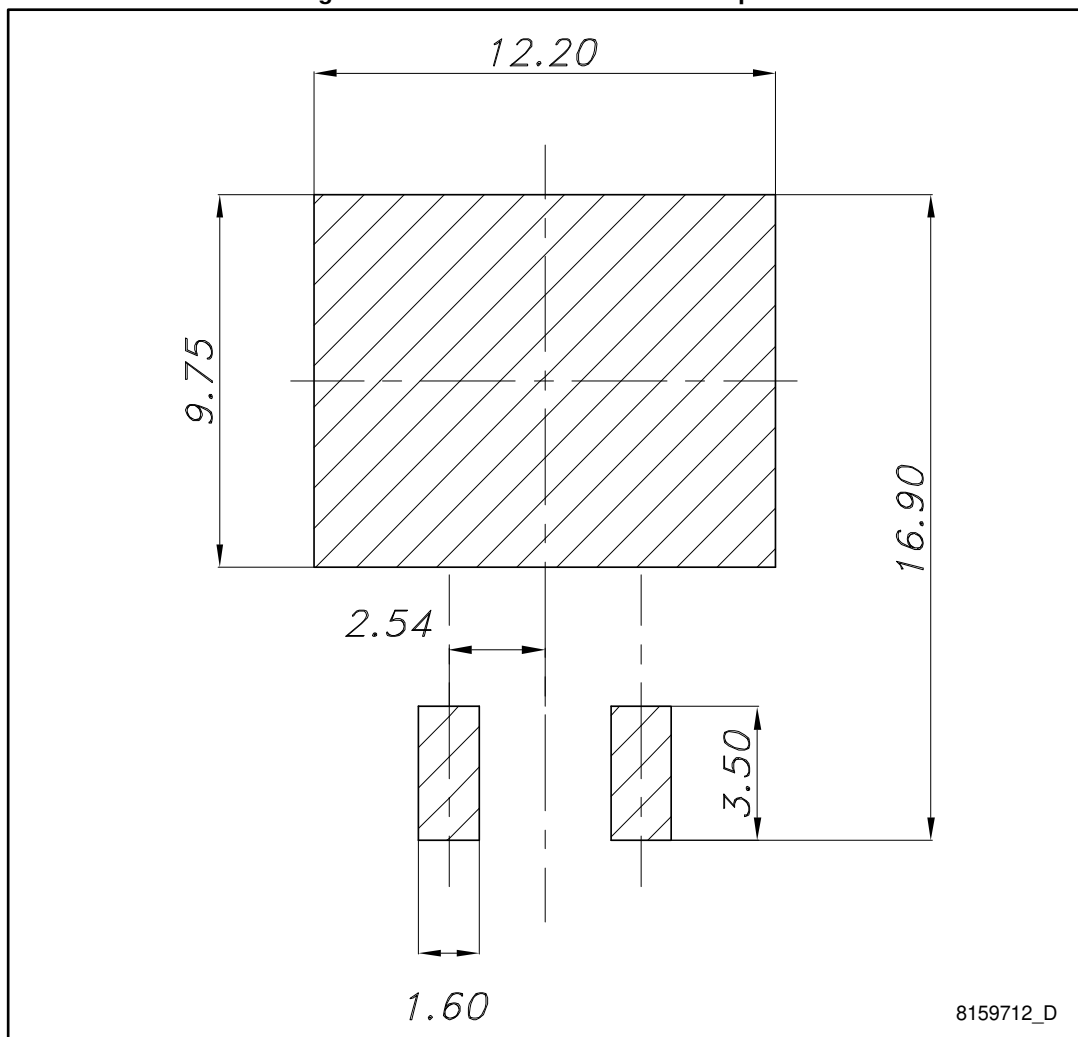


Table 8: H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 20: H²PAK-2 recommended footprint



8159712_D

4.2 H²PAK-6 package information

Figure 21: H²PAK-6 package outline

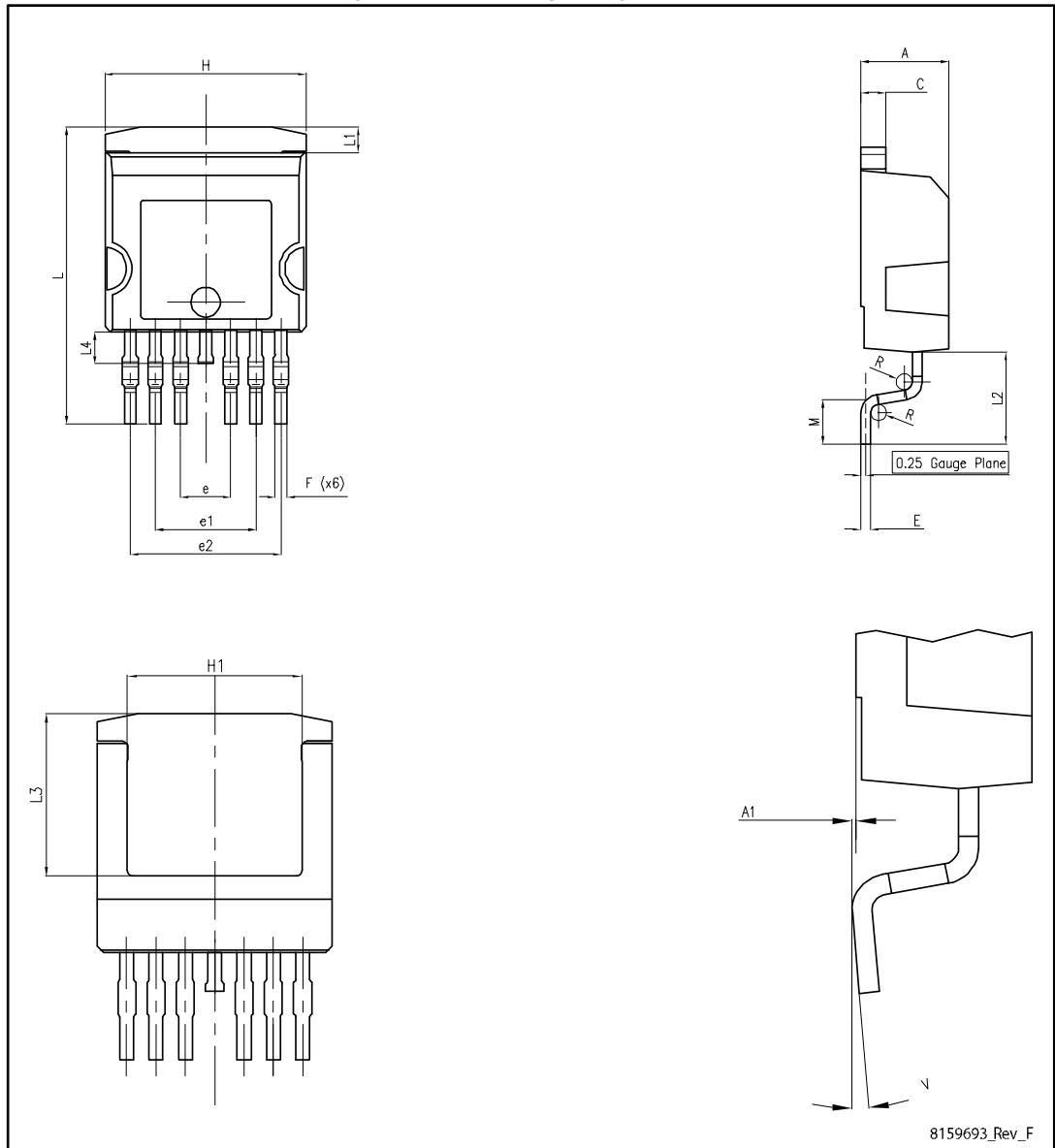
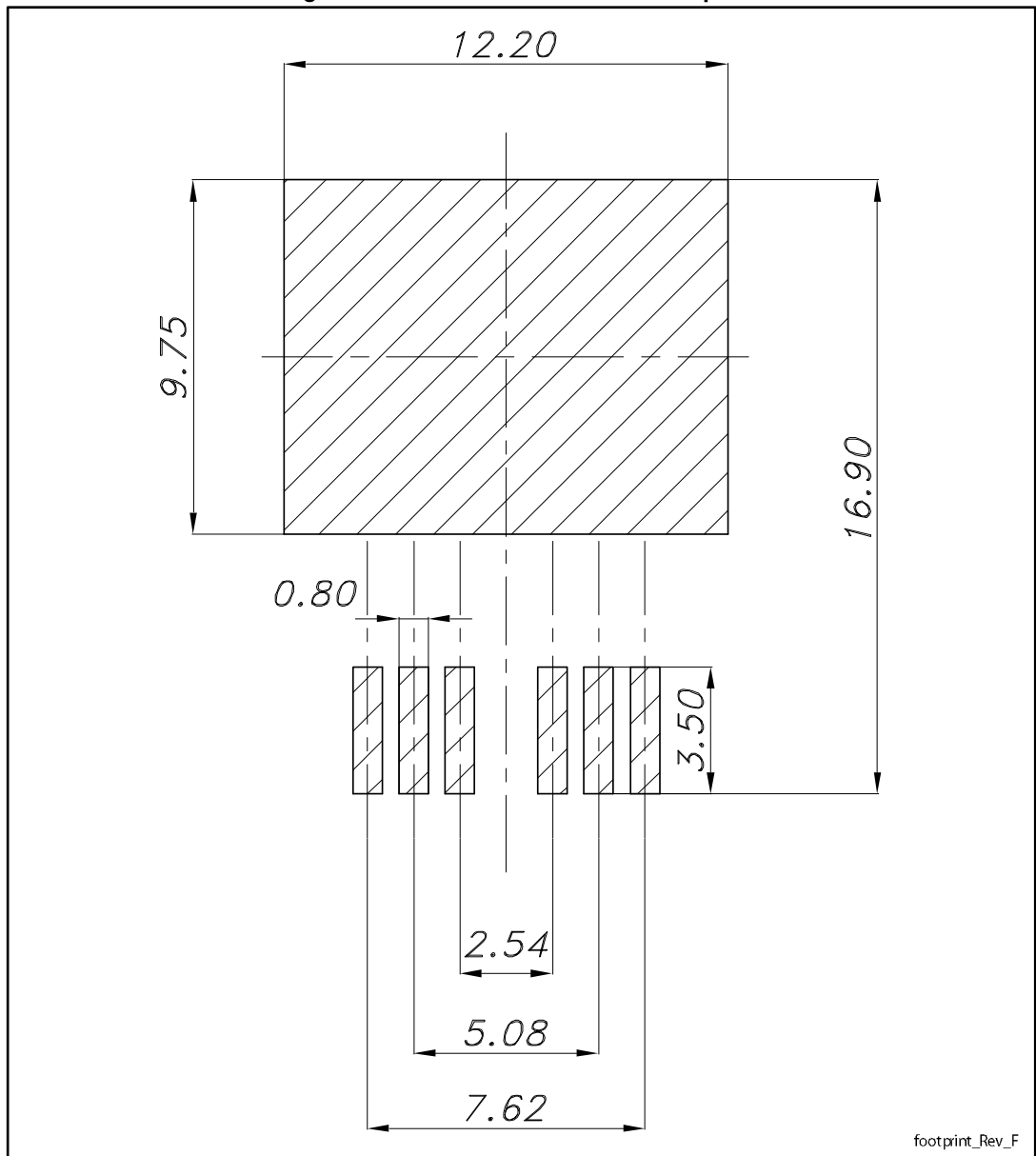


Table 9: H²PAK-6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	2.34		2.74
e1	4.88		5.28
e2	7.42		7.82
E	0.45		0.60
F	0.50		0.70
H	10.00		10.40
H1	7.40		7.80
L	14.75		15.25
L1	1.27		1.40
L2	4.35		4.95
L3	6.85		7.25
L4	1.5		1.75
M	1.90		2.50
R	0.20		0.60
V	0°		8°

Figure 22: H²PAK-6 recommended footprint



Dimensions are in mm.

4.3 H²PAK packing information

Figure 23: Tape outline

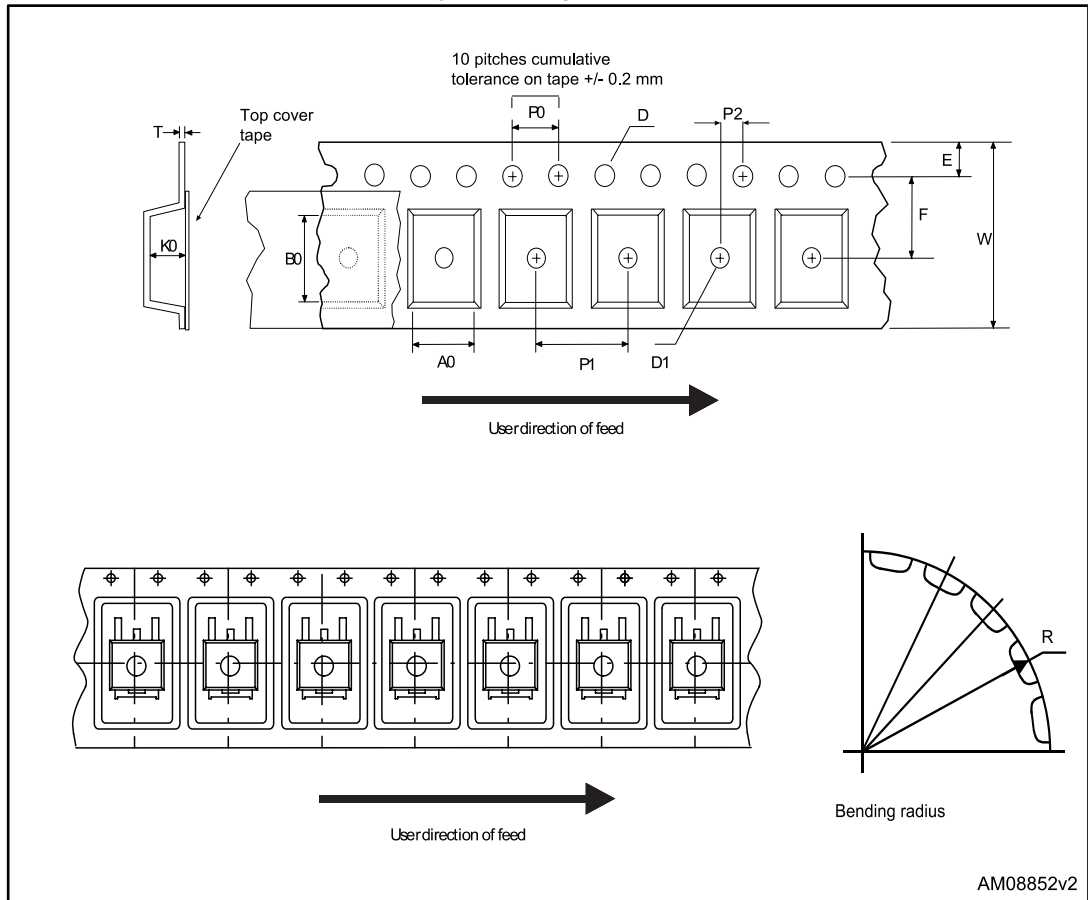


Figure 24: Reel outline

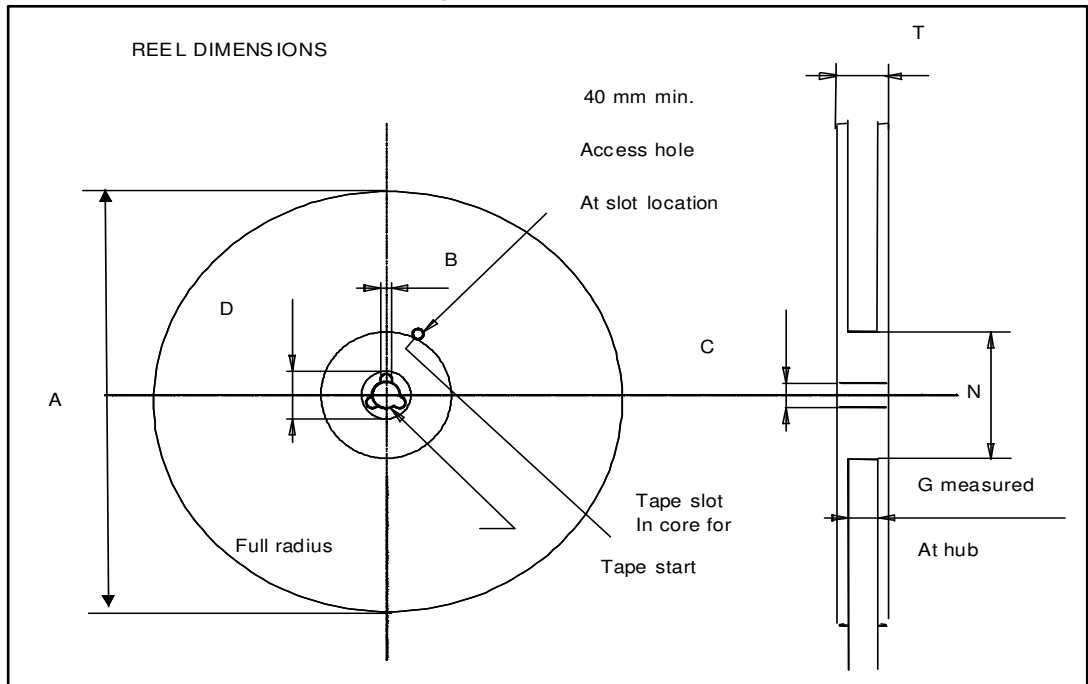


Table 10: Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
10-Apr-2015	1	First release.
13-May-2015	2	Updated Static.
04-Dec-2015	3	Updated note 1 in Table 2: "Absolute maximum ratings", Figure 2: "Safe operating area" and Figure 3: "Thermal impedance".
17-Feb-2016	4	Modified: <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 4: "Static"</i> Modified: <i>Figure 2: "Safe operating area"</i> Minor text changes

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved