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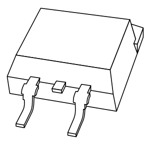


BUK7619-100B

N-channel TrenchMOS standard level FET

Rev. 01 — 10 October 2007 **Product data sheet**

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP High Performance Automotive (HPA) TrenchMOS technology.

1.2 Features

- TrenchMOS technology
- 175 °C rated
- Q101 compliant
- Standard level compatible

1.3 Applications

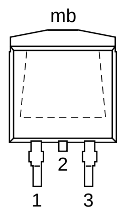
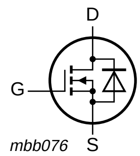
- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V, 24 V and 42 V loads.

1.4 Quick reference data

- $E_{DS(AL)S} \leq 222$ mJ
- $I_D \leq 64$ A
- $R_{DSon} = 17$ mΩ (typ)
- $P_{tot} \leq 200$ W

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	gate (G)	 **SOT404 (D2PAK)**	
2	drain (D)		
3	source (S)		
mb	mounting base; connected to drain (D)		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUK7619-100B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3-leads (one lead cropped)	SOT404

4. Limiting values

Table 3. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	100	V
V_{DGR}	drain-gate voltage (DC)	R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-	±20	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 10 V; see Figure 2 and 3		-	64	A
		T_{sp} = 100 °C; V_{GS} = 10 V; see Figure 2		-	45	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3		-	256	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 1		-	200	W
T_{stg}	storage temperature			–55	+175	°C
T_j	junction temperature			–55	+175	°C
Source-drain diode						
I_{DR}	reverse drain current	T_{mb} = 25 °C		-	64	A
I_{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs		-	256	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 64 A; V_{DS} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting at T_j = 25 °C		-	222	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy		[1]	-	-	mJ

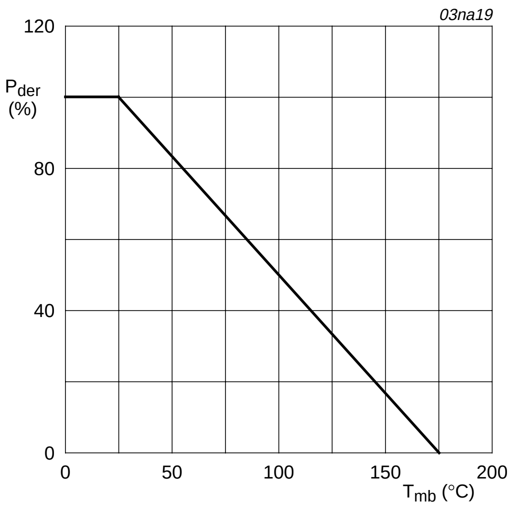
[1] Conditions:

a) Maximum value not quoted. Repetitive rating defined in Figure 16.

b) Single-pulse avalanche rating limited by $T_{j(max)}$ of 175 °C.

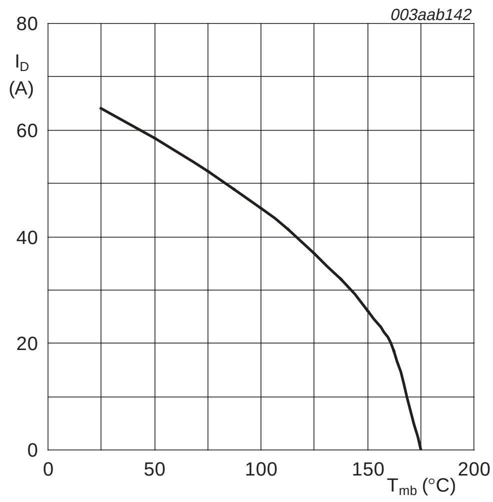
c) Repetitive avalanche rating limited by an average junction temperature of 170 °C.

d) Refer to application note *AN10273* for further information.



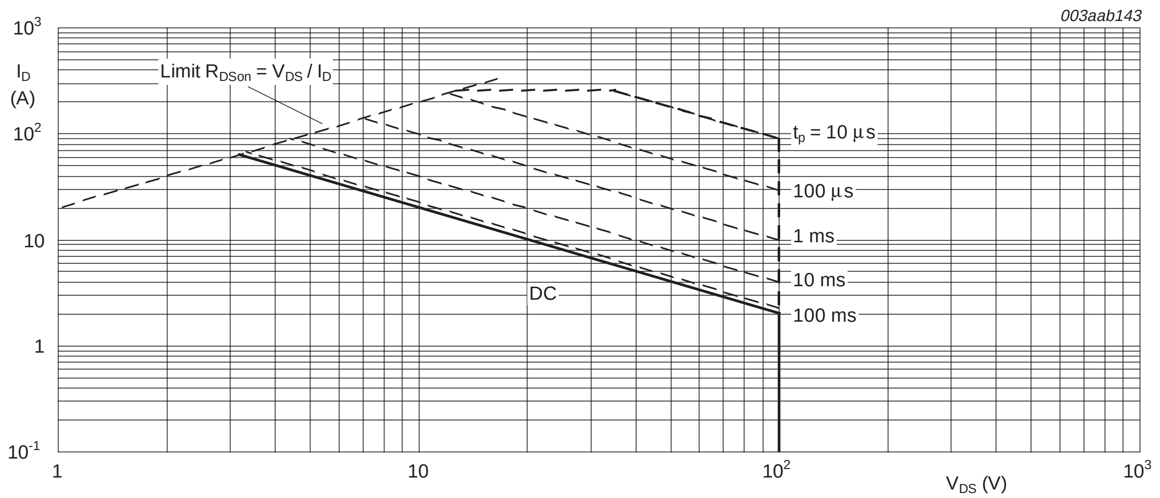
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10$ V

Fig 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	0.74	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W

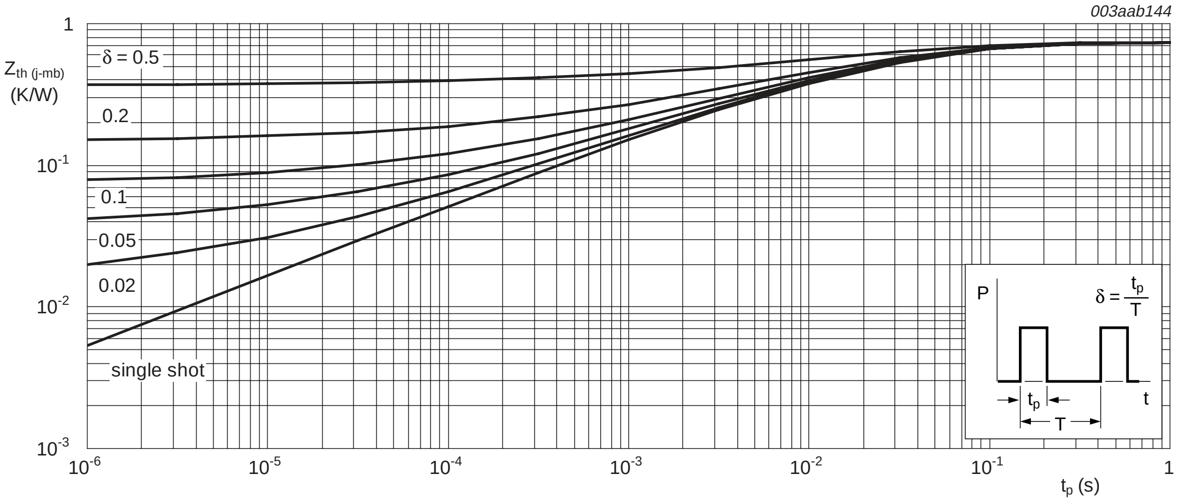


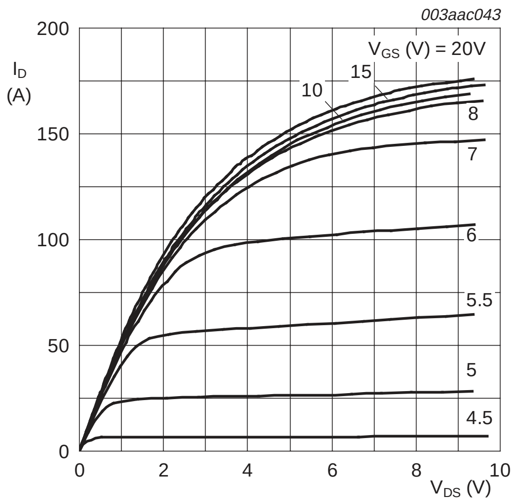
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

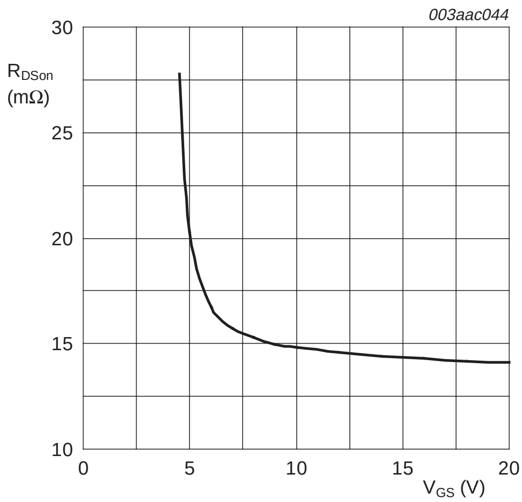
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	100	-	-	V
		T_j = –55 °C	89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9 and10				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	-	-	V
		T_j = –55 °C	-	-	4.4	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.02	1	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; see Figure 7 and 8				
		T_j = 25 °C	-	17	19	mΩ
		T_j = 175 °C	-	-	49	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DD} = 80 V; V_{GS} = 10 V; see Figure 14	-	53	-	nC
Q_{GS}	gate-source charge		-	11	-	nC
Q_{GD}	gate-drain charge		-	27	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; see Figure 12	-	2555	3400	pF
C_{oss}	output capacitance		-	340	480	pF
C_{rss}	reverse transfer capacitance		-	84	115	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	19	-	ns
t_r	rise time		-	45	-	ns
$t_{d(off)}$	turn-off delay time		-	85	-	ns
t_f	fall time		-	34	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; see Figure 15	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	116	-	ns
Q_r	recovered charge		-	130	-	nC



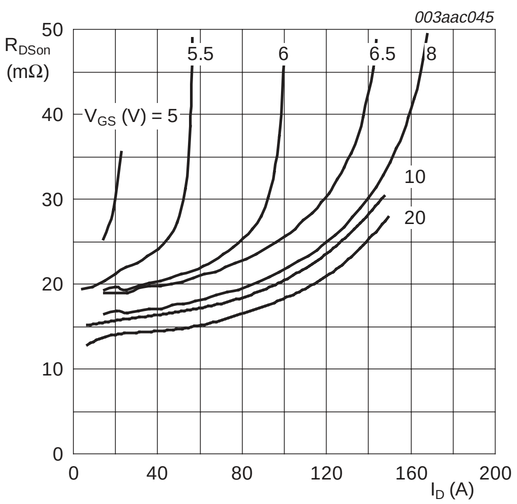
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



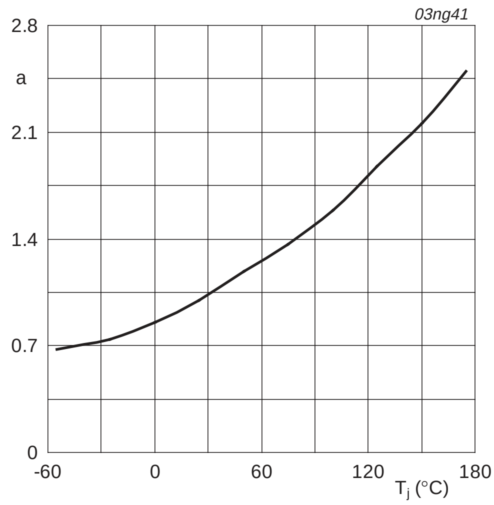
T_j = 25 °C; I_D = 10 A

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



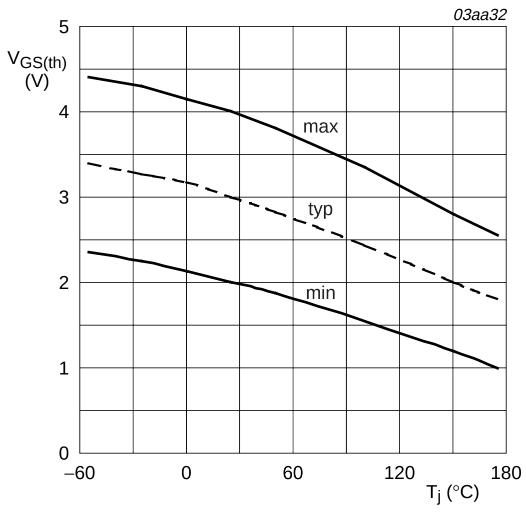
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values



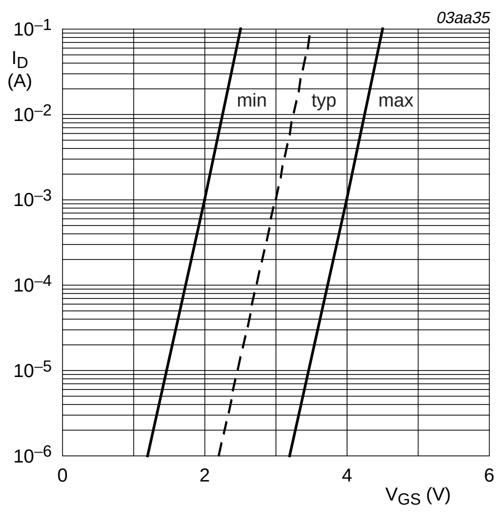
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



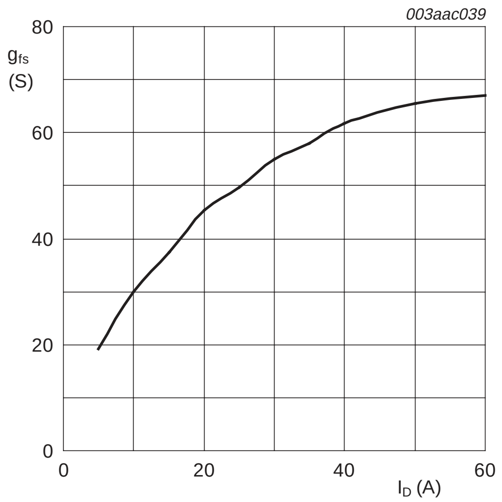
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature



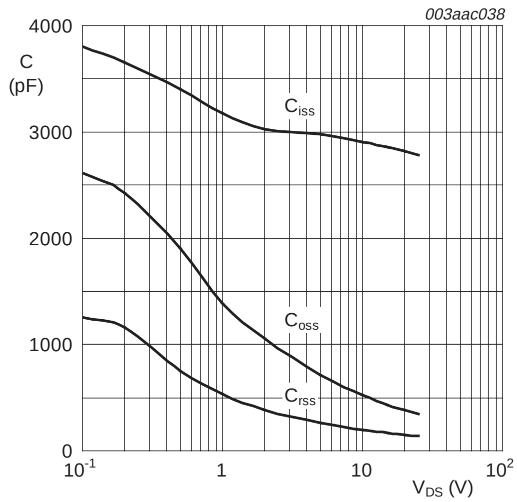
T_j = 25 °C; V_{DS} = V_{GS}

Fig 10. Sub-threshold drain current as a function of gate-source voltage



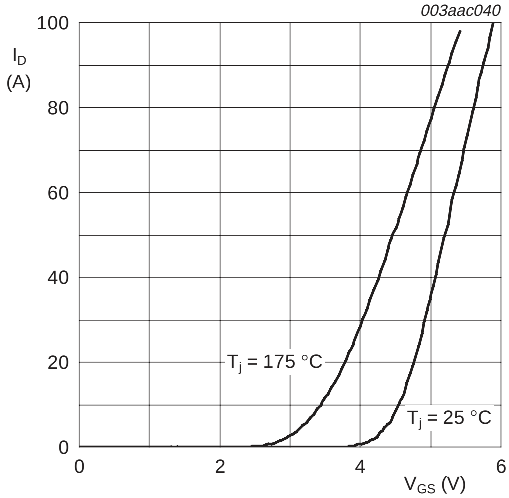
T_j = 25 °C; V_{DS} = 25 V

Fig 11. Forward transconductance as a function of drain current; typical values



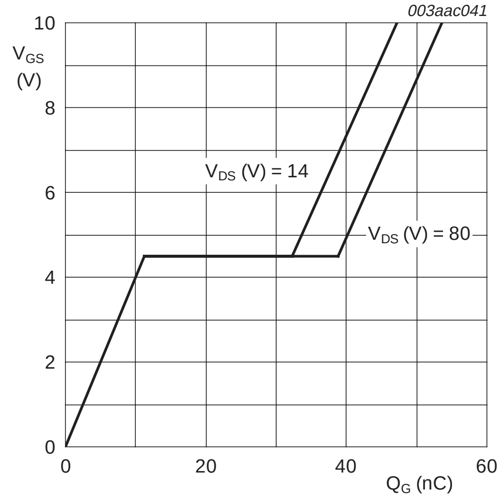
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



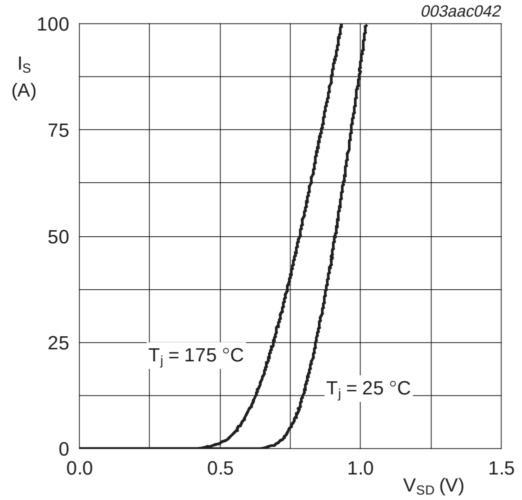
V_{DS} = 25 V

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



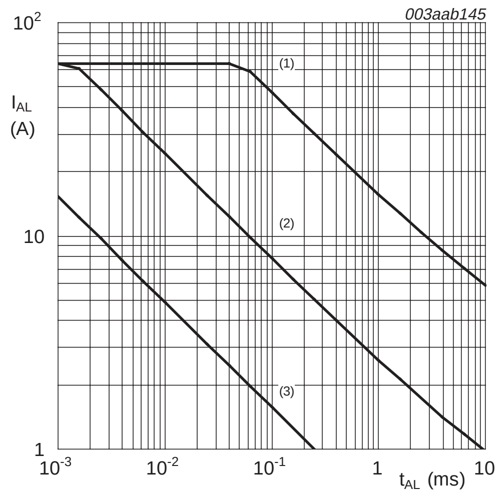
T_j = 25 °C; I_D = 25 A

Fig 14. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V

Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



See Table note 1 of Table 3 Limiting values.

(1) Single-pulse; T_j = 25 °C.

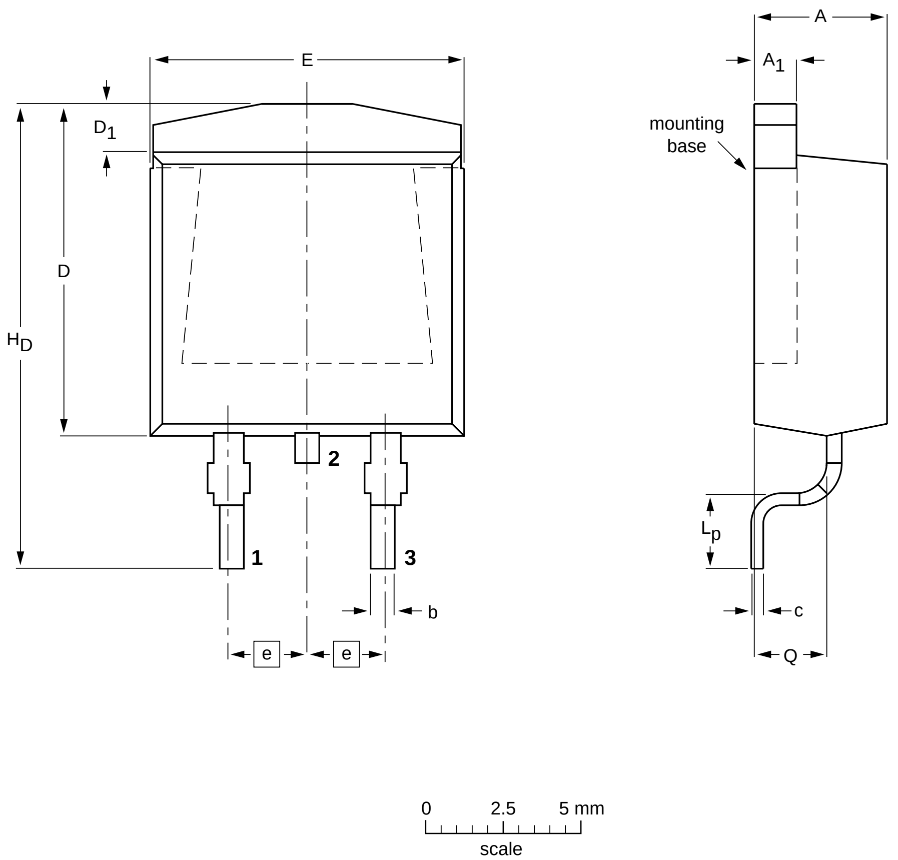
(2) Single-pulse; T_j = 125 °C.

(3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

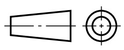
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 17. Package outline SOT404 (D2PAK)

8. Soldering

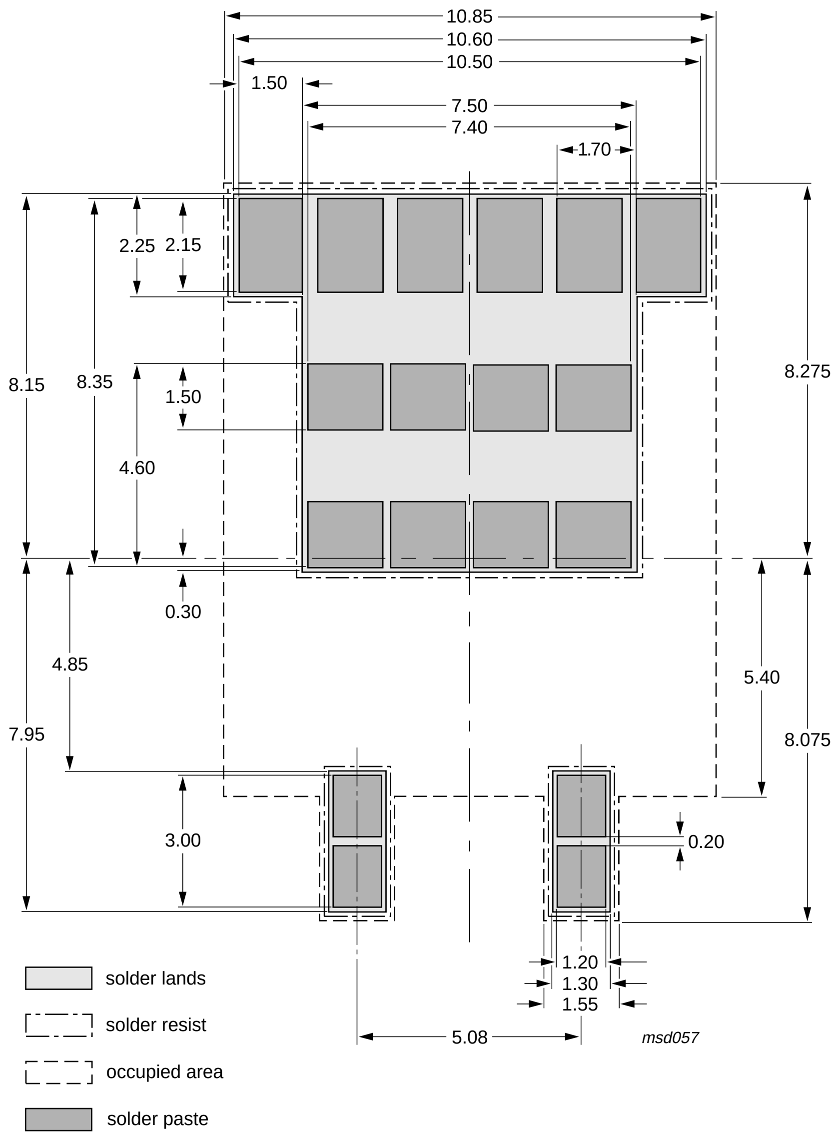


Fig 18. Reflow soldering footprint for SOT404

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK7619-100B_1	20071010	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

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