



Advanced
Micro
Devices

Am29863

High Performance Bus Transceiver

DISTINCTIVE CHARACTERISTICS

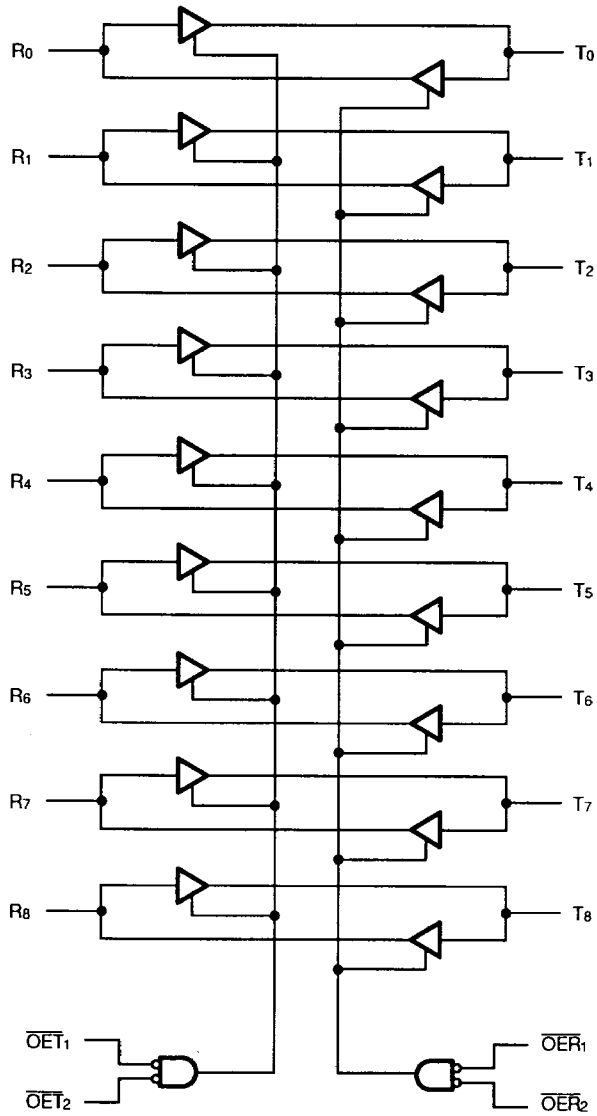
- **High-speed symmetrical bidirectional transceiver**
 - Noninverting $t_{PD} = 5.0$ ns typ
 - Inverting $t_{PD} = 4.5$ ns typ
- **200 mV minimum input hysteresis on input data ports**
- **Three-state outputs glitch-free during power-up and -down**
- **Outputs have Schottky clamp to ground**
- **48 mA commercial I_{OL}**
- **Low input/output capacitance**
- **I_{OH} specified 2.0 V and 2.4 V**
- **24-pin 0.3" space saving package**
- **Fully TTL compatible inputs and outputs**
- **IMOX™ high performance IMplanted OXide isolated process**

GENERAL DESCRIPTION

The Am29863 bus transceiver provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The Am29863 is a 9-bit transceiver with NOR-ed output enables for maximum control flexibility. All transceiver data inputs have 200 mV minimum input hysteresis to provide improved noise rejection.

All of the Am29800 high performance interface family are designed for high capacitance load drive capability while providing low capacitance bus loading at both inputs and outputs. All inputs are Schottky diode inputs, and all outputs are designed for low capacitance bus loading in the high impedance state.

BLOCK DIAGRAM

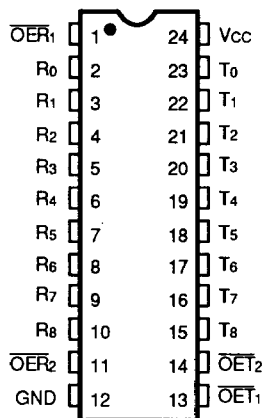


03369-001A

CONNECTION DIAGRAM

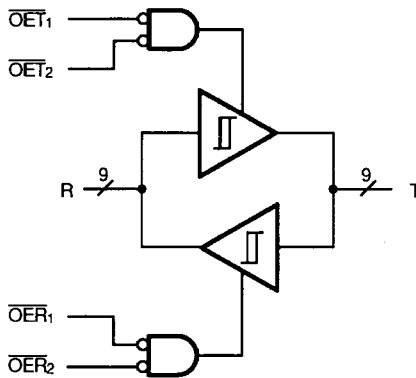
Top View

DIP



03369-002A

LOGIC SYMBOL



9-Bit Transceiver

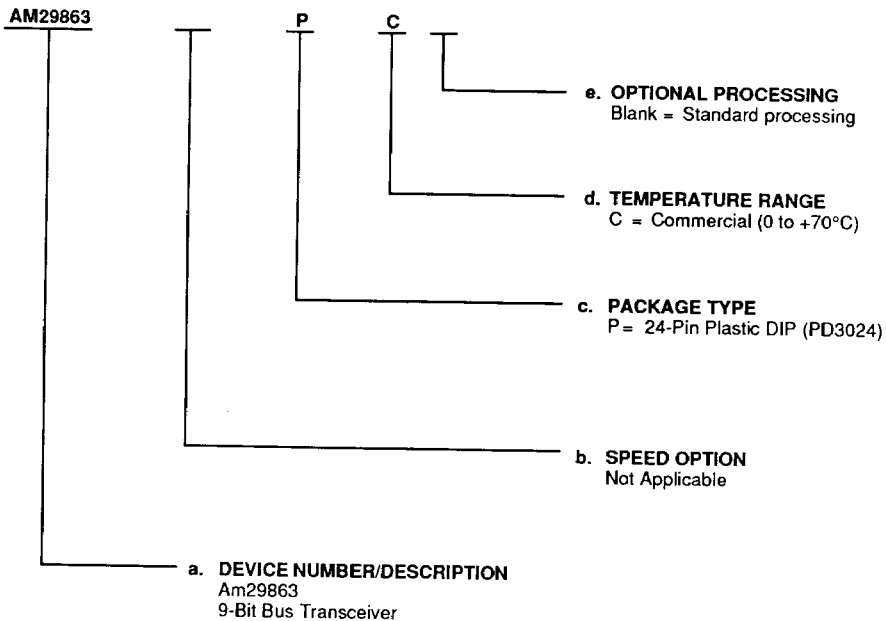
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM29863	PC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION \overline{OER}_i

When both are LOW in conjunction with any \overline{OET}_i HIGH indicates the RECEIVE mode.

 R_i

9-bit RECEIVE input/output.

 \overline{OET}_i

When both are LOW in conjunction with any \overline{OER}_i HIGH indicates the TRANSMIT mode.

 T_i

9-bit TRANSMIT input/output.

FUNCTION TABLE

Inputs						Outputs		Function
\overline{OET}_1	\overline{OET}_2	\overline{OER}_1	\overline{OER}_2	R_i	T_i	R_i	T_i	
L	L	H	X	L	N/A	N/A	L	Transmit
L	L	X	H	L	N/A	N/A	L	Transmit
H	X	L	L	N/A	L	L	N/A	Receive
X	H	L	L	N/A	L	L	N/A	Receive
L	L	H	X	H	N/A	N/A	H	Transmit
L	L	X	H	H	N/A	N/A	H	Transmit
H	X	L	L	N/A	H	H	N/A	Receive
X	H	L	L	N/A	H	H	N/A	Receive
H	X	H	X	X	X	Z	Z	Hi-Z
X	H	X	H	X	X	Z	Z	Hi-Z

H = HIGH

L = LOW

Z = High Impedance

X = Don't Care

N/A = Not Applicable

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7.0 V
DC Voltage Applied to Output for High Output State	-0.5 V to +5.5 V
DC Input Voltage	-0.5 V to +5.5 V
DC Output Current, Into Outputs	100 mA
DC Input Current	-30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T _A)	0 to +70°C
Supply Voltage (V _{CC})	5.0 V ± 10% +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 4.5 V V _{IN} = V _{IH} or V _{IL}	I _{OH} = -15 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = 4.5 V V _{IN} = V _{IH} or V _{IL}	I _{OL} = 48 mA	2.0	0.5	V
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		V
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	V
V _I	Input Clamp Voltage	V _{CC} = 4.5 V, I _{IN} = -18 mA			-1.2	V
V _{HYST}	Input Hysteresis	Tested output is connected to AC load test circuit		200		mV
I _{IL}	Input LOW Current	V _{CC} = 5.5 V, V _{IN} = 0.4 V			-1.0	mA
I _{IH}	Input HIGH Current	V _{CC} = 5.5 V, V _{IN} = 2.7 V			50	μA
I _I	Input HIGH Current	V _{CC} = 5.5 V, V _{IN} = 5.5 V			1.0	mA
I _{OZH}	Output Off-State Output Current (Hi-Z)	V _{CC} = 5.5 V, V _O = 2.4 V			50	μA
I _{OZL}	Output Off-State Output Current (Hi-Z)	V _{CC} = 5.5 V, V _O = 0.4 V			-1.0	mA
I _{SC}	Output Short Circuit Current	V _{CC} = 5.5 V		-75	-250	mA
I _{CC}	Supply Current	V _{CC} = 5.5 V Outputs Open	Over Temperature Range		160	mA
			+70°C		150	

SWITCHING CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$)

Parameter Symbol	Parameter Description	Test Conditions*	Min.	Typ.	Max.	Unit
t _{PLH}	Propagation Delay from R _i to T _i or T _i to R _i	C _L = 50 pF		4.8	6.0	ns
t _{PHL}				5.2	6.2	ns
t _{PLH}		C _L = 300 pF		8	11	ns
t _{PHL}				11	14	ns
t _{ZH}	Output Enable Time $\overline{\text{OET}}$ to T _i and $\overline{\text{OER}}$ to R _i	C _L = 50 pF		6.5	12	ns
t _{ZL}				9.5	12	ns
t _{ZH}		C _L = 300 pF		11	17	ns
t _{ZL}				17	21	ns
t _{HZ}	Output Disable Time $\overline{\text{OET}}$ to T _i and $\overline{\text{OER}}$ to R _i	C _L = 5 pF		3.5	8.0	ns
t _{LZ}				3.5	8.0	ns
t _{HZ}		C _L = 50 pF		11.2	16	ns
t _{LZ}				4.5	9.0	ns

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

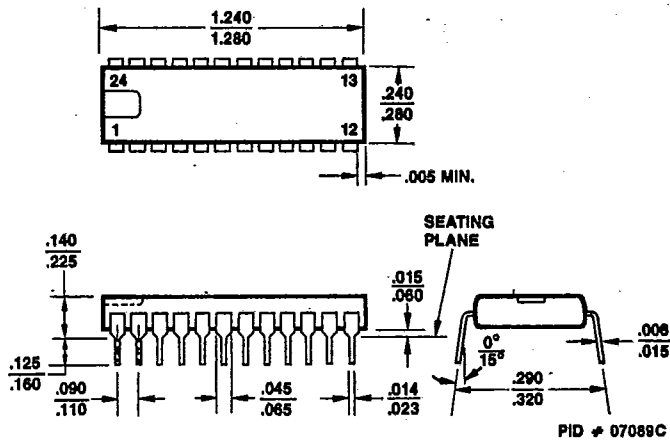
Parameter Symbol	Parameter Description	Test Conditions*	Min.	Max.	Unit
t _{PLH}	Propagation Delay from R _i to T _i or T _i to R _i	C _L = 50 pF		8	ns
t _{PHL}				8	ns
t _{PLH}		C _L = 300 pF		15	ns
t _{PHL}				15	ns
t _{ZH}	Output Enable Time $\overline{\text{OET}}$ to T _i or $\overline{\text{OER}}$ to R _i	C _L = 50 pF		15	ns
t _{ZL}				15	ns
t _{ZH}		C _L = 300 pF		20	ns
t _{ZL}				23	ns
t _{HZ}	Output Disable Time $\overline{\text{OET}}$ to T _i or $\overline{\text{OER}}$ to R _i	C _L = 5 pF		9	ns
t _{LZ}				9	ns
t _{HZ}		C _L = 50 pF		17	ns
t _{LZ}				12	ns

*See Test Circuit and Waveforms (Chapter 2).

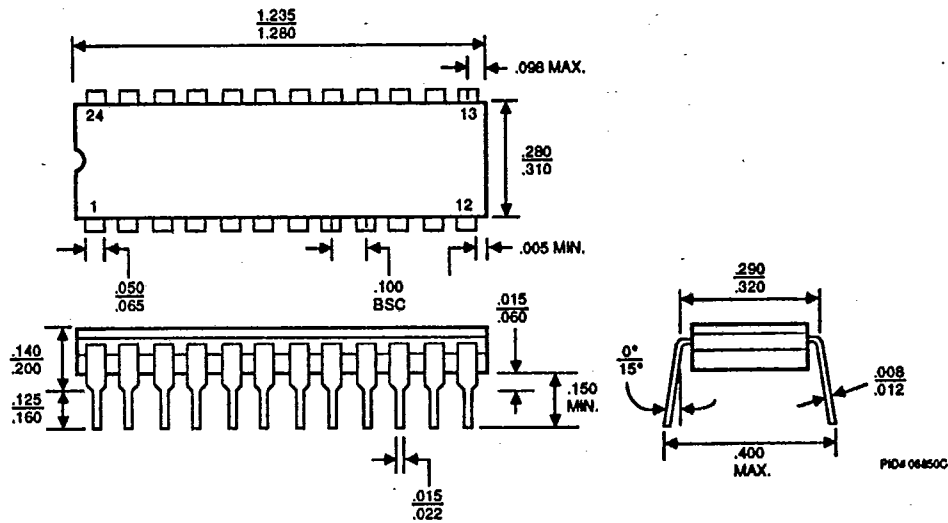
PACKAGE OUTLINES*

T-90-20

PD3024



CD3024

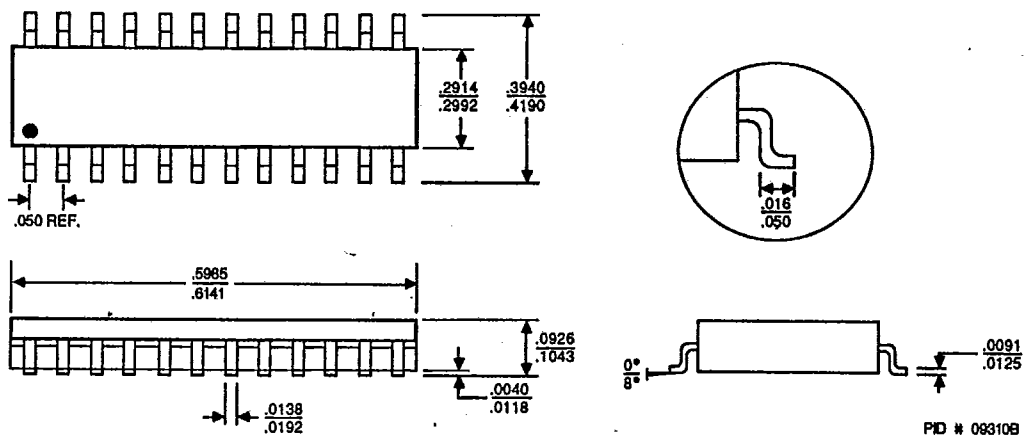


*For reference only.

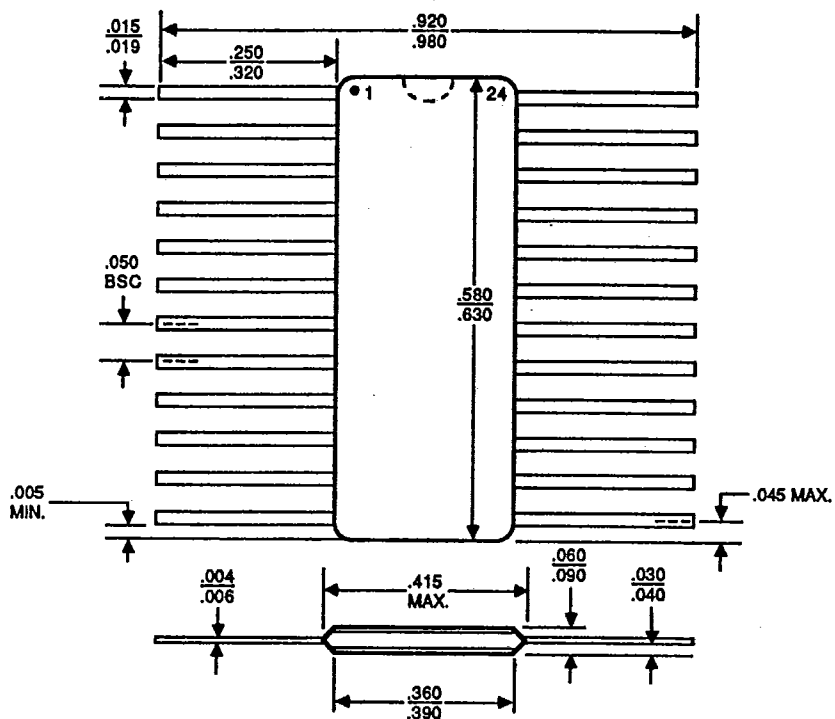
PACKAGE OUTLINES (Cont'd.)

T-90-20

SO 024



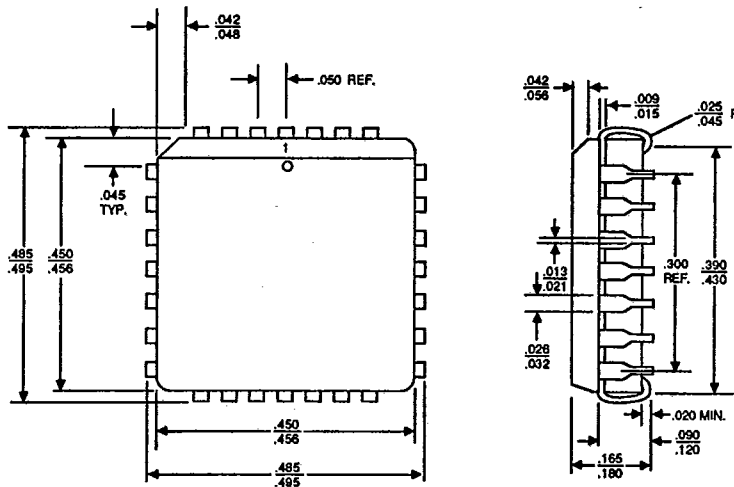
CFM024



PACKAGE OUTLINES (Cont'd.)

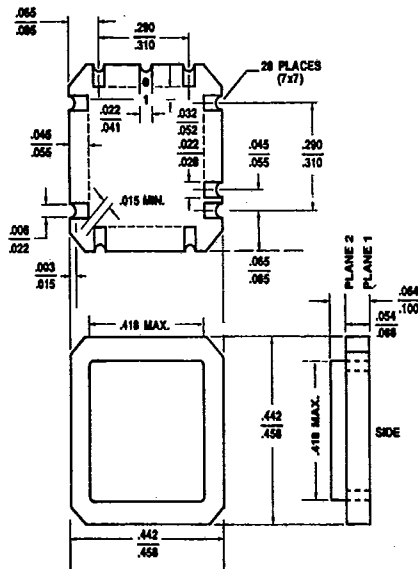
T-90-20

PL 028



PID # 06751E

CL 028



PID # 06595D

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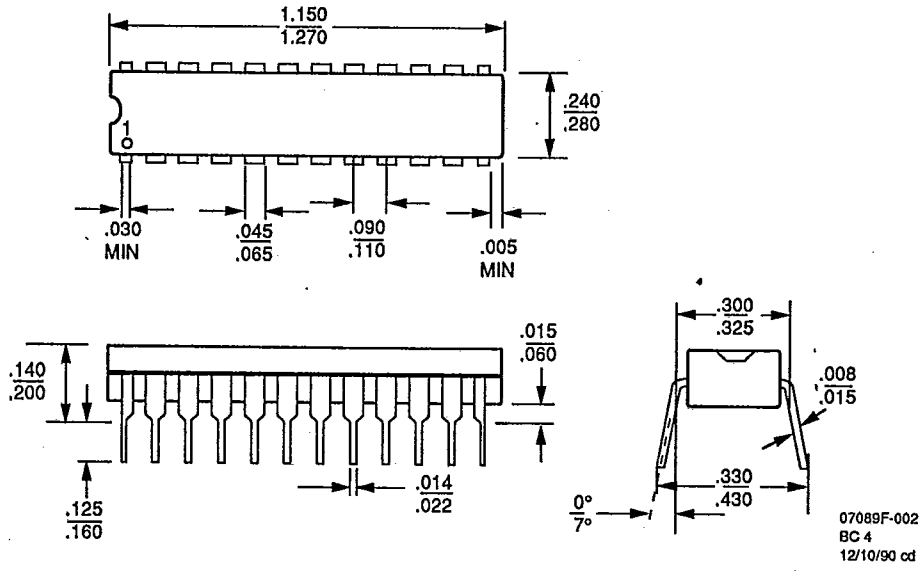


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PD3024
24-Pin 300-mil Plastic SKINNYDIP

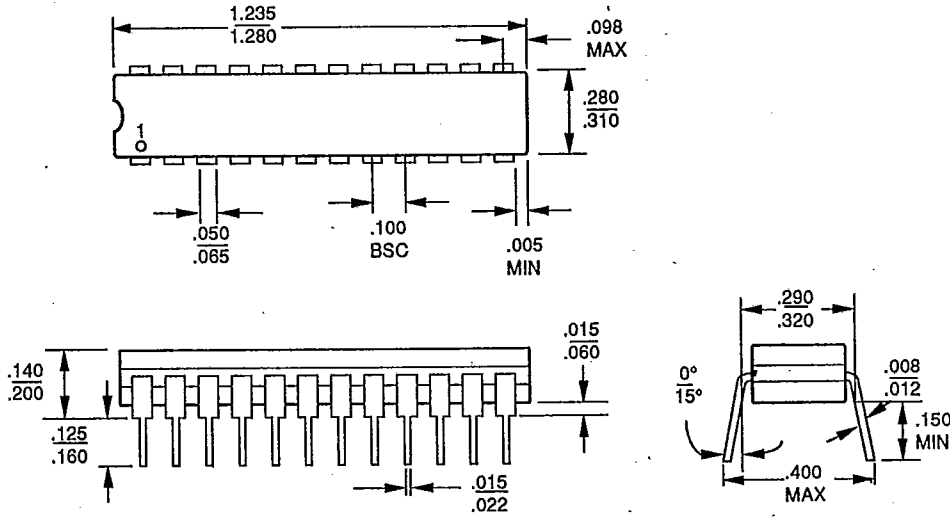
T-90-20



Note:
For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

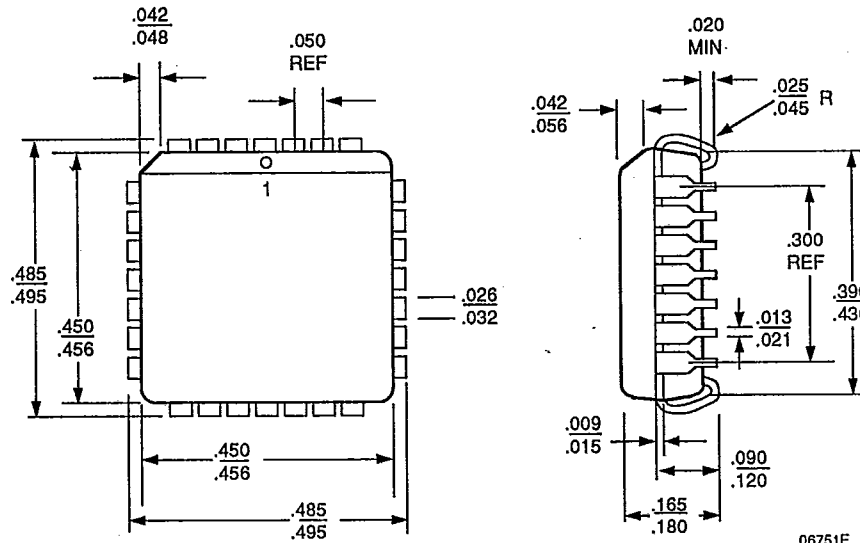
T-90-20

CD3024
24-Pin 300-mil Ceramic SKINNYDIP



06850C

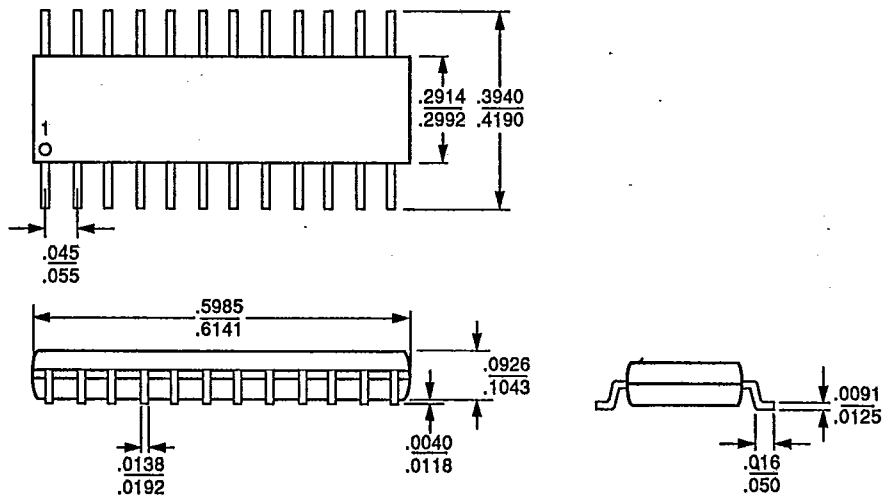
PL 028
28-Pin Plastic Leaded Chip Carrier



06751E

SO 024
24-Pin Plastic Small Outline Package

T-90-20



09310B