Title	***Reference Design Report for a 17 W Dual Output Flyback Converter for LCD Monitor Using LinkSwitch™-HP LNK6774V***
Specification	90 VAC – 265 VAC Input; 5 V, 1 A and 18 V, 670 mA Output
Application	LCD Monitor
Author	Applications Engineering Department
Document Number	RDR-321
Date	September 28, 2012
Revision	2.2

Summary and Features

- Primary-side regulated isolated flyback converter with ±5% regulation
- 132 kHz switching frequency for small transformer and output filter size
- Full load continuous conduction mode operation for improved efficiency and reduced output capacitor ripple currents
- Multimode operation maximizes efficiency over full load range
- Below 100 mW input power with 50 mW standby load at 230 VAC
- Extensive protection features including OVP, OTP, brown-in/out, line overvoltage, and lost-regulation (auto-restart)
- Meets EN-550022 and CISPR-22 Class B conducted EMI
- Meets IEC61000-4-5 1 kV / 2 kV surge

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This report describes a universal input, 5 V/1000 mA and 18 V/670 mA isolated flyback converter employing LNK6774V from the LinkSwitch-HP family of ICs. It contains the complete specification of the power supply, a detailed circuit diagram, the entire bill of materials required to build the supply, extensive documentation of the power transformer, along with test data and waveform plots of the most important electrical waveforms.

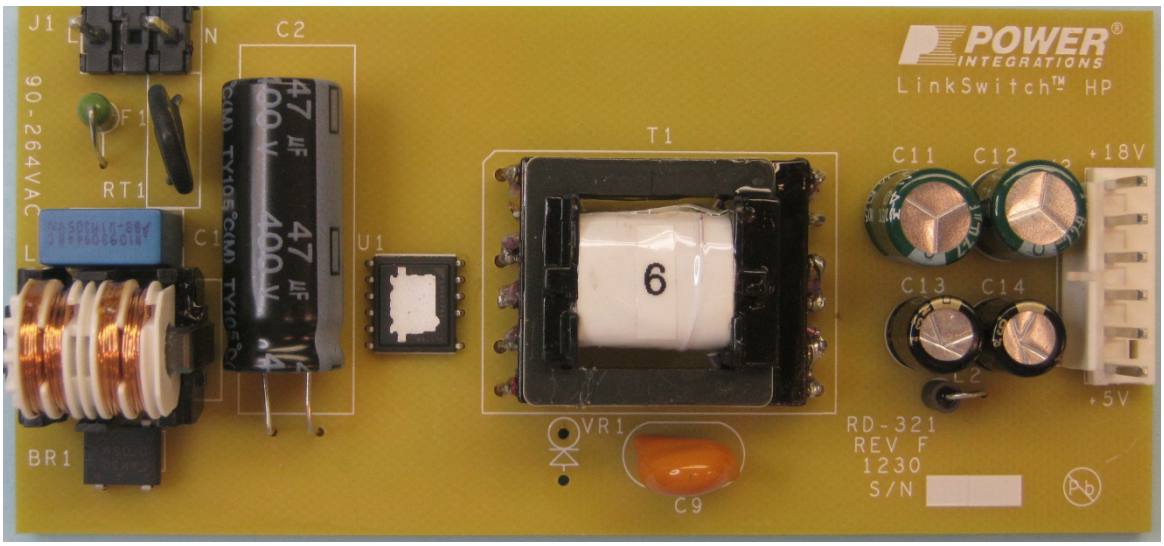

Figure 1 – Prototype Top View.

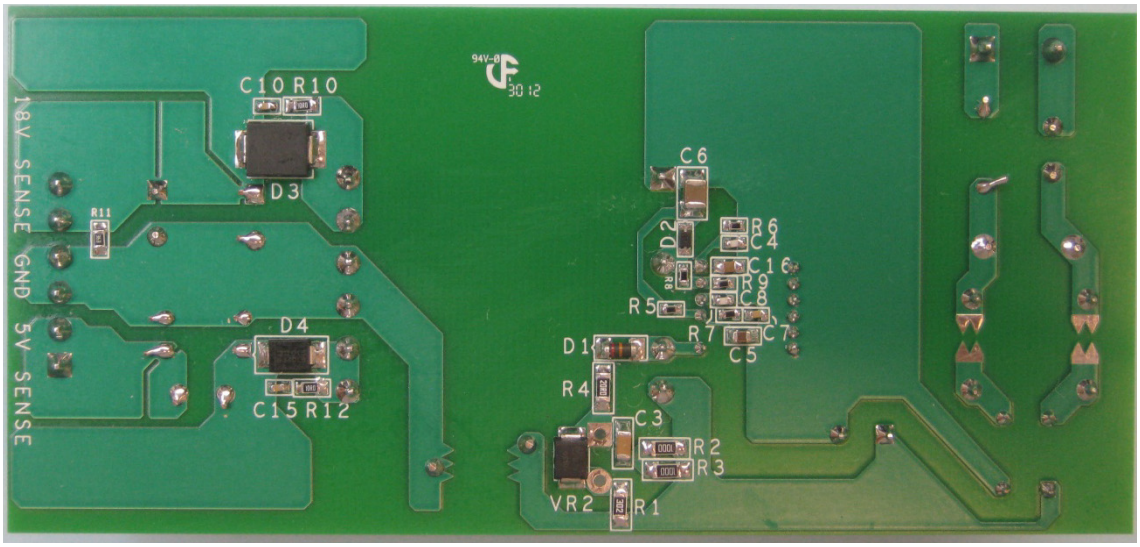

Figure 2 – Prototype Bottom View.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
Input Power at Standby				100	mW	230 VAC, 5 V 0.01 A, 18 V no-load
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	
Output Ripple Voltage 1	$V_{RIPPLE1}$			100	mVpp	20 MHz bandwidth with steady-state load
Output Current 1	I_{OUT1}	0.01		1500	mA	See load profile below
Output Voltage Transient 1	$V_{TRANSIENT1}$	4.75		5.5	V	See load profile below
Output Voltage 2	V_{OUT2}	16.2	18	26	V	
Output Ripple Voltage 2	$V_{RIPPLE2}$				mV	20 MHz bandwidth
Output Current 2	I_{OUT2}	0		670	mA	See load profile below
Output Voltage Transient 2	$V_{TRANSIENT2}$	16.2		28	V	See load profile below
Total Output Power						
Continuous Output Power	P_{OUT}	0.05		17.1	W	
Efficiency						
Full Load efficiency	η	80			%	90 VAC and Full Load
Environmental						
Conducted EMI		Meets CISPR22B / EN55015B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge	DM	1			kV	1.2/50 μs surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω Common Mode: 12 Ω
	CM	2				
ESD	**Air**	-15		15	kV	Air discharge onto output connector
	Contact	-6		6	kV	Contact discharge onto output connector
Ambient Temperature	T_{AMB}	0		40	°C	Free convection, sea level

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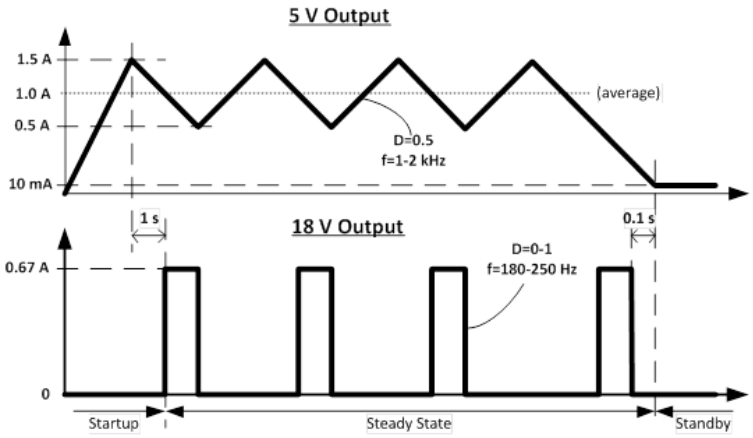

Figure 3 – Typical LCD Monitor Load Profile.

3 Schematic

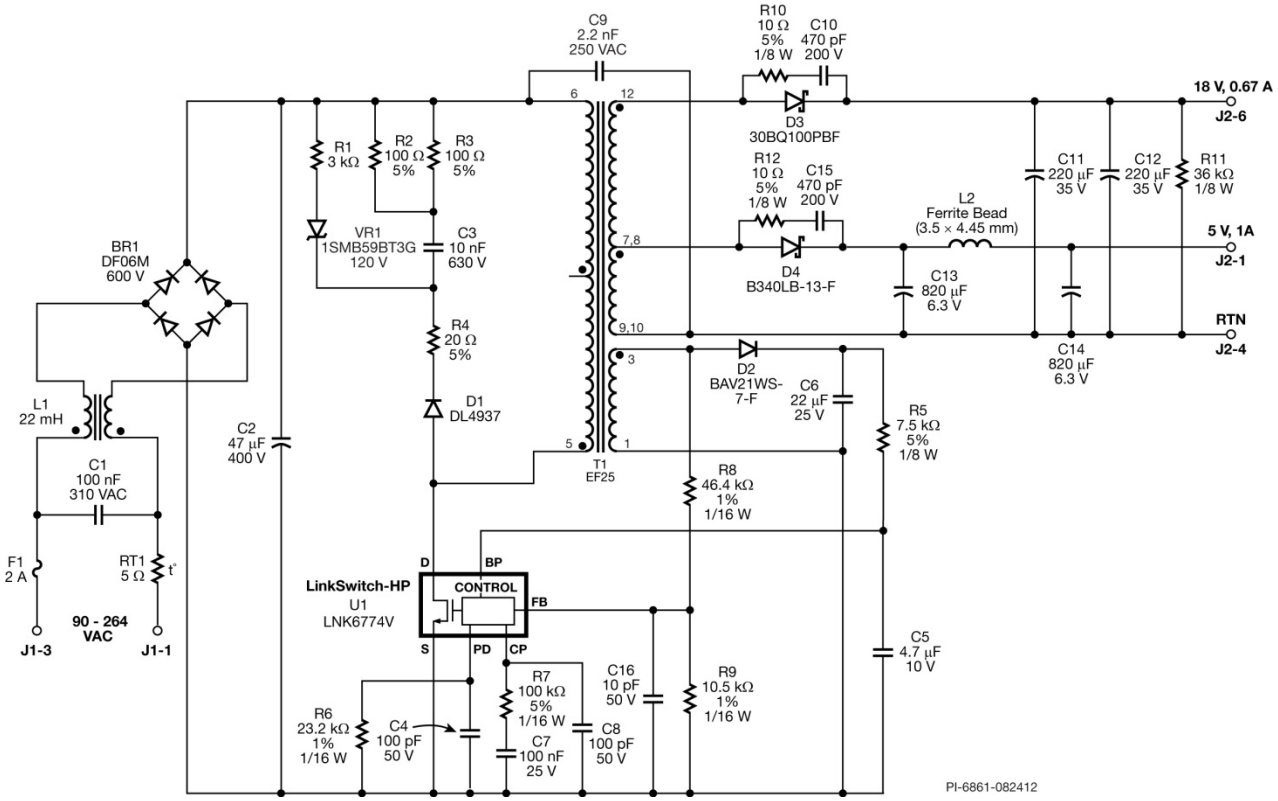

Figure 4 – Circuit Schematic.

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4 Circuit Description

4.1 Input Rectification and Filtering

Bridge rectifier BR1 rectifies the AC input which is filtered by C2. Inductor L1, C1 and C2 are used to attenuate differential mode and common mode conducted EMI. Shielding techniques (*E-Shield*™) were used in the construction of transformer T1 to reduce common mode EMI displacement currents. This filter arrangement, the proprietary E-Shield techniques together with the IC's frequency jitter function provide excellent EMI performance for this solution with a Y capacitor and a primary-side RCD clamp circuit.

4.2 LinkSwitch-HP Primary

The LNK6774V device (U1) integrates an oscillator, an error amplifier and multi-mode control circuit, startup and protection circuitry and a high-voltage power MOSFET all on one monolithic IC.

One side of the power transformer is connected to the high-voltage bus and the other side is connected to the DRAIN pin of U1. At the start of a switching cycle, the controller turns the power MOSFET on and current ramps up in the primary winding, which stores energy in the core of the transformer. When that current reaches the limit threshold which is set by the output of internal error amplifier (CP pin voltage), the controller turns the power MOSFET off. Due to the phasing of the transformer windings and the orientation of the output diode, the stored energy then induces a voltage across the secondary winding, which forward biases the output diode, and the stored energy is delivered to the output capacitor.

Capacitor C5 (4.7 μF) connected to the BP pin sets overvoltage protection (OVP), lost regulation protection (auto-restart), and over-temperature protection (OTP) to automatic restart attempts after a given off-period (typ. 1500 ms). Other combinations including latching OTP and OVP can be programmed with different capacitor values. Refer to LinkSwitch-HP data sheet for further details.

4.3 Primary RCD Clamp

Diode D1, VR1, C3, R1, R2, R3 and R4 form a RCD snubber that is used to limit the voltage stress across the LinkSwitch-HP. Peak drain voltage is therefore limited to typically less than 580 V at 265 VAC – providing significant margin to the 725 V drain voltage (BV_{DSS}). Zener VR1 prevents the capacitor C3 from fully discharging every switching cycle to reduce power consumption during standby operation.

Diode D1, R2, VR1, C3, R5 and R6 form a RCD snubber that is used to limit the voltage stress across the LinkSwitch-HP. Peak drain voltage is therefore limited to typically less than 580 V at 265 VAC – providing significant margin to the 700 V drain voltage (BV_{DSS}).

4.4 Output Rectification

Output rectification of 18 V output is provided by diode D3 and filtering is provided by capacitor C11 and C12. The snubber formed by R10 and C10 provides high frequency filtering for improved EMI. Output rectification of 5 V output is provided by diode D4 and filtering is provided by capacitor C13 and C14 and inductor L2. The snubber formed by R12 and C15 provides high frequency filtering for improved EMI.

4.5 External Current Limit Setting

The maximum cycle-by-cycle current limit is set by the resistor R6 connected to PD pin. A 23.2 kΩ resistor in the design sets the maximum current limit to 60% of the LNK6774V's default current limit.

4.6 Feedback and Compensation Network

The output voltage is sensed through bias winding and resistor divider (R8 and R9) during the flyback period. The sensed output voltage is compared to the FB pin threshold to regulate the output or to stop switching in case an overvoltage condition is detected (OVP). This primary-side regulation solution not only reduces the system cost, but also improves the lifetime of the system as no optocoupler (which reduces the life of the power supply significantly) is necessary for power suppliers designed with LinkSwitch-HP.

Voltage divider R8 and R9 is also used to indirectly monitor the bus voltage during the integrated power MOSFET on-time. At start-up the IC enables switching only if the bus voltage has typically reached 100 V (brown-in threshold). If the bus voltage drops for instance during a brown-out condition below typically 40 V the device stops switching (brown-out protection). In case the bus voltage reaches excessive levels (e.g. caused by line surge) the device stops switching. Additionally the cycle-by-cycle current limit is compensated over line to limit the available overload power. See the device data sheet for further details.

The voltage sensed at the FB pin produces a control voltage at the CP pin. Resistor R7 and capacitor C7, C8 are used for control loop compensation. The operating peak primary current and the operating switching frequency are determined by the CP pin voltage.

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5 PCB Layout

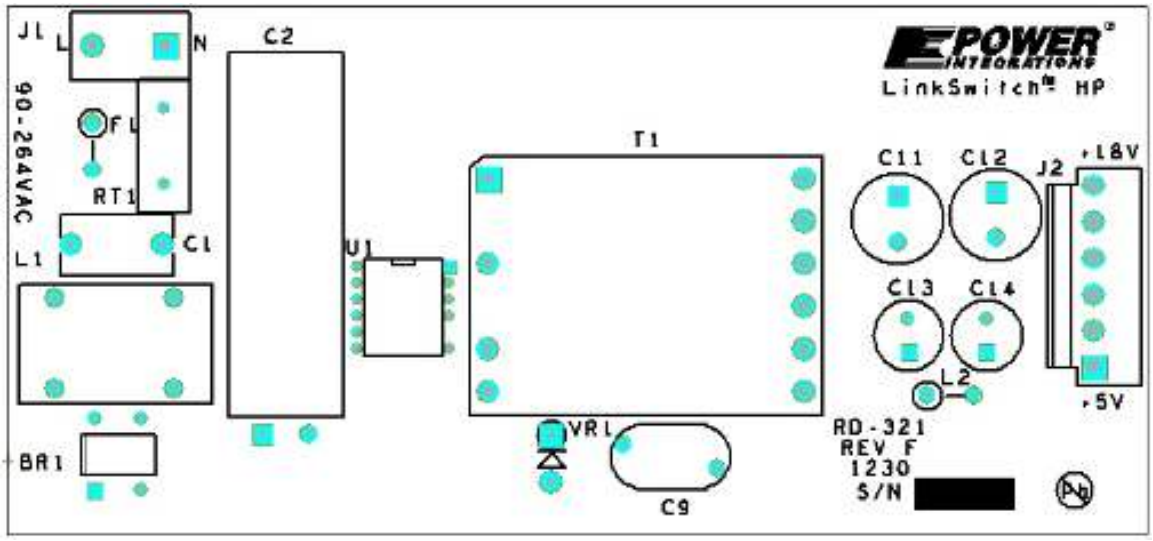

Figure 5 – PCB Top Side.

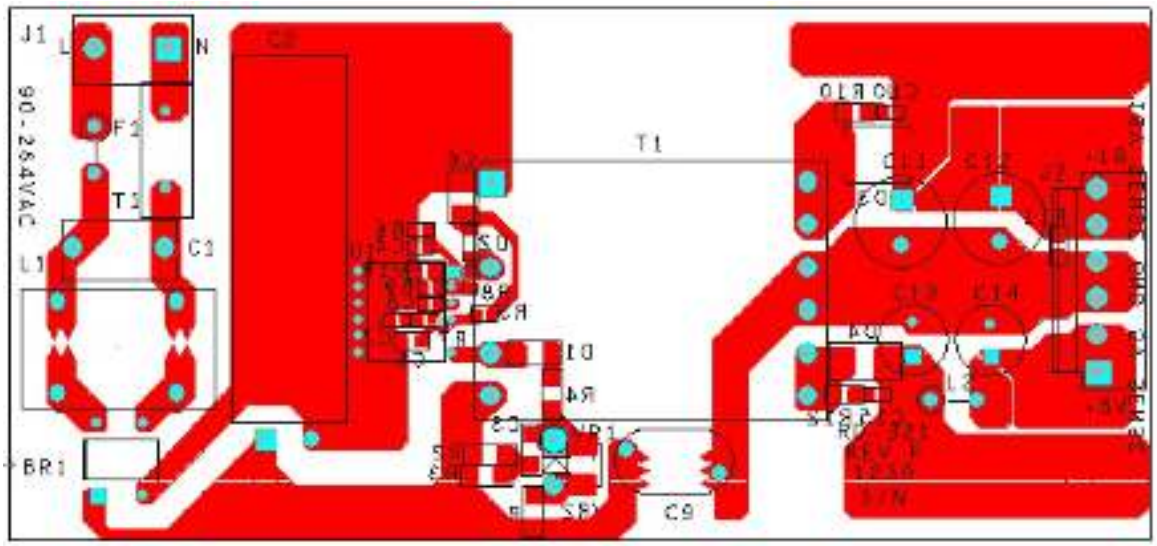

Figure 6 – PCB Bottom Side.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 1 A, Bridge Rectifier, DFM package	DF06M	Diodes, Inc.
2	1	C1	100 nF, 310 VAC, Film, X2	B32921C3104M	Epcos
3	1	C2	47 µF, 400 V, Electrolytic, Low ESR, (12.5 x 30)	EPAG401ELL470MK30S	Nippon Chemi-Con
4	1	C3	10 nF, 630 V, Ceramic, X7R, 1206	C1206C103KBRACTU	Kemet
5	2	C4 C8	100 pF 50 V, Ceramic, NPO, 0603	CC0603JRNPO9BN101	Yageo
6	1	C5	4.7 µF, 10 V, Ceramic, X7R, 0805	C0805C475K8PACTU	Kemet
7	1	C6	22 µF, 25 V, Ceramic, X5R, 1210	ECJ-4YB1E226M	Panasonic
8	1	C7	100 nF, 25 V, Ceramic, X7R, 0603	VJ0603Y104KNXAO	Vishay
9	1	C9	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
10	2	C10 C15	470 pF, 200 V, Ceramic, X7R, 0603	06032C471KAT2A	AVX
11	2	C11 C12	220 µF, 35 V, Electrolytic, Very Low ESR, 53 mΩ, (10 x 12.5)	EKZE350ELL221MJC5S	Nippon Chemi-Con
12	2	C13 C14	820 µF, 6.3 V, Electrolytic, Low ESR, (8 x 11.5)	UHN0J821MPD	Nichicon
13	1	C16	10 pF, 50 V, Ceramic, NPO, 0805	ECJ-2VC1H100D	Panasonic
14	1	D1	600 V, 1 A, Rectifier, Fast Recovery, MELF (DL-41)	DL4937-13-F	Diodes, Inc.
15	1	D2	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
16	1	D3	100 V, 3 A, Schottky, SMC	30BQ100PBF	Vishay
17	1	D4	40 V, 3 A, Schottky, SMD, DO-214AA	B340LB-13-F	Diodes, Inc.
18	1	F1	Fuse, Pico, 2 A, 250 V, Fast, Axial	0263002.MXL	Littlefuse Inc.
19	1	J1	CONN HEADER 3POS (1x3).156 VERT TIN	26-64-4030	Molex
20	1	J2	CONN HEADER 6POS (1x6).156 VERT TIN	26-60-4060	Molex
21	1	L1	22 mH, 0.4 A, Common Mode Choke	ELF18D290C	Panasonic
22	1	L2	3.5 mm x 4.45 mm, 68 Ω at 100 MHz, #22 AWG hole, Ferrite Bead	2743001112	Fair-Rite
23	1	R1	3 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
24	2	R2 R3	100 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ 101V	Panasonic
25	1	R4	20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ 200V	Panasonic
26	1	R5	7.5 k Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3GEYJ 752V	Panasonic
27	1	R6	23.2 k Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF2322V	Panasonic
28	1	R7	100 k Ω, 5%, 1/16 W, Thick Film, 0603	ERJ-3GEYJ 104V	Panasonic
29	1	R8	46.4 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4642V	Panasonic
30	1	R9	10.5 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1052V	Panasonic
31	2	R10 R12	10 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6 GEYJ100V	Panasonic
32	1	R11	36 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ363V	Panasonic
33	1	RT1	NTC Thermistor, 5 Ohms, 4.7 A	CL-150	Thermometrics
34	1	T1	Bobbin, EF25, Horizontal, 12 pins Transformer	YC2504 SNX-R1652	Ying Chin Santronics USA
35	1	U1	LinkSwitch-HP, eDIP-12P	LNK6774V	Power Integrations
36	1	VR1	120 V, 550 mW, 5%, SMB, 403A	1SMB59xxBT3G	Semiconductor
37	1	VR2	OPEN	OPEN	

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7 Transformer Design Spreadsheet

ACDC_LinkSwitch-HP_051612; Rev.0.13; Copyright Power Integrations 2012	INPUT	OUTPUT	UNIT	LinkSwitch-HP Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES				
VACMIN	90	90	V	Minimum AC Input Voltage
VACMAX	265	265	V	Maximum AC Input Voltage
fL	50	50	Hz	AC Mains Frequency
VO	5	5	V	Output Voltage (main)
PO	17	17	W	Output Power
n	0.82	0.82		Efficiency Estimate
Z	0.50	0.50		Loss Allocation Factor
VB	10	10	V	Bias Voltage
tC	3	3	ms	Bridge Rectifier Conduction Time Estimate
CIN	47	47	uF	Input Filter Capacitor
ENTER LINKSWITCH-HP VARIABLES				
LinkSwitch-HP	LNK6774V		LNK6774V	
ILIMITMIN		0.967	A	Minimum Current limit
ILIMITMAX		1.113	A	Maximum current limit
KI	0.60	0.600	A	Current limit reduction factor
ILIMITMIN_EXT			0.580	A
ILIMITMAX_EXT			0.668	A
fS		132000	Hz	LinkSwitch-HP Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin		124000	Hz	LinkSwitch-HP Minimum Switching Frequency
fSmax		140000	Hz	LinkSwitch-HP Maximum Switching Frequency
KP	0.5	0.50		Ripple to Peak Current Ratio (0.4 < KP < 6.0)
VOR	110	110.00	V	Reflected Output Voltage
Voltage Sense				
VUVON			100	100.00
VUVOFF			42.55	V
VOV			446.26	V
FMAX_FULL_LOAD		132885	Hz	Maximum switching frequency at full load
FMIN_FULL_LOAD		117698	Hz	Minimum switching frequency at full load
TSAMPLE_FULL_LOAD				
TSAMPLE_LIGHT_LOAD		1.77	us	Minimum available Diode conduction time at light load. This should be greater than 1.11 us

Rpd		23.20	k-ohm	Program delay Resistor
Cpd	10	10.00	nF	Program delay Capacitor
Total programmed delay		0.06	sec	Total program delay
VDS		4.11	V	LinkSwitch-HP on-state Drain to Source Voltage
VD				
VDB			0.70	V
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES				
Core Type	EF25			
Core		EF25		Selected Core
Custom Core				Enter name of custom core is applicable
AE	0.5180	0.518	cm^2	Core Effective Cross Sectional Area
LE	5.7800	5.78	cm	Core Effective Path Length
AL	2000.0	2000	nH/T^2	Ungapped Core Effective Inductance
BW	15.6	15.6	mm	Bobbin Physical Winding Width
M	0.00	0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			4.00	4
NS	3.00	3		Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS				
VMIN	85	85	V	Minmum DC Input Voltage
VMAX	375	375	V	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS				
DMAX		0.58		Maximum Duty Cycle
IAVG		0.24	A	
IP		0.56	A	Peak Primary Current
IR				
IRMS		0.33	A	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS				
LP_TYP		1436	uH	Typical Primary Inductance
LP_TOL	7	7	%	Primary inductance Tolerance
NP		60		Primary Winding Number of Turns
NB		6		Bias Winding Number of Turns
ALG		399	nH/T^2	Gapped Core Effective Inductance
BM		2607	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP		3301	Gauss	Peak Flux Density (BP<3700)
BAC		652	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)

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ur		1776		Relative Permeability of Ungapped Core
LG		0.13	mm	Gap Length (Lg > 0.1 mm)
BWE		62.4	mm	Effective Bobbin Width
OD	0.32	0.32	mm	Maximum Primary Wire Diameter including insulation
INS		0.05	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA		0.27	mm	Bare conductor diameter
AWG		30	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM				
CMA		310	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)
FEEDBACK SENSING SECTION				
RFB1		37.40	k-ohms	Feedback divider upper resistor
RFB2				
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)				
Lumped parameters				
ISP		11.29	A	Peak Secondary Current
ISRMS		5.61	A	Secondary RMS Current
IO		3.40	A	Power Supply Output Current
IRIPPLE		4.46	A	Output Capacitor RMS Ripple Current
CMS		1122	Cmils	Secondary Bare Conductor minimum circular mils
AWGS		19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS		0.91	mm	Secondary Minimum Bare Conductor Diameter
ODS				5.20
INSS		2.14	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS				
VDRAIN		626	V	Peak voltage acoss drain to source of Linkswitch-HP
PIVS		24	V	Output Rectifier Maximum Peak Inverse Voltage
PIVB				
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)				
1st output				
VO1	5.00	5	V	Output Voltage
IO1	1.00	1.00	A	Output DC Current
PO1		5.00	W	Output Power
VD1	0.35	0.35	V	Output Diode Forward Voltage Drop
NS1		2.92		Output Winding Number of Turns
ISRMS1		1.651	A	Output Winding RMS Current

IRIPPLE1		1.31	A	Output Capacitor RMS Ripple Current
PIVS1		23	V	Output Rectifier Maximum Peak Inverse Voltage
CMS1		330	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1		24	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1		0.51	mm	Minimum Bare Conductor Diameter
ODS1		5.35	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output				
VO2	18.00		V	Output Voltage
IO2	0.67		A	Output DC Current
PO2		12.06	W	Output Power
VD2	0.50	0.5	V	Output Diode Forward Voltage Drop
NS2		10.09		Output Winding Number of Turns
ISRMS2		1.106	A	Output Winding RMS Current
IRIPPLE2		0.88	A	Output Capacitor RMS Ripple Current
PIVS2		81	V	Output Rectifier Maximum Peak Inverse Voltage
CMS2		221	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2		26	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2		0.41	mm	Minimum Bare Conductor Diameter
ODS2		1.55	mm	Maximum Outside Diameter for Triple Insulated Wire

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8 Transformer Specification

8.1 Electrical Diagram

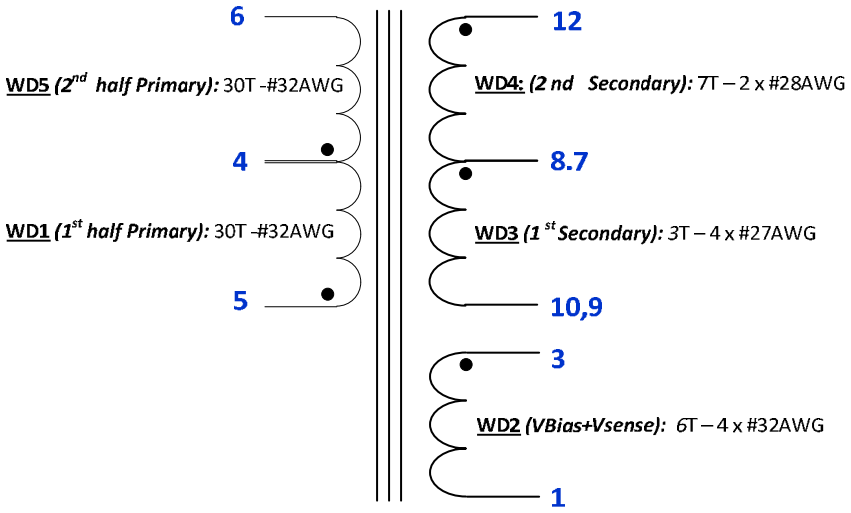

Figure 7 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-6 and pins 7-12.	3000 VAC
Primary Inductance	Pins 5-6, all other windings open, measured at 100 kHz, 0.4 VRMS.	1436 µH ±7%
Resonant Frequency	Pins 5-6, all other windings open.	1500 kHz (Min.)
Primary Leakage Inductance	Pins 5-6, with pins 7-12 shorted, measured at 100 kHz, 0.4 VRMS.	15 µH (Max.)

8.3 Materials

Item	Description
[1]	Core: EF25, TDK PC44-EF25Z, and gapped ALG 398.9 nH/T^2.
[2]	Bobbin: EF25-Horizontal, 12 pins (6/6), Ying Chin, P/N: YC-2504.
[3]	Magnet wire: #32 AWG Solderable, double coated.
[4]	Magnet wire: #27 AWG Solderable, double coated.
[5]	Magnet wire: #28 AWG Solderable, double coated.
[6]	Teflon tube: Alpha Wire, TFT, or equivalent.
[7]	Tape: 3M 44 Margin tape (cream), 3.5 mm wide, or equivalent.
[8]	Tape: 3M 1298 Polyester Film, 8.6 mm wide, 2.0 mils thick, or equivalent.
[9]	Tape: 3M 1298 Polyester Film, 15.6 mm wide, 2.0 mils thick, or equivalent.
[10]	Varnish: Dolph BC-359, or equivalent.

8.4 Transformer Build Diagram:

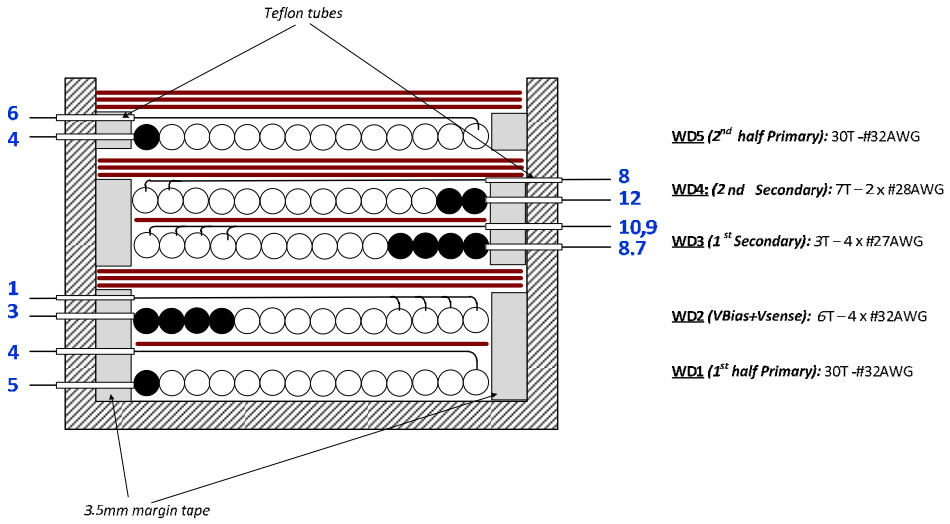

Figure 8 – Transformer Build Diagram.

8.5 Transformer Construction:

Winding preparation	Place the bobbin item [2] on the mandrel with the primary side is on the left side. Winding direction is clockwise direction. Margin tape item [7] should be applied for all windings. Note: Teflon tubes item [6] should be inserted into all wire ends and reach to inside edge of margin tapes. Return wires should be inside the winding section and not overlap on the margin tape. (See pictures below).
WD1 1st Half Primary	Start at pin 5, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 4.
Insulation	Place 1 layer of tape item [8].
WD2 VBias+VSense	Start at pin 3, wind 6 quad-filar turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 1.
Insulation	Place 3 layers of tape item [9].
WD3 1st Secondary	Start at pins 8,7, wind 3 quad-filar turns of wire item [4] from right to left, spread the wire evenly, at the last turn bring the wire back to the right, and terminate at pin 10,9.
Insulation	Place 1 layer of tape item [8].
WD4 2nd Secondary	Start at pins 12, wind 7 bi-filar turns of wire item [5] from right to left, spread the wire evenly, at the last turn bring the wire back to the right, and terminate at pin 8.
Insulation	Place 3 layers of tape item [9].
WD5 2nd Half Primary	Start at pin 4, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 6.
Final Assembly	Grind and secure core halves with tape. Vanish item [10].

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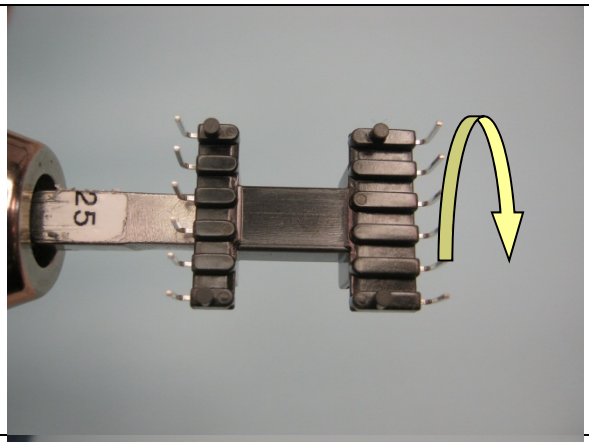
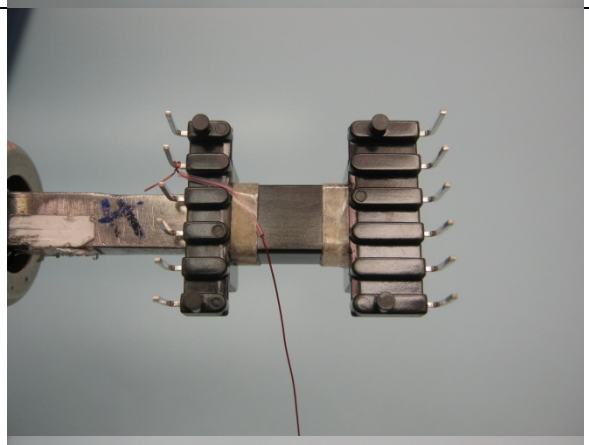
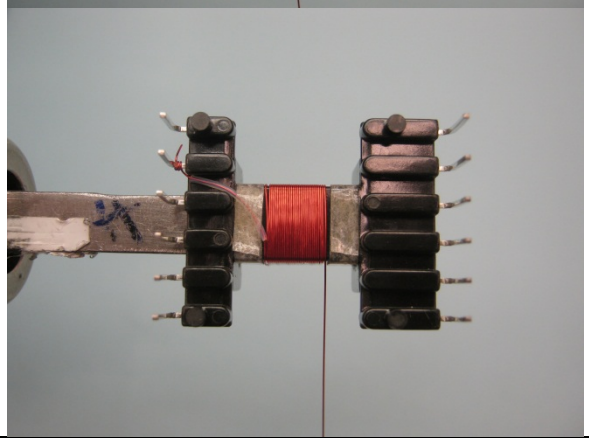
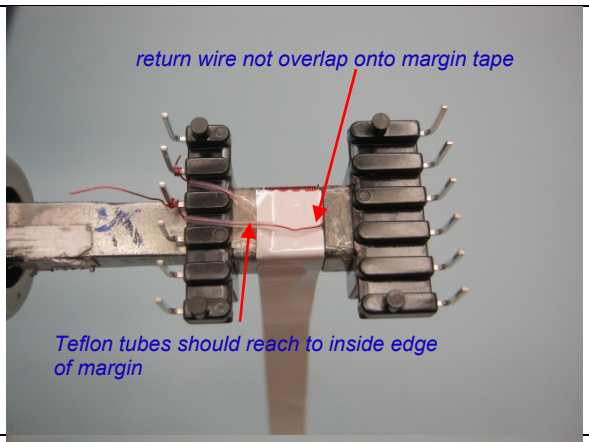
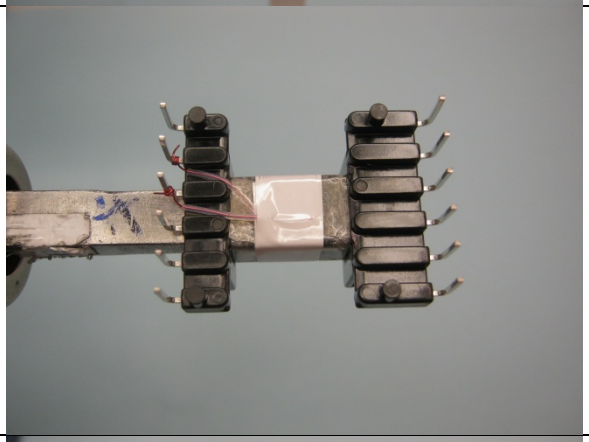
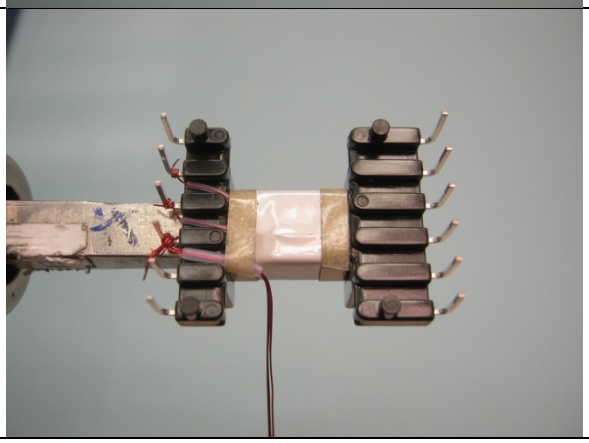
8.6 Transformer Illustrations:

Winding Preparation		Place the bobbin item [2] on the mandrel with the primary-side is on the left side. Winding direction is clockwise direction.
WD1 **1st Half Primary**	 	Start at pin 5, wind 30 turns of wire item [3] from left to right with tight tension, at the last turn bring the wire back to the left, and terminate at pin 4.

		
Insulation		Place 1 layer of tape item [8].
WD2 **VBias+VSense**		Start at pin 3, wind 6 quad-filar turns of wire item [3] from left to right with tight tension,

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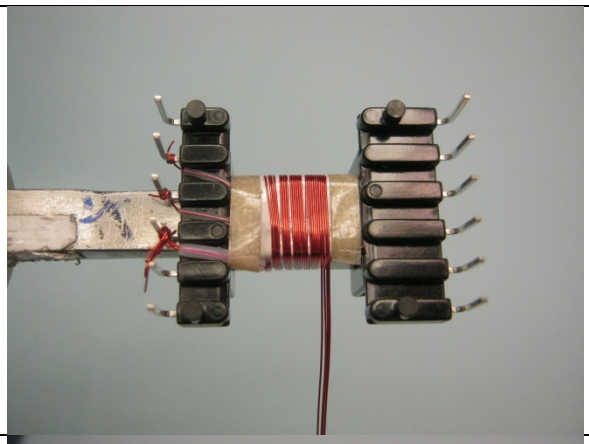
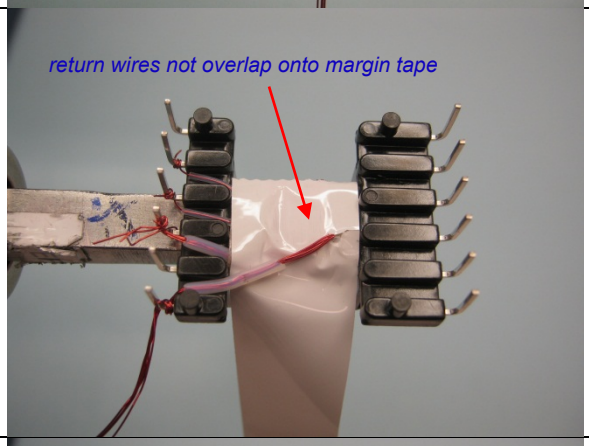
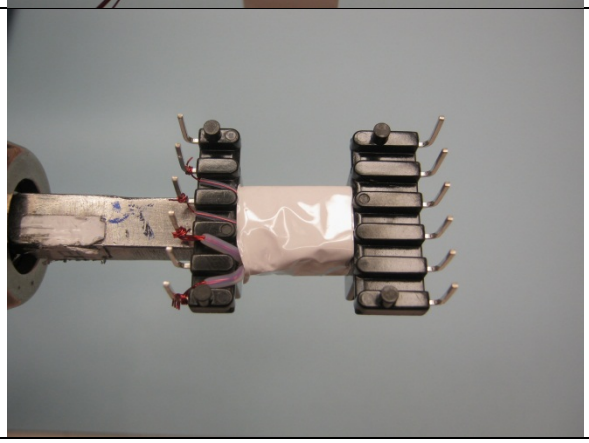
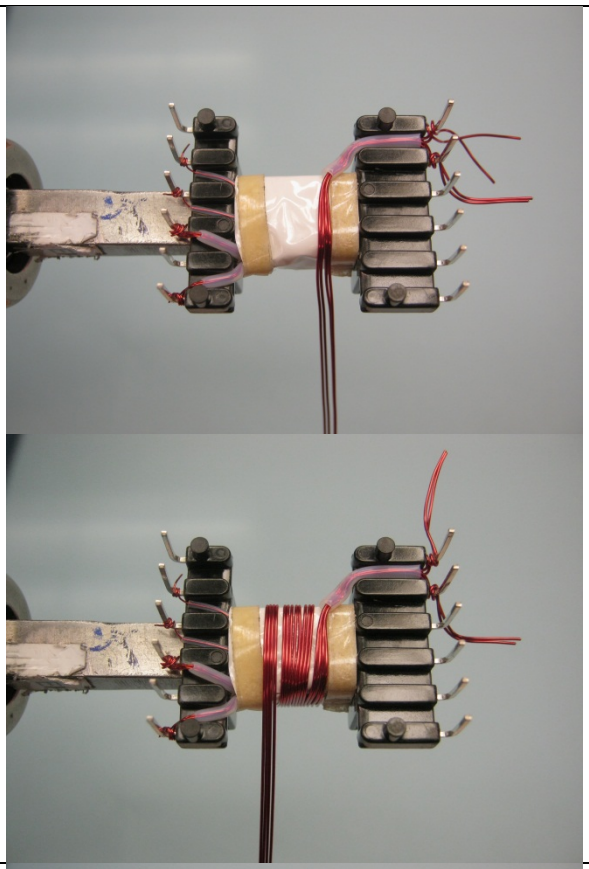
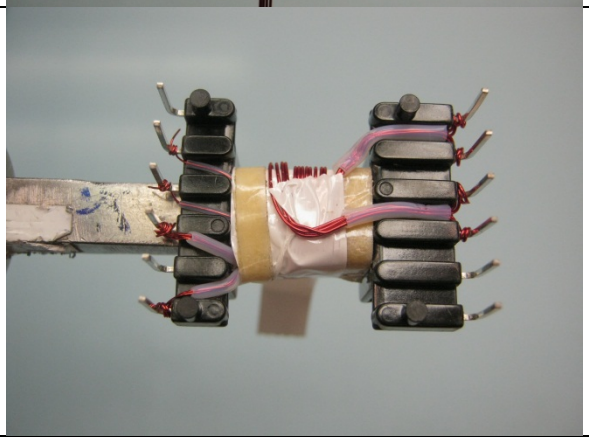
		
		At the last turn bring the wire back to the left, and terminate at pin 1.
Insulation		Place 3 layers of tape item [9].

WD3 **1st Secondary**		Start at pins 8, 7, wind 3 quad-filar turns of wire item [4] from right to left, spread the wire evenly,
		At the last turn bring the wire back to the right, and terminate at pin 10, 9.

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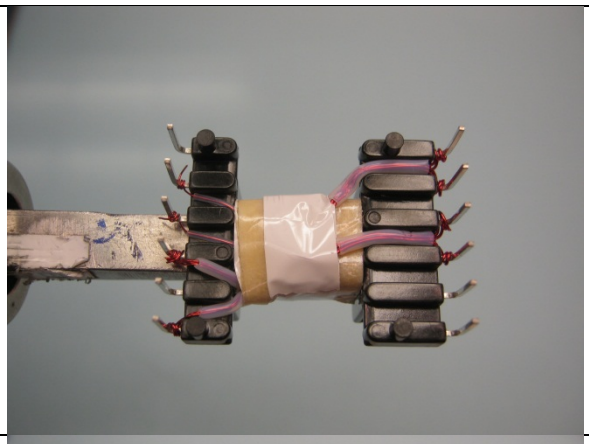
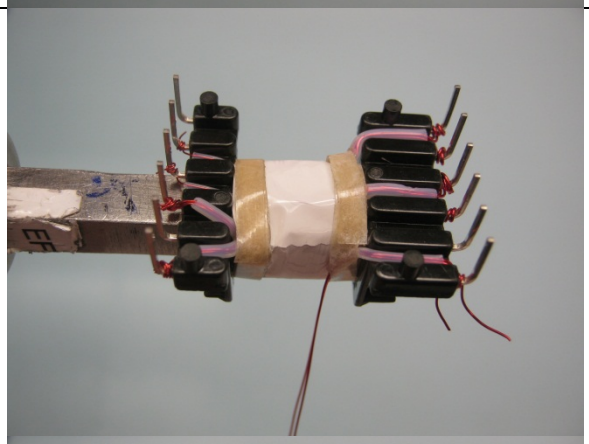
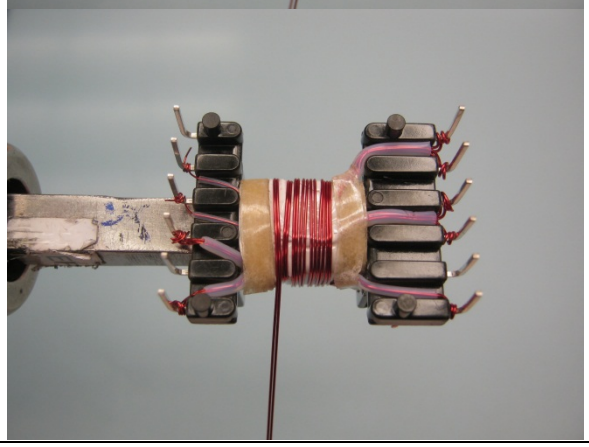
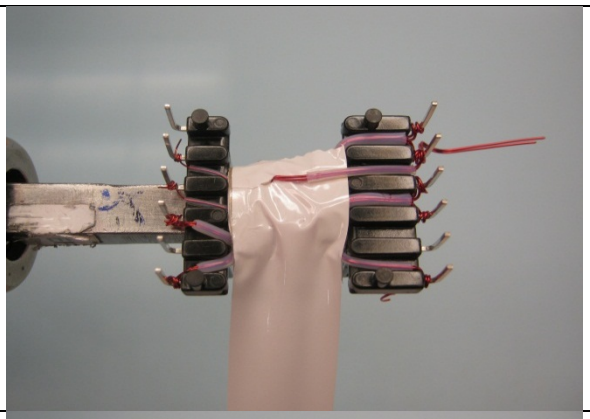
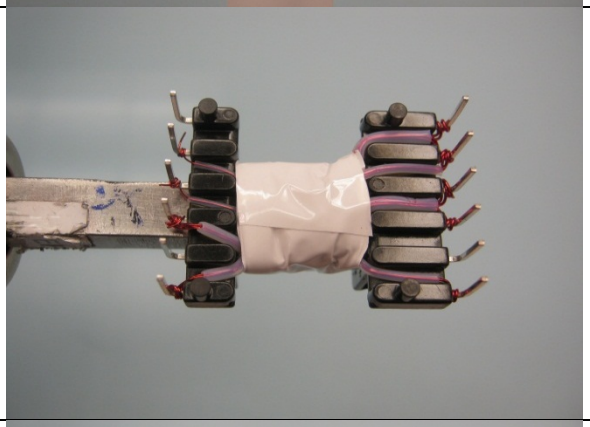
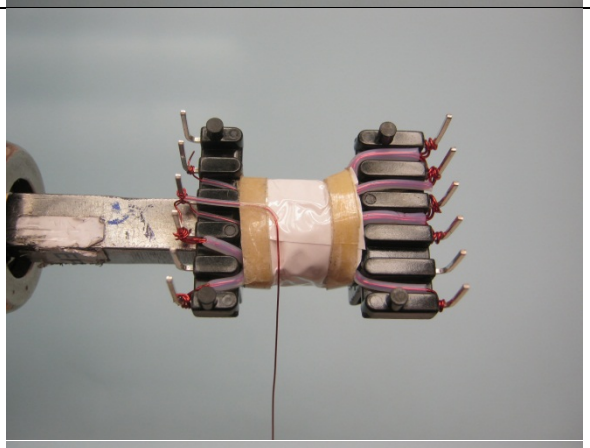
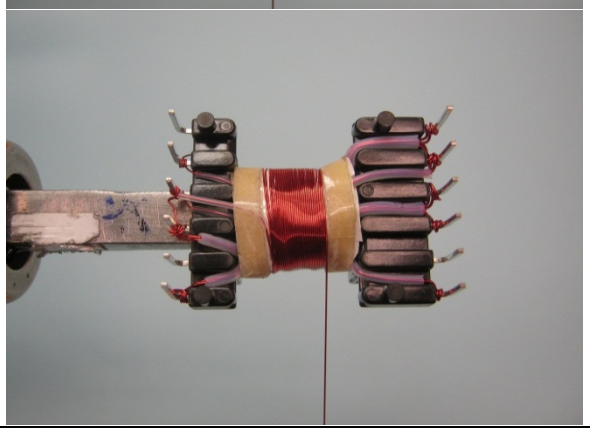
Insulation		Place 1 layer of tape item [8].
WD4 **2nd Secondary**	 	Start at pins 12, wind 7 bi-filar turns of wire item [5] from right to left, spread the wire evenly,

		At the last turn bring the wire back to the right, and terminate at pin 8.
Insulation		Place 3 layers of tape item [9].
WD5 **2nd Half Primary**	 	Start at pin 4, wind 30 turns of wire item [3] from left to right with tight tension,

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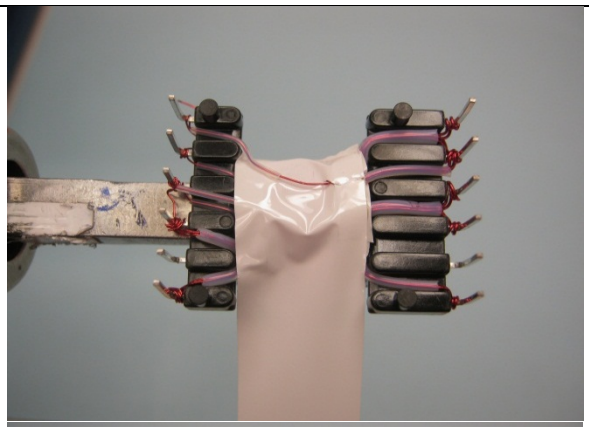
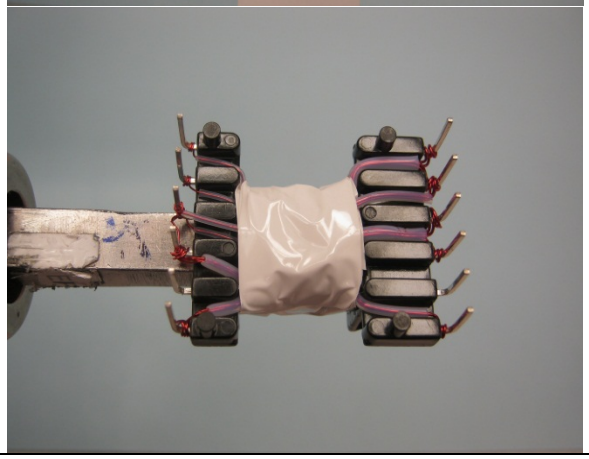
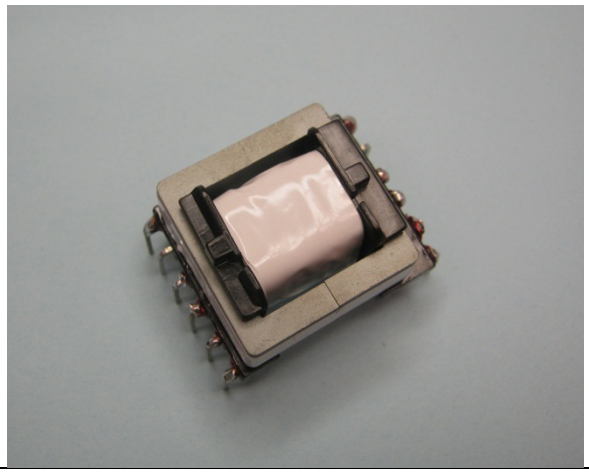
	 	At the last turn bring the wire back to the left, and terminate at pin 6.
Core Assembly		Grind and secure core halves with tape.
Varnish Transformer and Finish		Varnish item [10].

9 Performance Data

All measurements performed at room temperature and 50 Hz line frequency, except where otherwise stated. For all tests, the full load is 1000 mA for the 5 V output and 670 mA for the 18 V output (17 W total output power).

9.1 Active Mode Efficiency

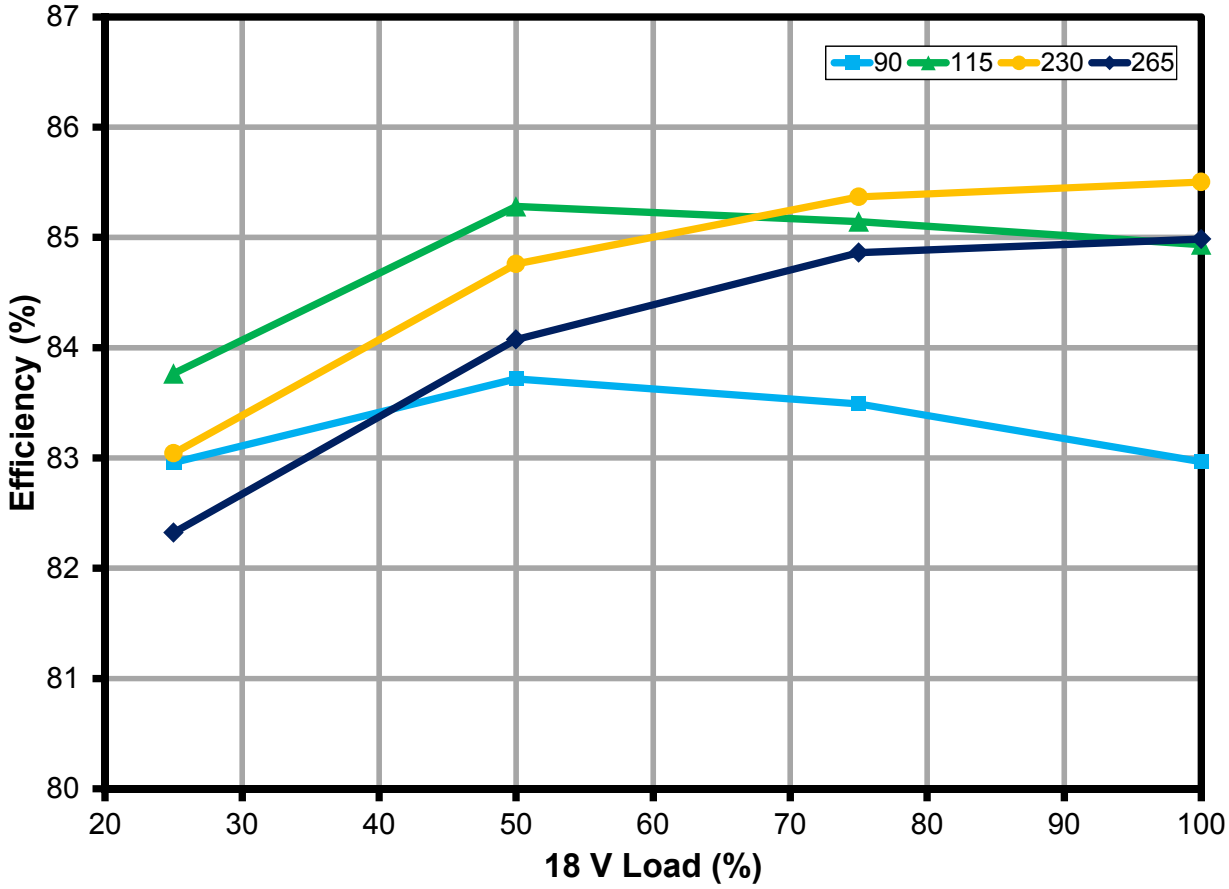


Figure 9 – Efficiency vs. LCD brightness, Room Temperature.

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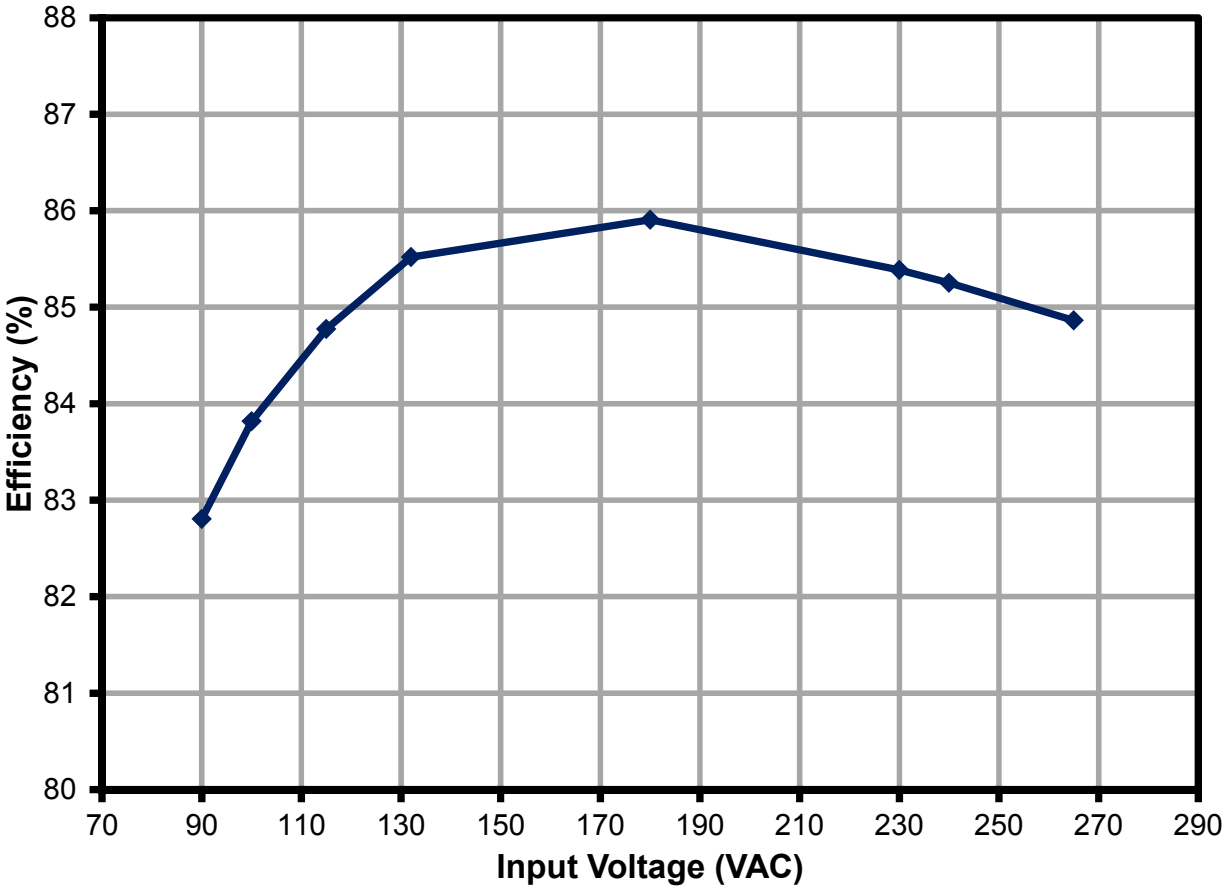

Figure 10 – Full Load Efficiency vs. Input Voltage, Room Temperature.

9.2 Input Power at Standby and Standby Efficiency

Standby power and efficiency is measured using a 10 mA load on the 5 V output. The 18 V output is unloaded.

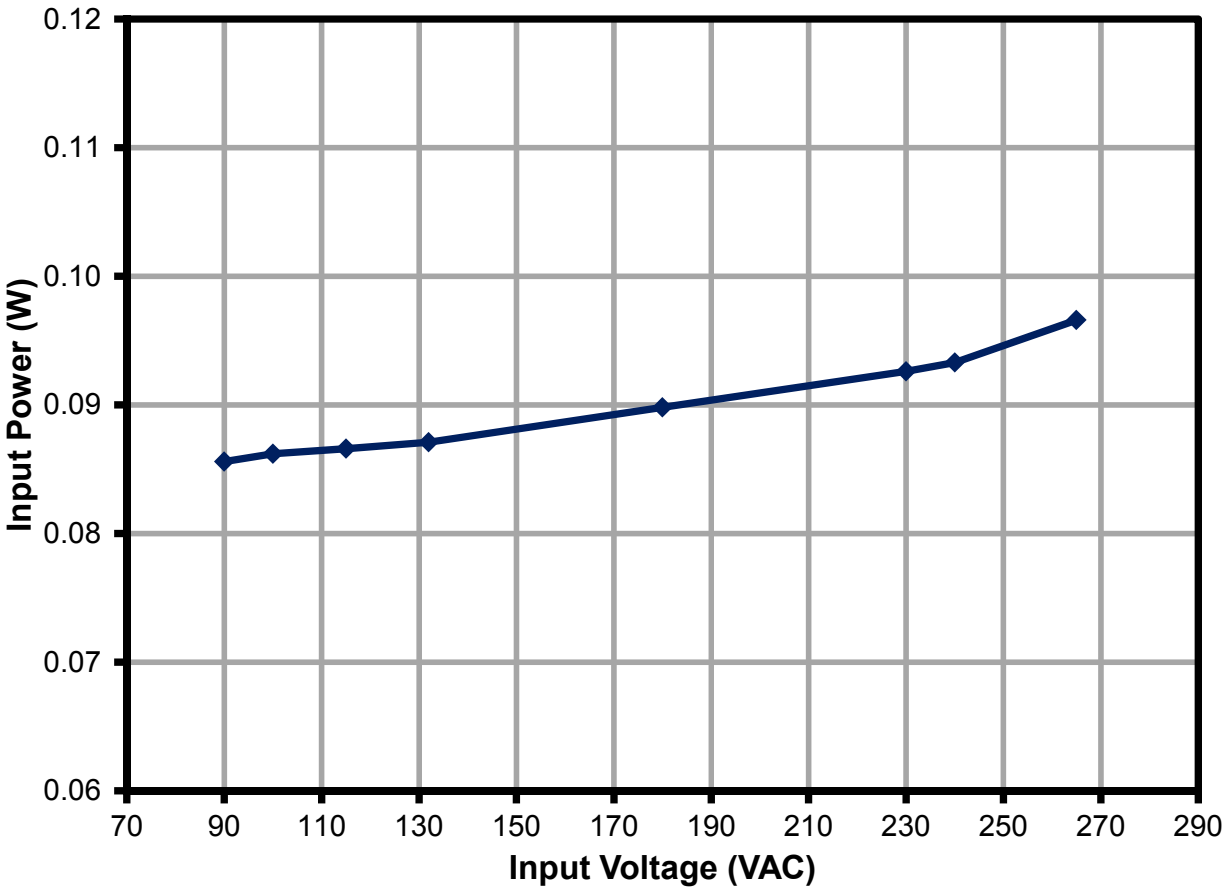

Figure 11 – Standby Input Power vs. Input Line Voltage, Room Temperature.

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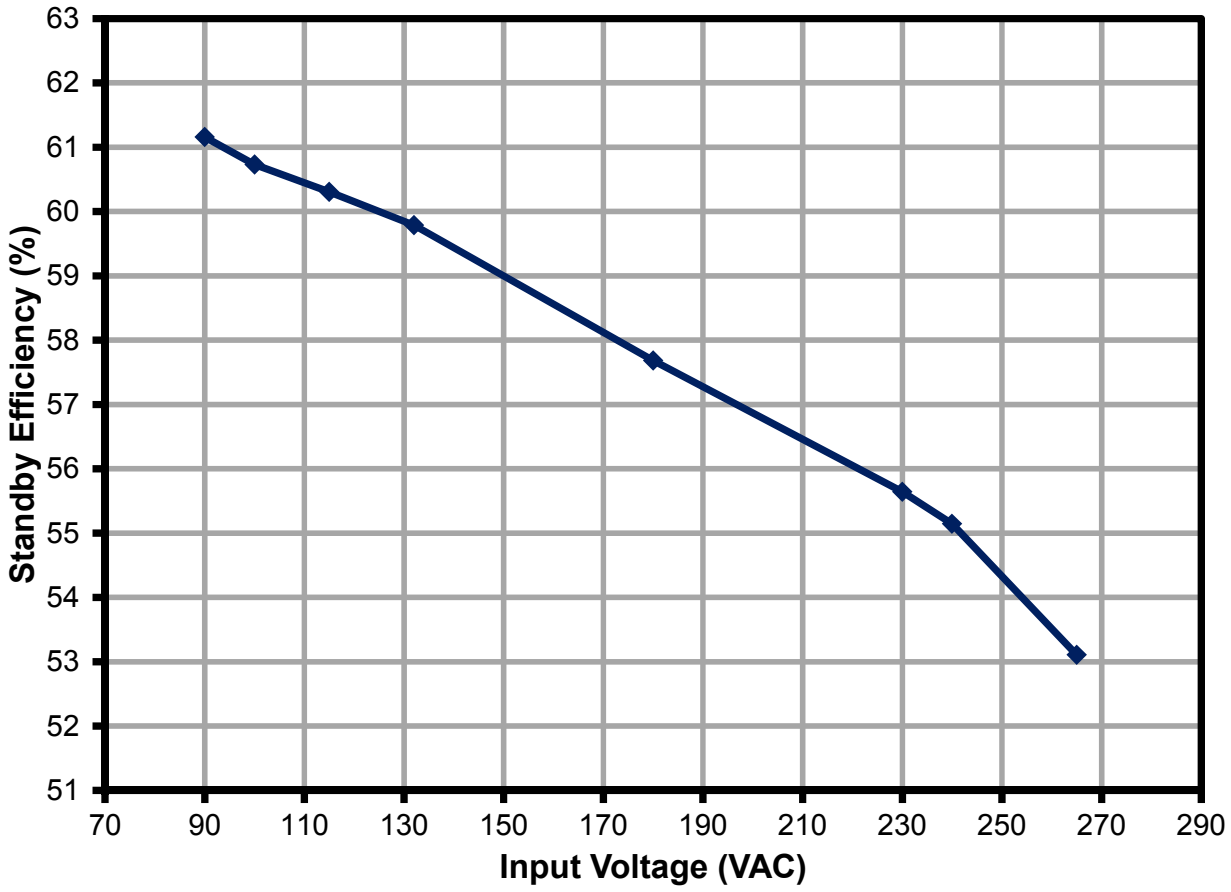

Figure 12 – Standby Efficiency vs. Input Voltage, Room Temperature.

9.3 Line Regulation at 18 V 0.67 A DC Load and 5 V 1 A Average Load

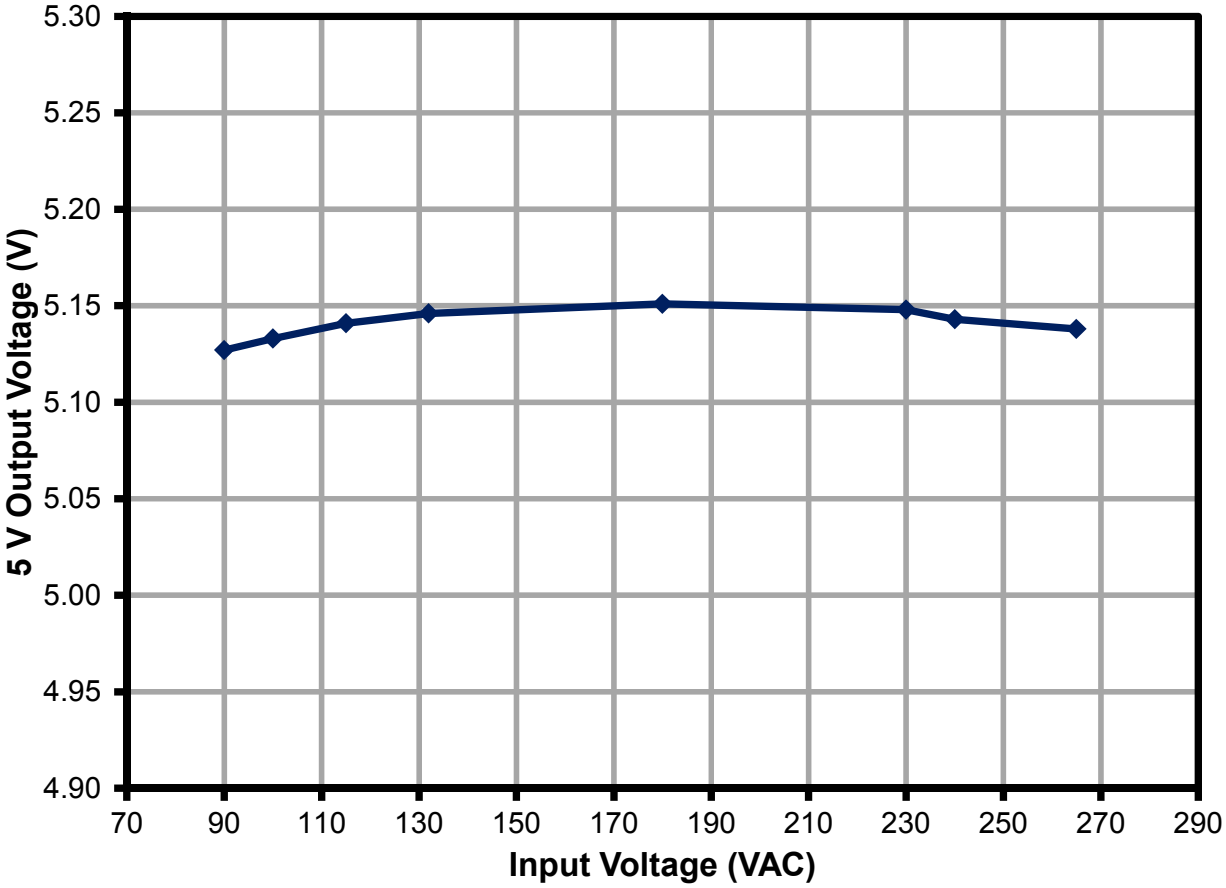

Figure 13 – 5 V Line Regulation under Full Load.

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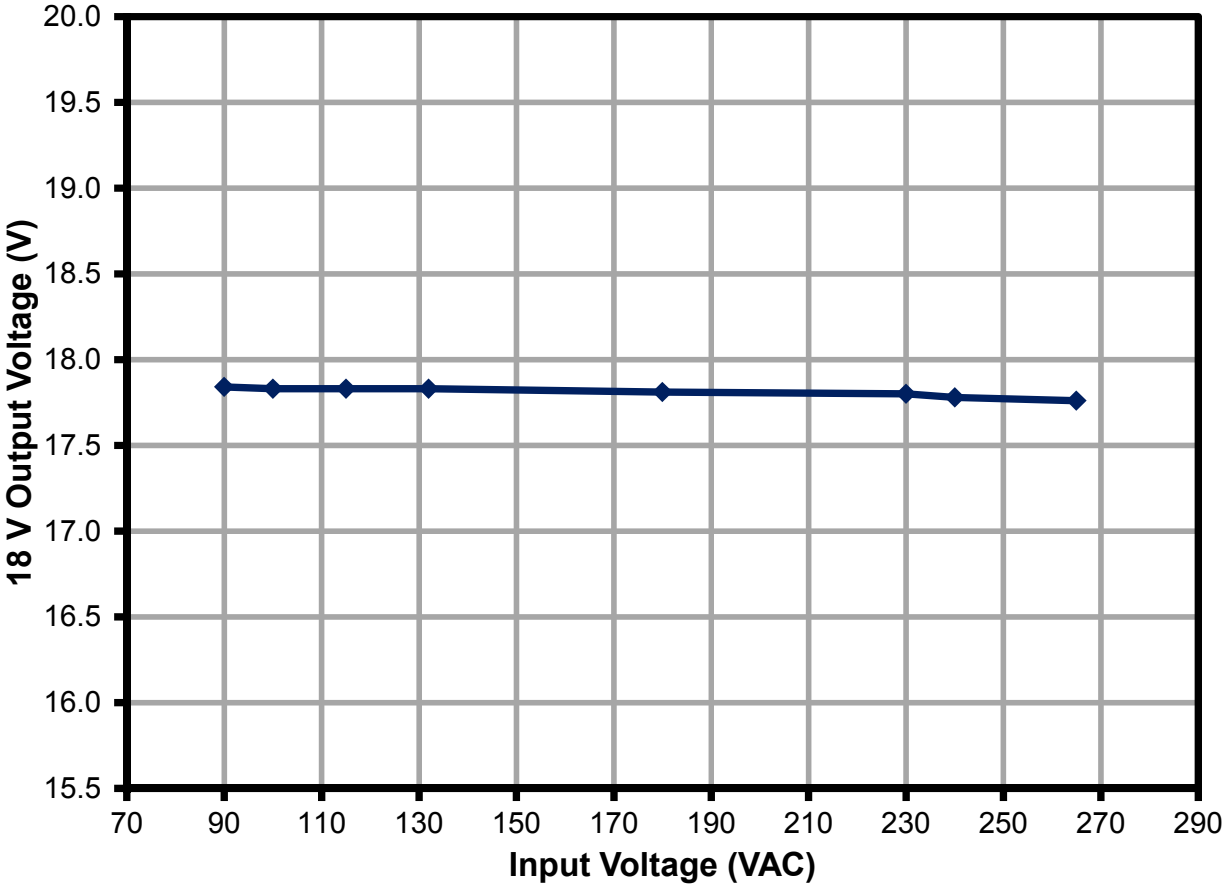

Figure 14 – 18 V Line Regulation under Full Load.

9.4 Output Voltage under Specified Dynamic Load Profile Including Peak, Minimum and Mean Value

9.4.1 Test Method for Peak and Minimum Output Voltage

Figure 15 shows how the peak value and minimum value were collected. The power supply was loaded with the specified load profile in Figure 3. 18 V output load (LCD brightness) is always a pulsed load from 0 to 0.67 A with different duty cycle and 5 V load is always transient from 0.5 A to 1.5 A. Scope were used to record the peak value and minimum value for both output voltage, and the mean value is recorded with multimeter.

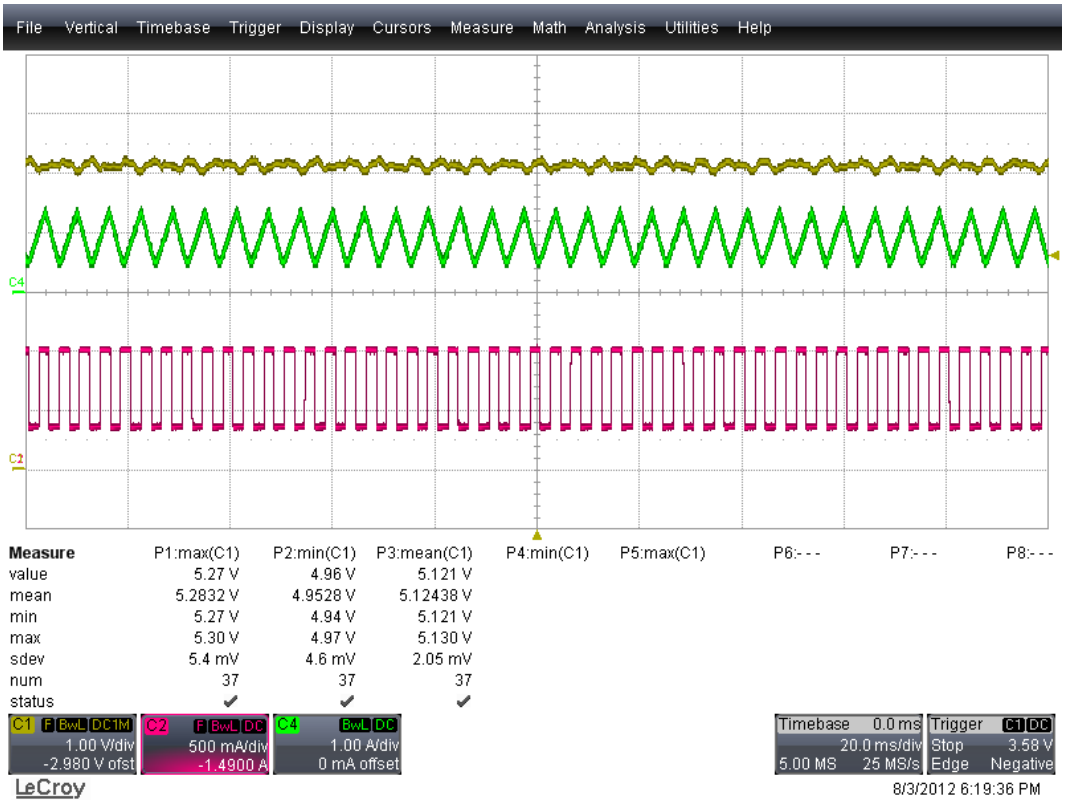

Figure 15 – Test Method for Peak and Minimum Output Voltage.

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9.4.2 5 V Output Voltage under Specified Load Profile

Figures below shows mean regulation (measured with multimeter), peak and minimum output voltage (measured with scope) under specified dynamic load profile.

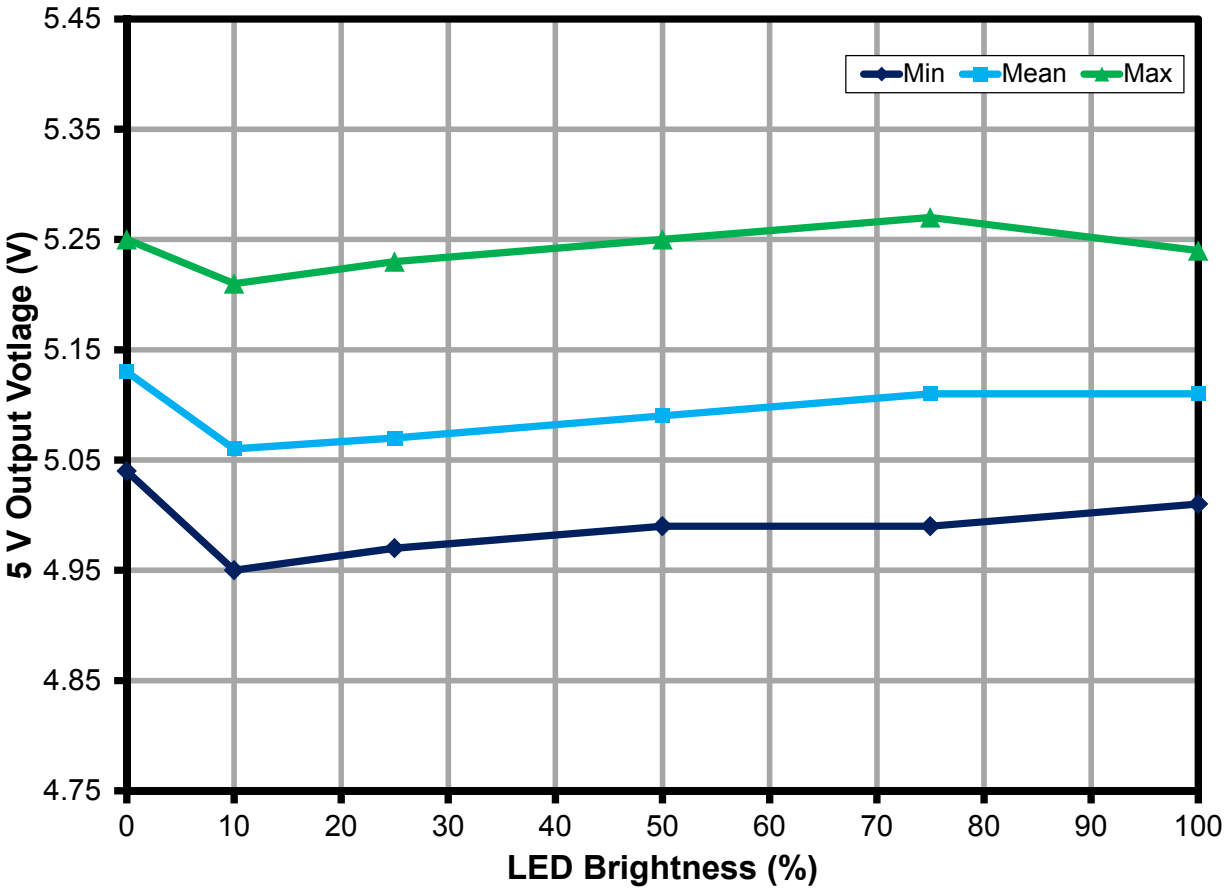

Figure 16 – 5 V Output Voltage under Specified Load Profile at 90 VAC.

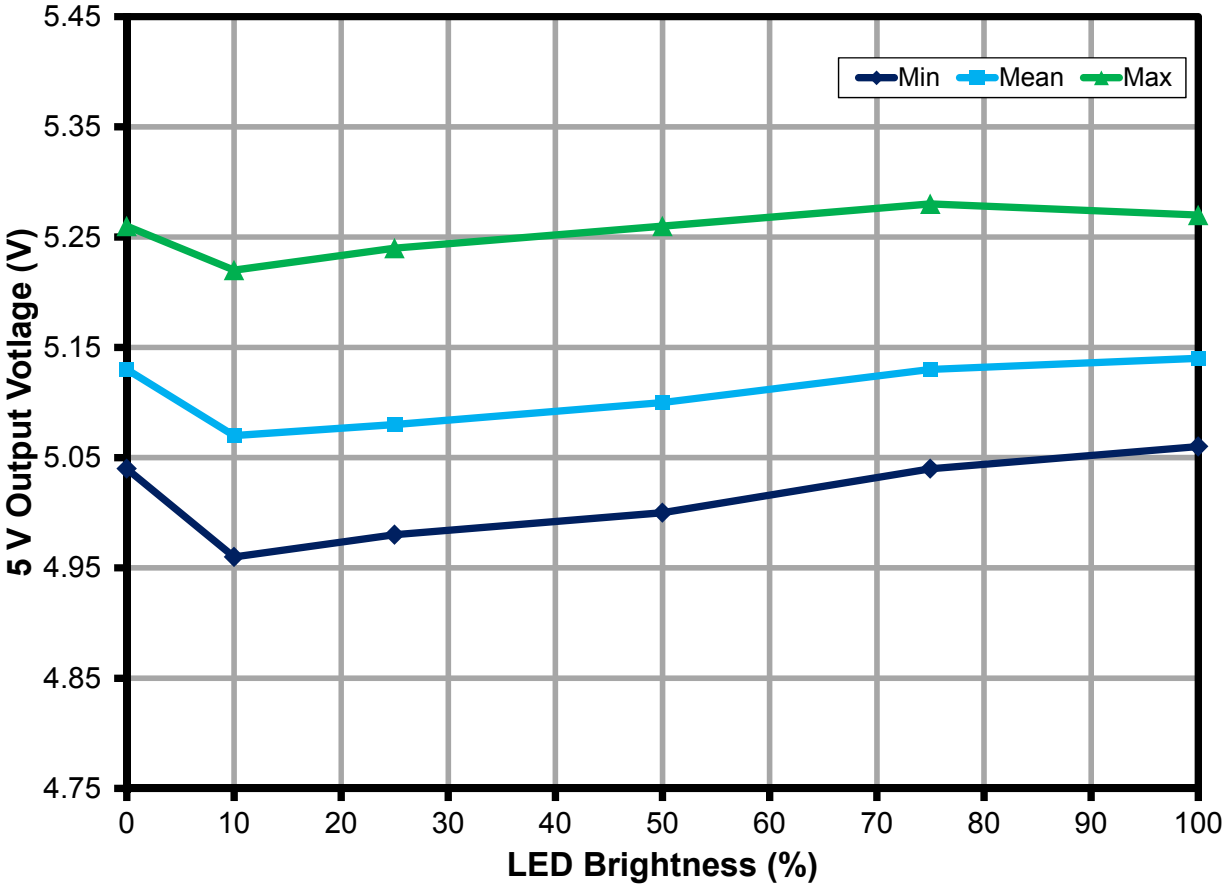

Figure 17 – 5 V Output Voltage under Specified Load Profile at 115 VAC.

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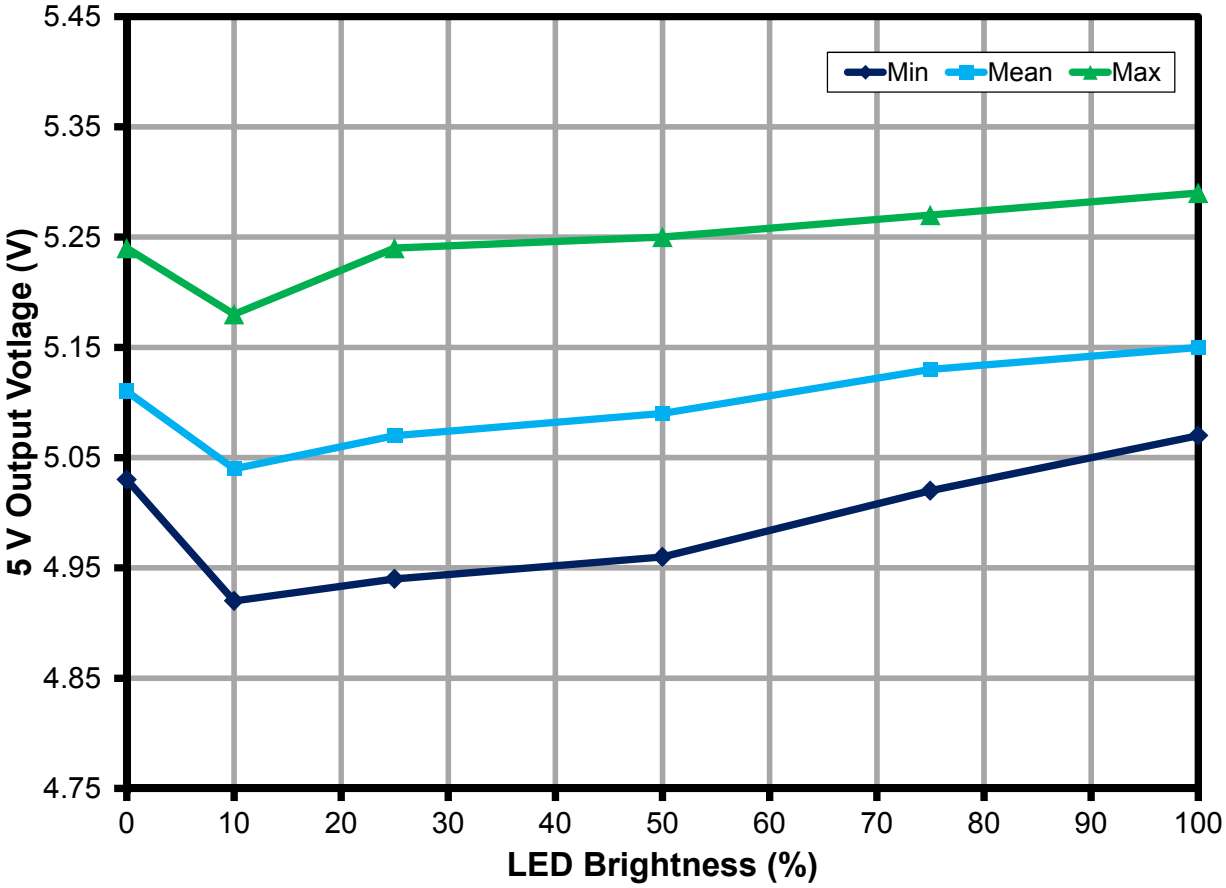

Figure 18 – 5 V Output Voltage under Specified Load Profile at 230 VAC.

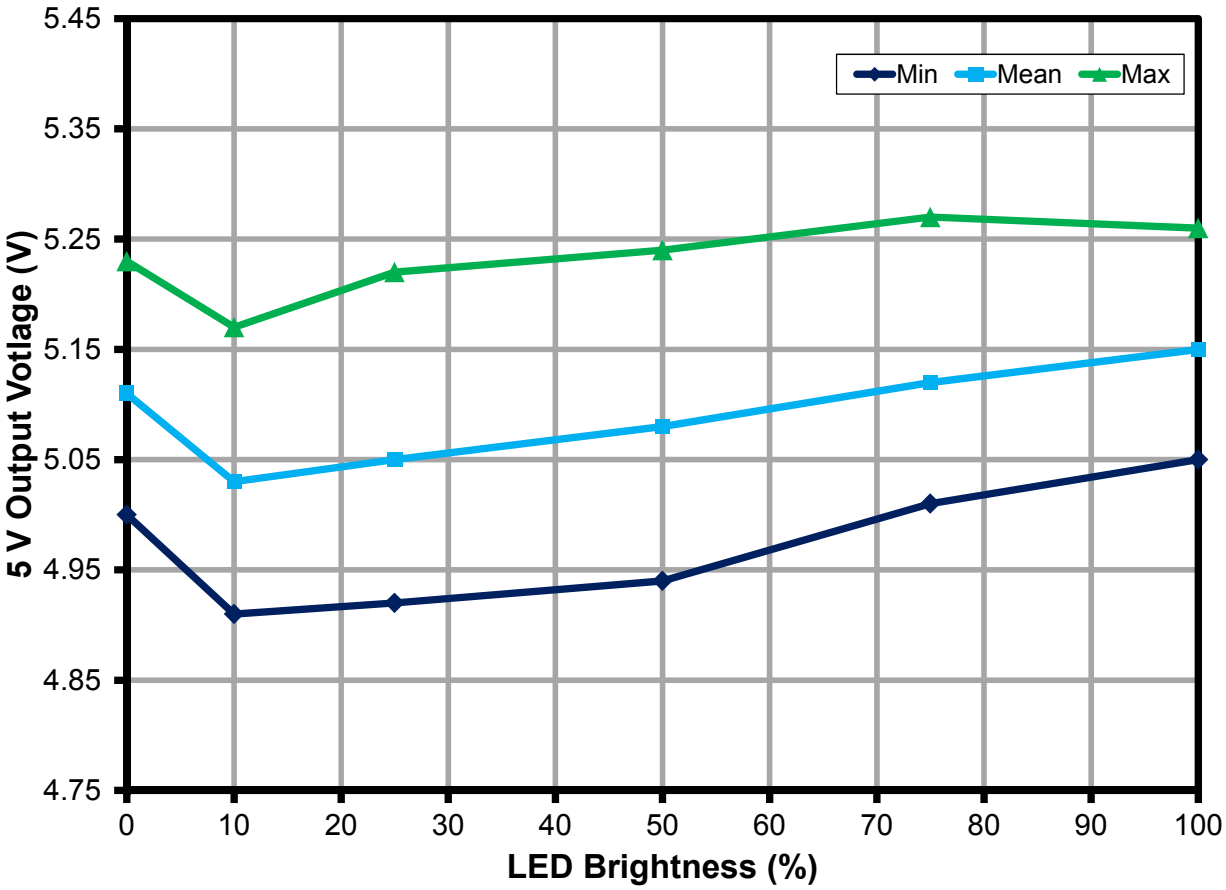

Figure 19 – 5 V Output Voltage under Specified Load Profile at 265 VAC.

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9.4.3 18 V Output Voltage under Specified Load Profile

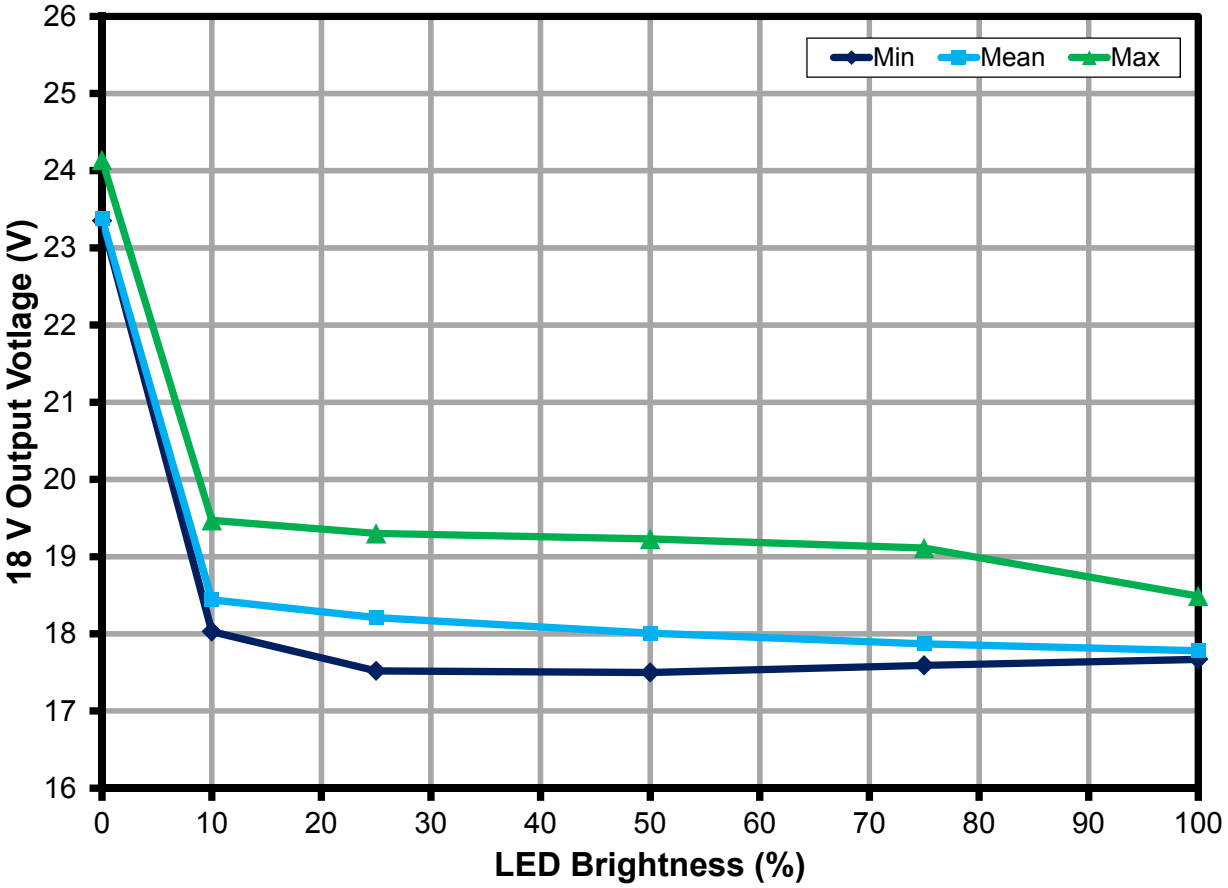

Figure 20 – 18 V Output Voltage under Specified Load Profile at 90 VAC

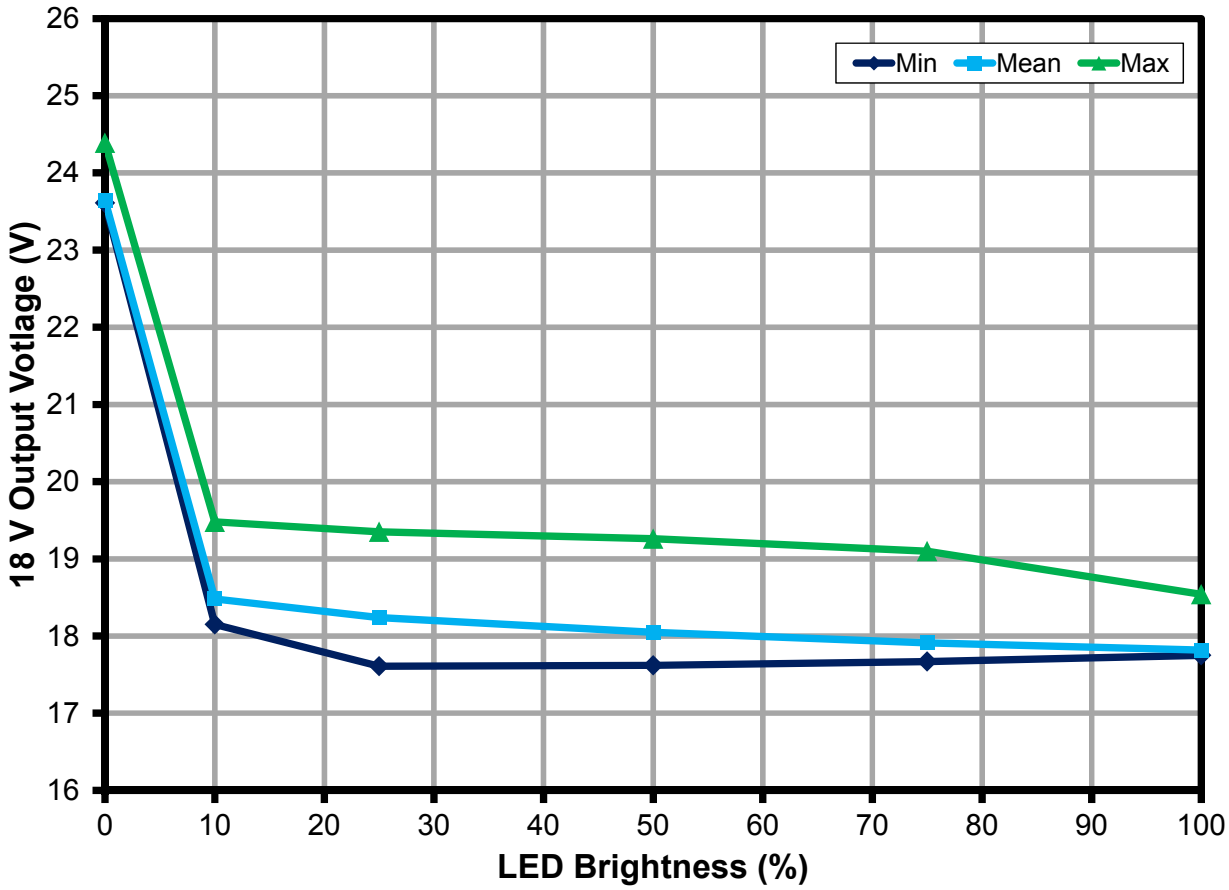

Figure 21 – 18 V Output Voltage under Specified Load Profile at 115 VAC.

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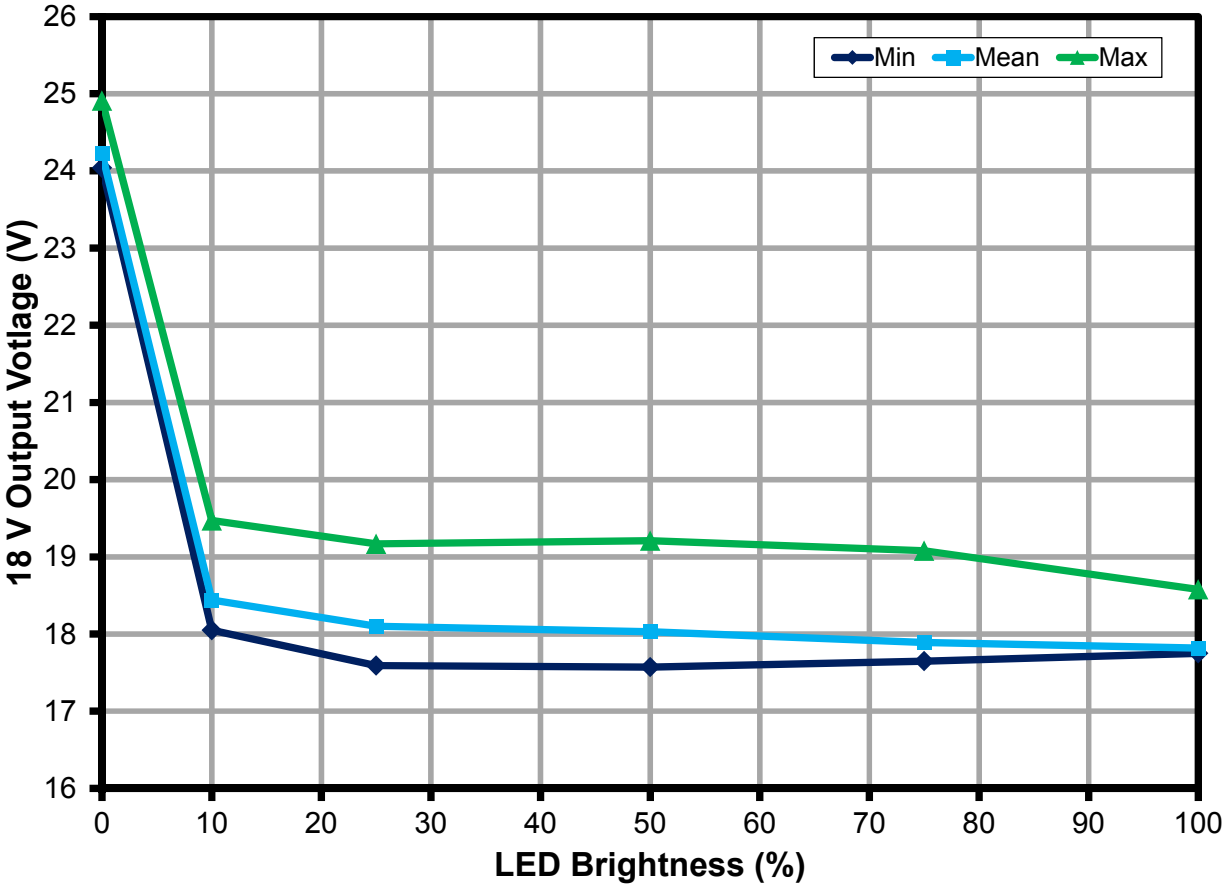

Figure 22 – 18 V Output Voltage under Specified Load Profile at 230 VAC.

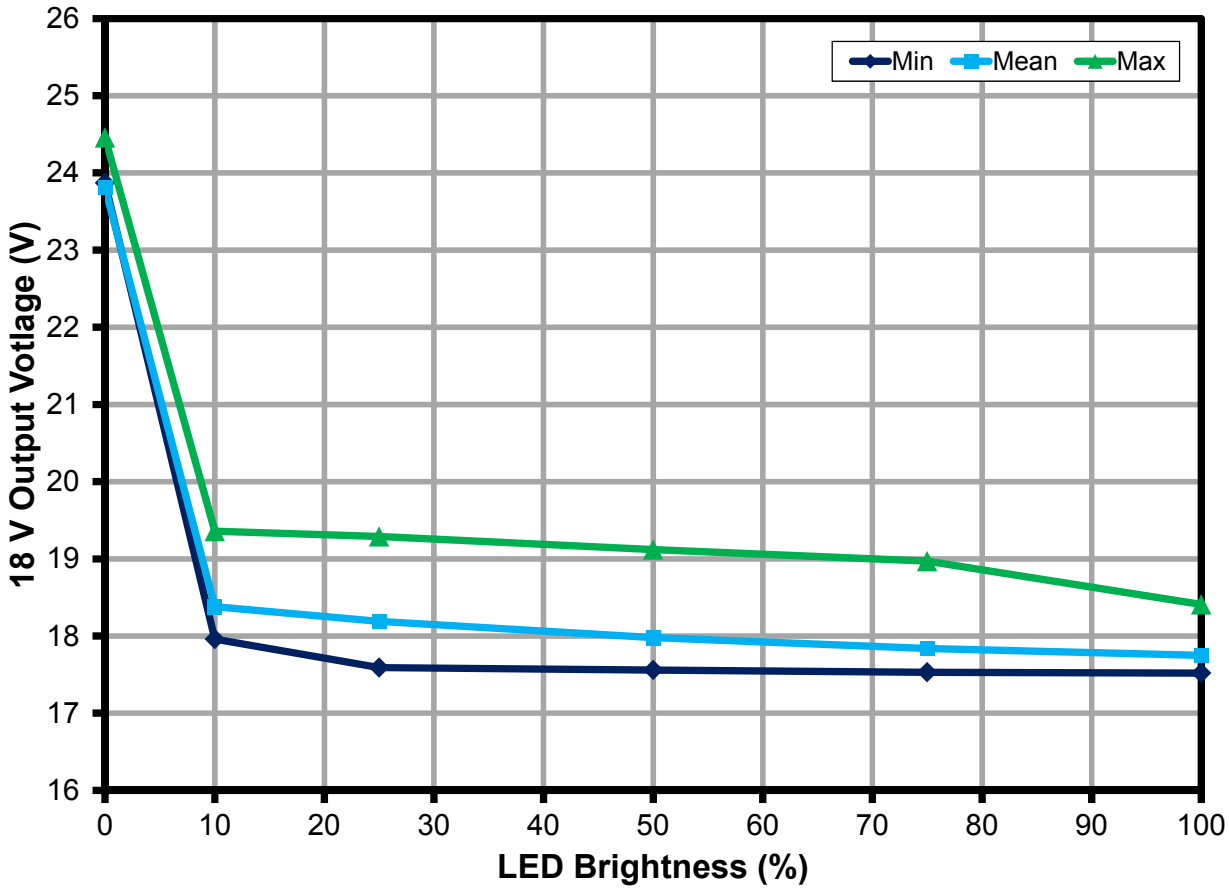

Figure 23 – 18 Output Voltage under Specified Load Profile at 265 VAC.

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10 Thermal Performance

The unit was allowed to reach thermal equilibrium prior to the measurement. Figure 24 is the temperature profile of the board at room temperature.

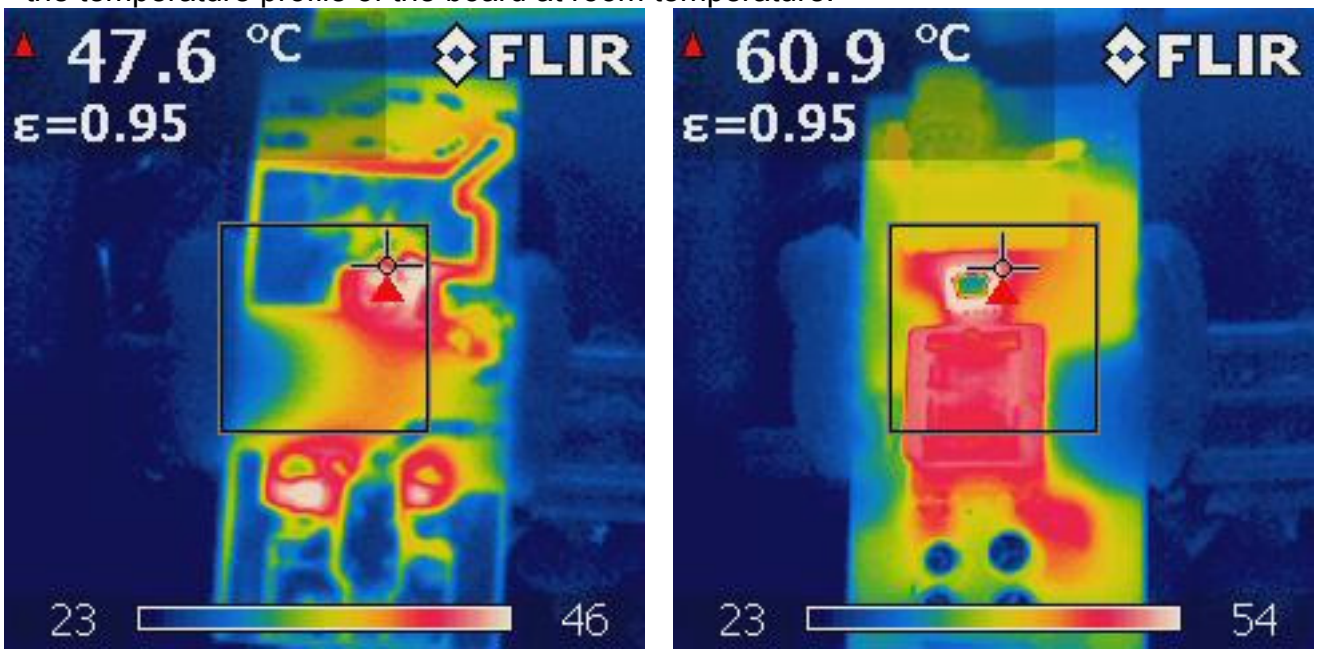

Figure 24 – Top (Right) and Bottom (left) Side Thermal Images at 265 VAC, Full Load, Room Temperature.

Table below shows the temperature of key components at 40 °C .The power supply was sealed into a box first, and the box was placed into a thermal chamber with 40 °C ambient. Temperatures of LinkSwitch-HP SOURCE pin and cathode pin of the output diode were measured at system full load (18 V/0.67 A, 5 V/1 A average). Temperature was recorded after the thermal reading was stable.

Temperature measurements of key components were taken using T-type (Copper-Constantan) thermocouples. The thermocouples were soldered directly to a SOURCE pin of the LNK6774V device and to the cathode of the output rectifier. The thermocouples were glued to the external core and to winding surfaces of the transformer.

The unit was sealed inside a large box to eliminate any air currents. The ambient temperature outside the box was raised to 40 °C. The unit was then operated at full load (5 V, 1 A and 18 V 0.67 A) and the temperature measurements were taken after they stabilized for 1 hour at 40 °C.

Temperature (°C)		
Item	**90 VAC**	**265 VAC**
LN6774V (U1)	76	79
5 V Output Diode	63	63
18 V Output Diode	61	61
Transformer	61	68

These results show that the IC has an acceptable rise in temperature.

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11 Waveforms

11.1 Drain Voltage and Current, Normal Operation

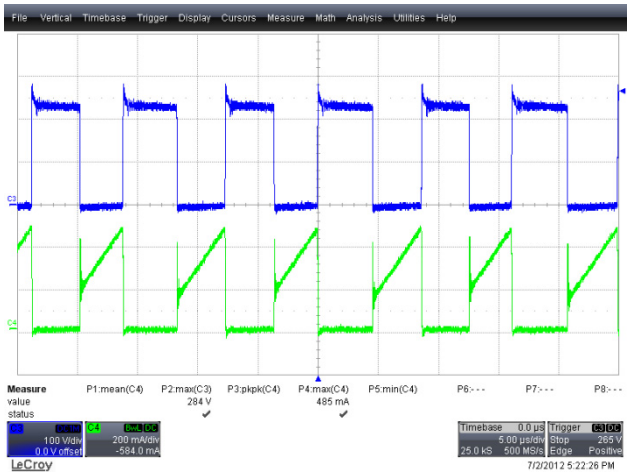

Figure 25 – 90 VAC, Full Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 5 µs / div.

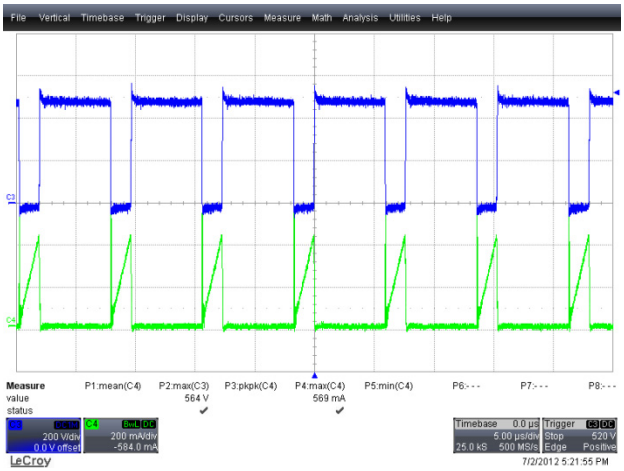

Figure 26 – 265 VAC, Full Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.2 A, 5 µs / div.

11.2 Drain Voltage and Current Start-up Profile

Drain and current profile during startup was tested with 5 V average 1 A load and 18 V no-load, since the power supply always start up into 18 V no load based on the specification. 5 V was tested with the dynamic load specified in the specification.

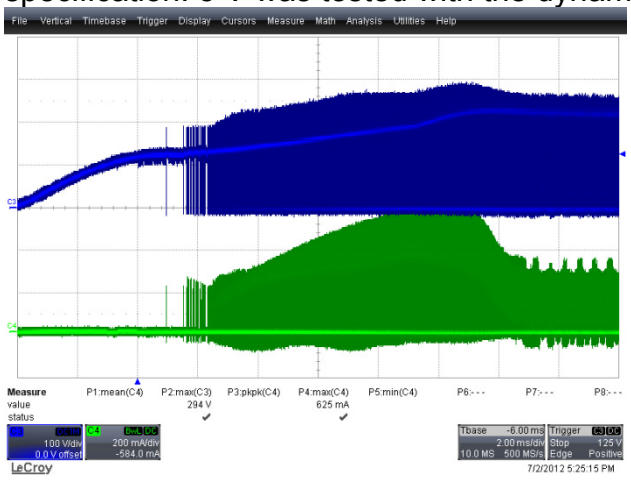

Figure 27 – 90 VAC, 5 V Dynamic, 18 V No-Load.
Upper: V_{DRAIN}, 100 V / div.
Lower: I_{DRAIN}, 0.2 A, 2 ms / div.

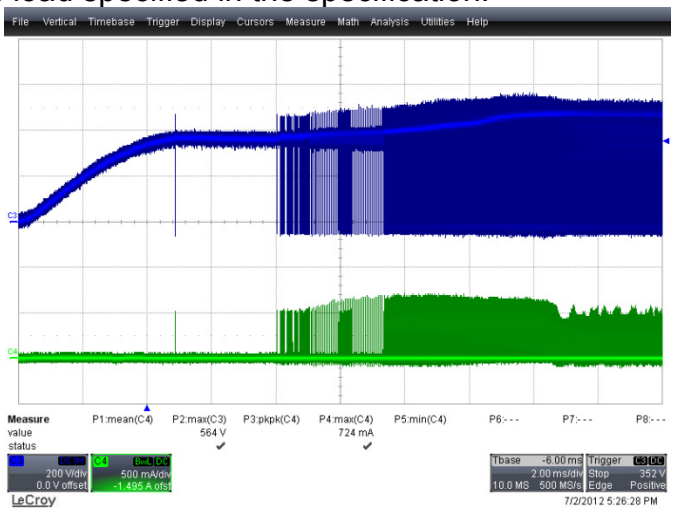

Figure 28 – 265 VAC 5 V Dynamic, 18 V No-Load.
Upper: V_{DRAIN}, 200 V / div.
Lower: I_{DRAIN}, 0.5 A, 2 ms / div.

11.3 Output Voltage Start-up Profile with Input Voltage

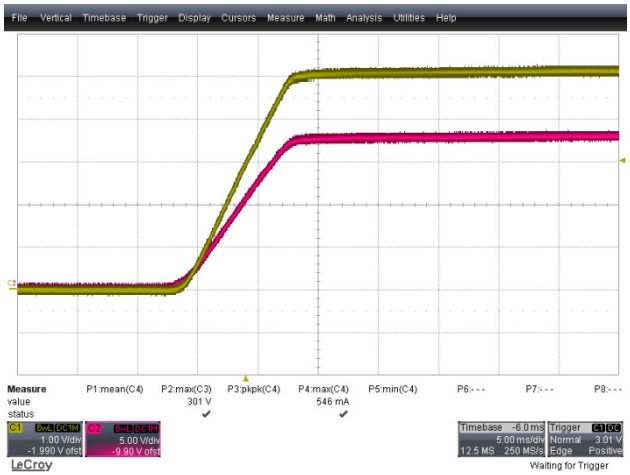

Figure 29 – Start-up Profile, 90 VAC, Standby Load.
Upper: V_{OUT}, 5 V, 1 V / div.
Lower: V_{OUT}, 18 V, 5 V, 5 ms / div.

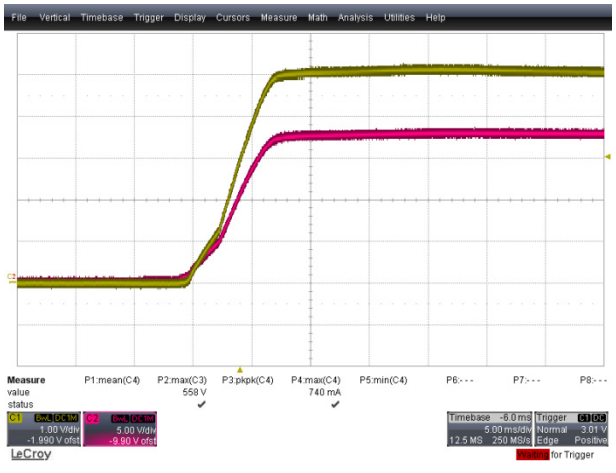

Figure 30 – Start-up Profile, 265 VAC, Standby Load.
Upper: V_{OUT}, 5 V, 1 V / div.
Lower: V_{OUT}, 18 V, 5 V, 5 ms / div.

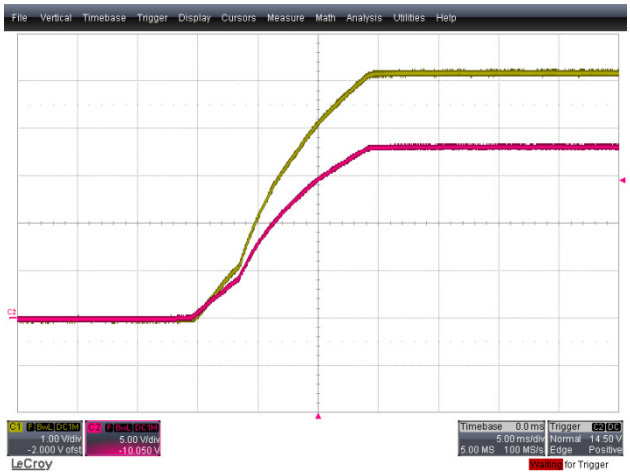

Figure 31 – Start-up Profile, 90 VAC, Full CC Load.
Upper: V_{OUT}, 5 V, 1 V / div.
Lower: V_{OUT}, 18 V, 5 V, 5 ms / div.

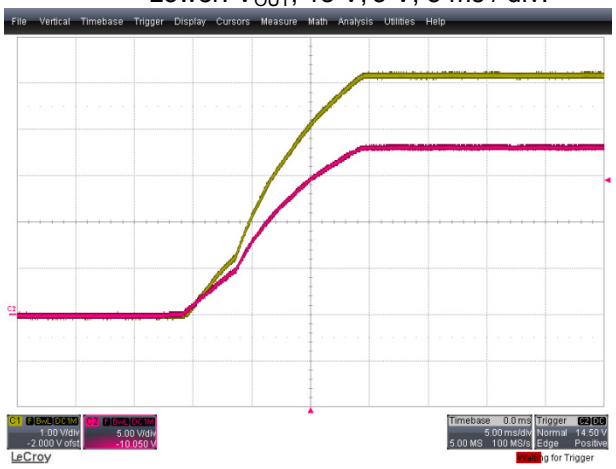

Figure 32 – Start-up Profile, 265 VAC, Full CC Load.
Upper: V_{OUT}, 5 V, 1 V / div.
Lower: V_{OUT}, 18 V, 5 V, 5 ms / div.

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11.4 5 V Load Transient Response

11.4.1 5 V Transient Tested with 5 V 500 mA to 1500 mA Step Load and Fixed 18 V, 0.67 A DC Load

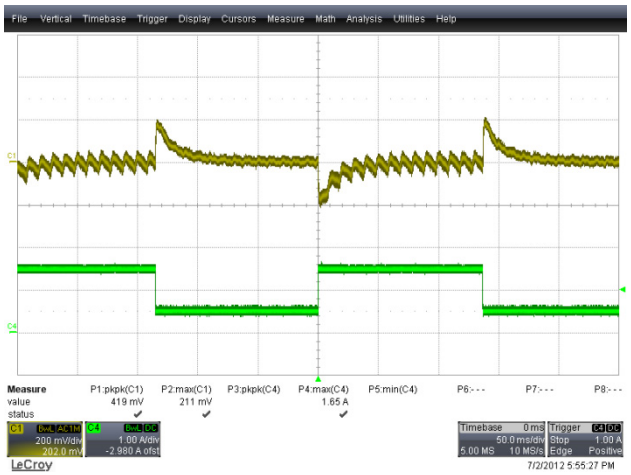

Figure 33 – 90 VAC, 18 V 0.67 A.
Upper: V_{OUT}, 5 V, 200 mV / div.
Lower: I_{OUT}, 5 V, 1 A, 50 ms / div.

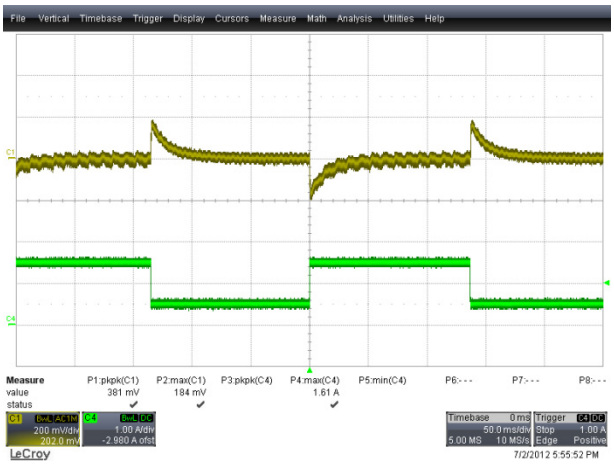

Figure 34 – 115 VAC, 18 V 0.67 A.
Upper: $V_{OUT,}$ 5 V, 200 mV / div.
Lower: I_{OUT}, 5 V, 1 A, 50 ms / div.

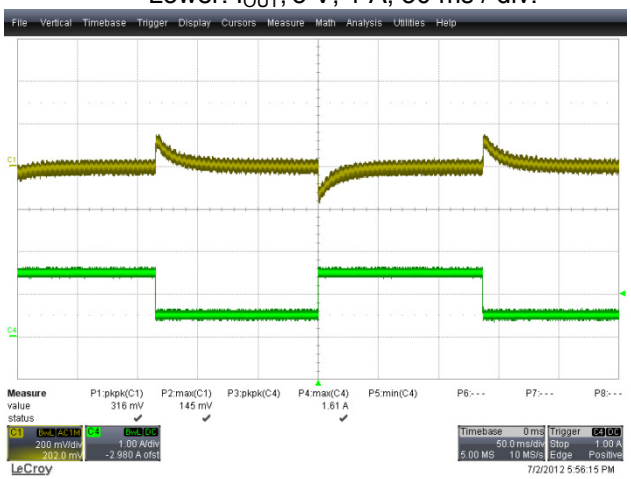

Figure 35– 230 VAC, 18 V 0.67 A.
Upper: V_{OUT}, 5 V, 200 mV / div.
Lower: I_{OUT}, 5 V, 1 A, 50 ms / div.

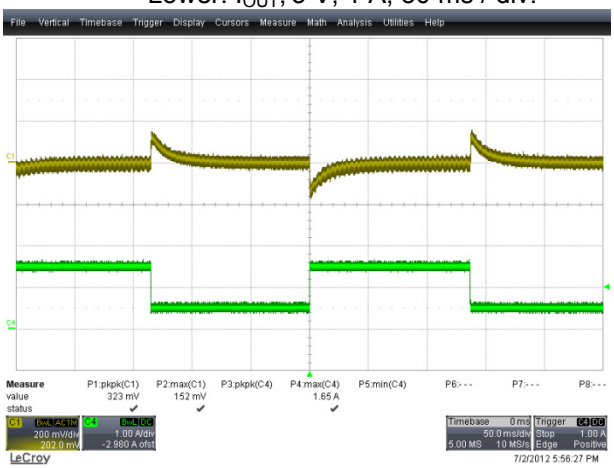

Figure 36 – 265 VAC, 18 V 0.67 A.
Upper: V_{OUT}, 5 V, 200 mV / div.
Lower: I_{OUT}, 5 V, 1 A, 50 ms / div.

11.4.2 5 V Transient Tested with Specified Load Profile

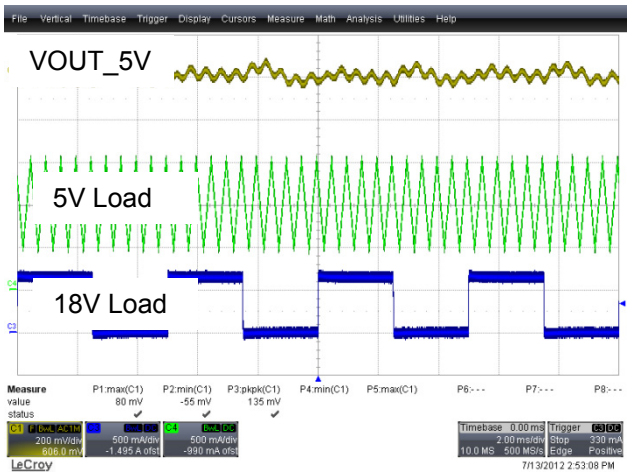

Figure 37 – 90 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: V_{OUT}, 5 V, 100 mV / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

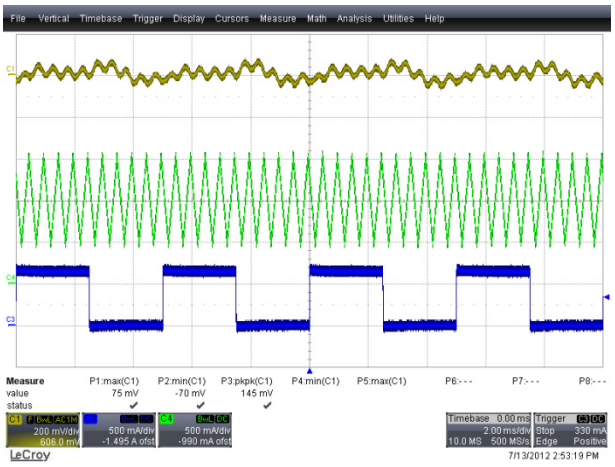

Figure 38 – 115 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: $V_{OUT,}$ 5 V, 100 mV / div.
Lower: $I_{OUT,}$ 18 V, 0.5 A, 5 ms / div.

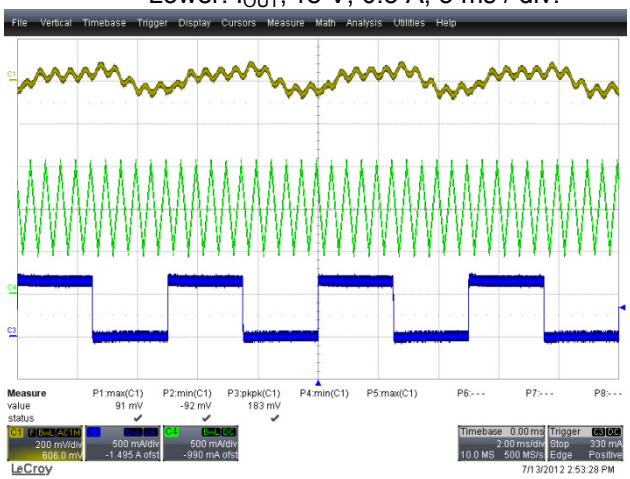

Figure 39 – 230 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.67 A Step Load.
Upper: V_{OUT}, 5 V, 100 mV / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

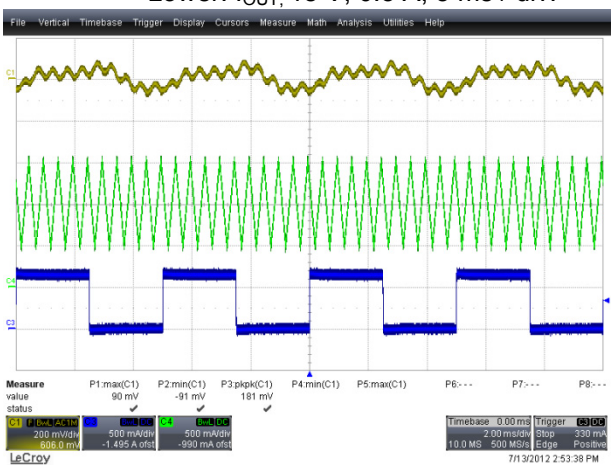

Figure 40 – 265 VAC, 5 V 1 A Dynamic Load and 18 V 0 to 0.6 A Step Load.
Upper: V_{OUT}, 5 V, 100 mV / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

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11.4.3 18 V Transient Tested with Specified Load Profile

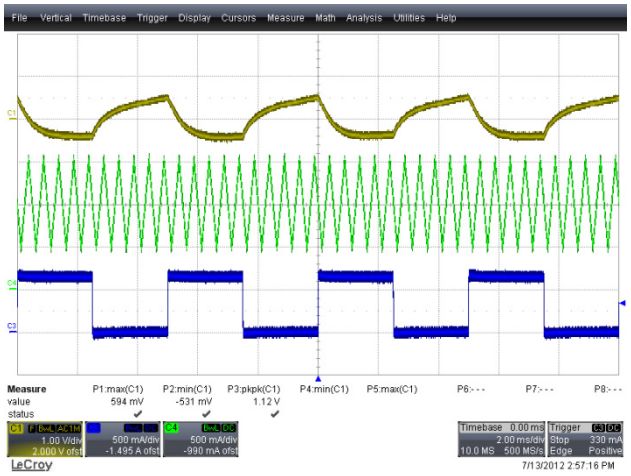

Figure 41 – 90 VAC, 5 V 1 A Average Load.
Upper: V_{OUT}, 18 V, 1 V / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

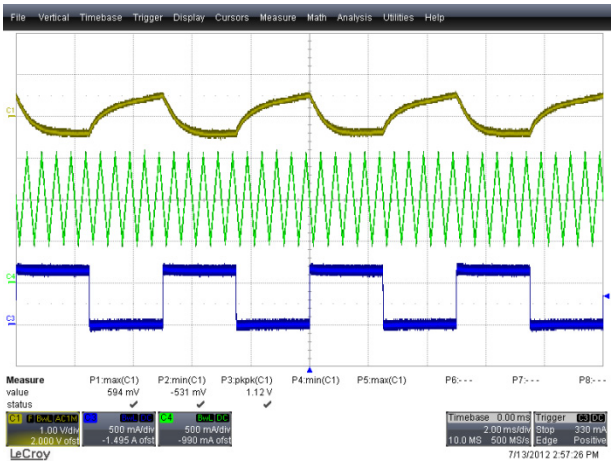

Figure 42 – 115 VAC, 5 V 1 A Average Load.
Upper: V_{OUT}, 18 V, 1 V / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

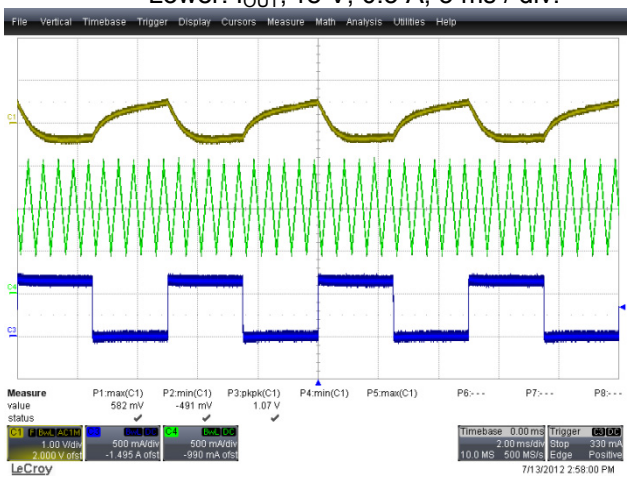

Figure 43 – 230 VAC, 5 V 1 A Average Load.
Upper: V_{OUT}, 18 V, 1 V / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

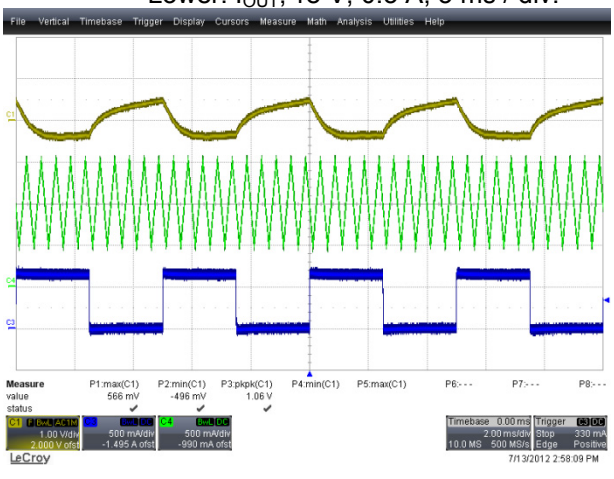

Figure 44 – 265 VAC, 5 V 1 A Average Load.
Upper: V_{OUT}, 18 V, 1 V / div.
Lower: I_{OUT}, 18 V, 0.5 A, 5 ms / div.

11.5 Output Ripple and Noise Measurements

11.5.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the figures below.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 1.0 μF / 50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

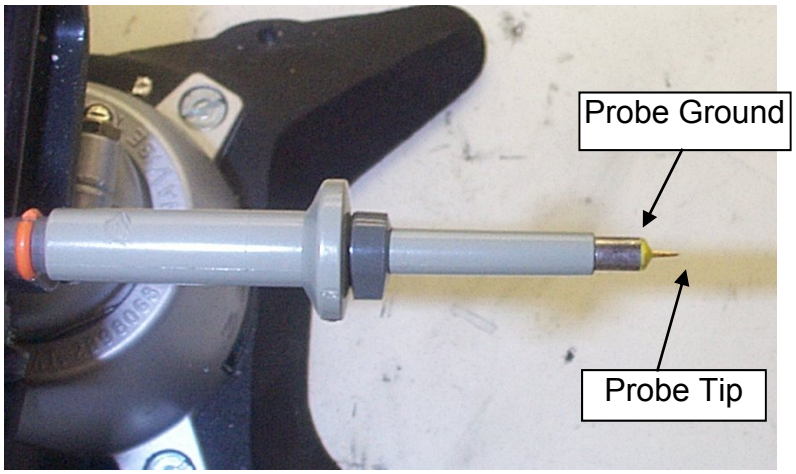

Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement.
(End Cap and Ground Lead Removed).

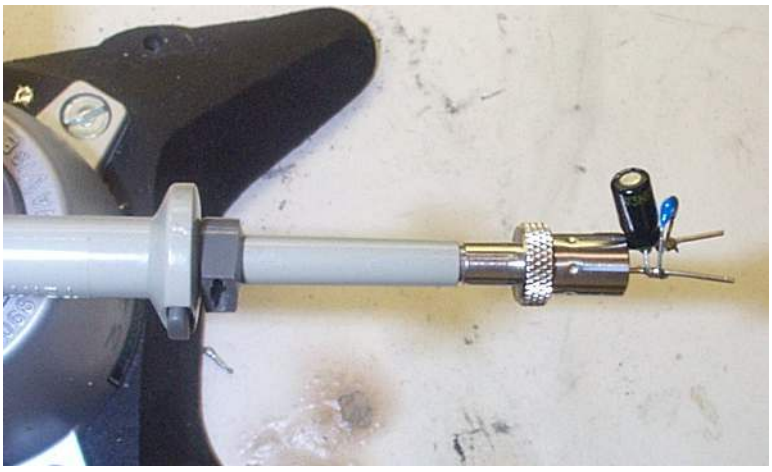

Figure 46 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added).

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11.5.2 Ripple of 18 V Tested at 18 V Maximum Load and 5 V 1 A Steady Load.

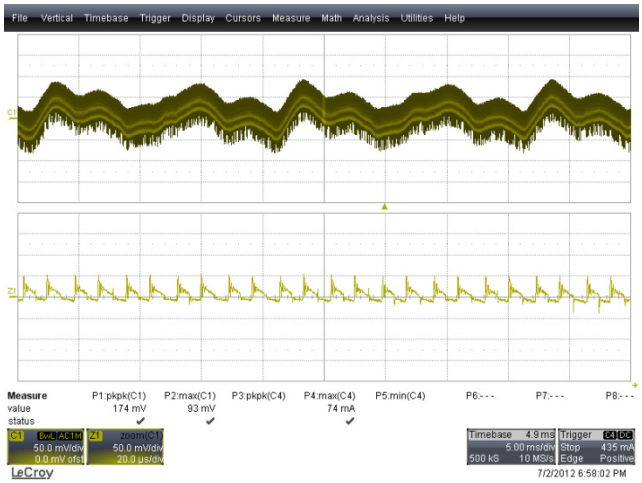

Figure 47 – 18 V Ripple, 90 VAC, Full Load.
Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
Lower: 18 V_{RIPPLE}, 20 µs, 50 mV / div.

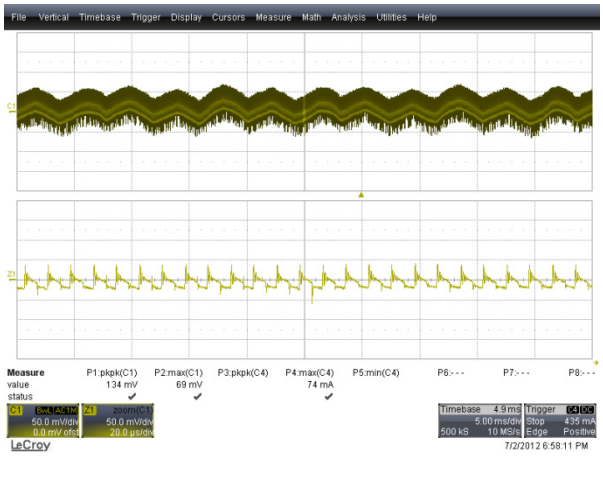

Figure 48 – 18 V Ripple, 115 VAC, Full Load.
Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
Lower: 18 V_{RIPPLE}, 20 µs, 50 mV / div.

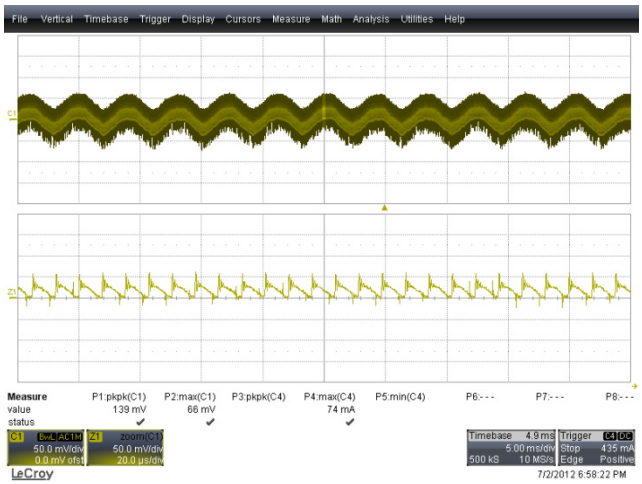

Figure 49 – 18 V_{RIPPLE}, 230 VAC, Full Load.
Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
Lower: 18 V_{RIPPLE}, 20 µs, 50 mV / div.

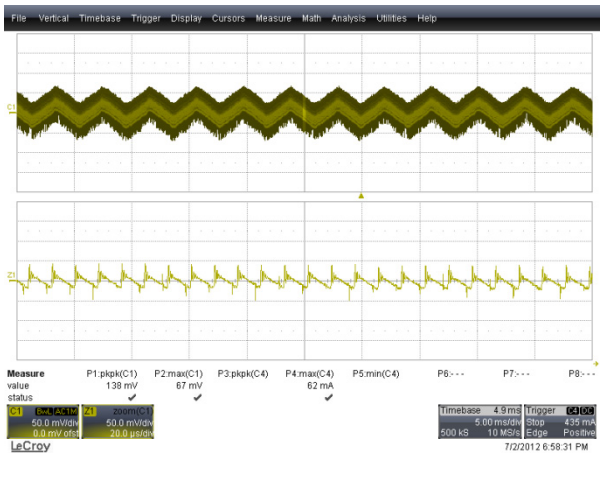

Figure 50 – 18 V_{RIPPLE}, 265 VAC, Full Load.
Upper: 18 V_{RIPPLE}, 5 ms, 50 mV / div.
Lower: 18 V_{RIPPLE}, 20 µs, 50 mV / div.

11.5.3 Ripple of 5 V Tested at 18 V Maximum Load and 5 V 1 A Steady Load

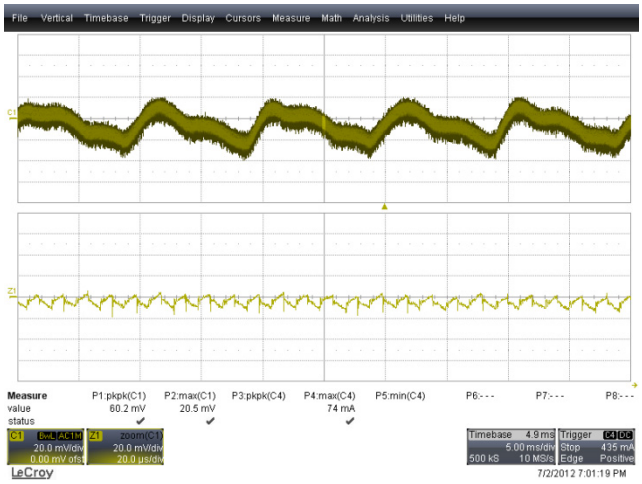

Figure 51 – Output Ripple, 90 VAC, Full Load.
Upper: 5 V_{RIPPLE}, 5 ms, 20 mV / div.
Lower: 5 V_{RIPPLE}, 20 µs, 20 mV / div.

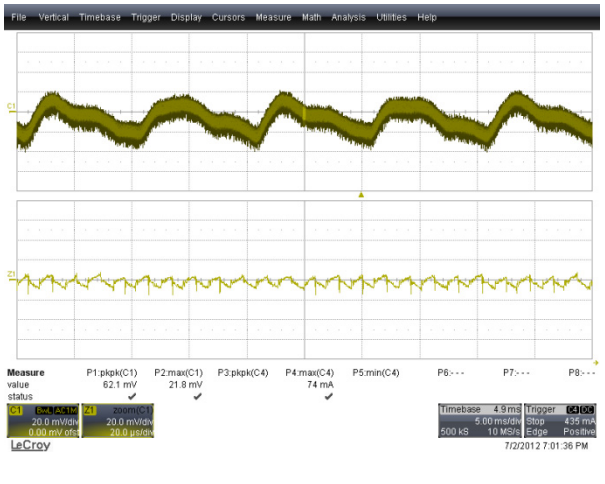

Figure 52 – Output Ripple, 115 VAC, Full Load.
Upper: 5 V_{RIPPLE}, 5 ms, 20 mV / div.
Lower: 5 V_{RIPPLE}, 20 µs, 20 mV / div.

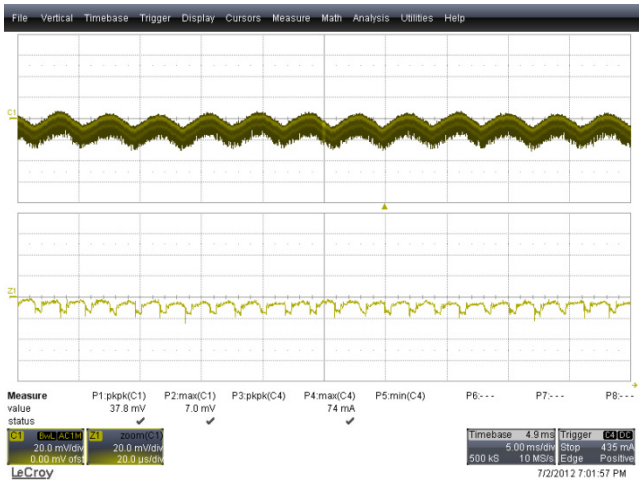

Figure 53 – Output Ripple, 230 VAC, Full Load.
Upper: 5 V_{RIPPLE}, 5 ms, 20 mV / div.
Lower: 5 V_{RIPPLE}, 20 µs, 20 mV / div.

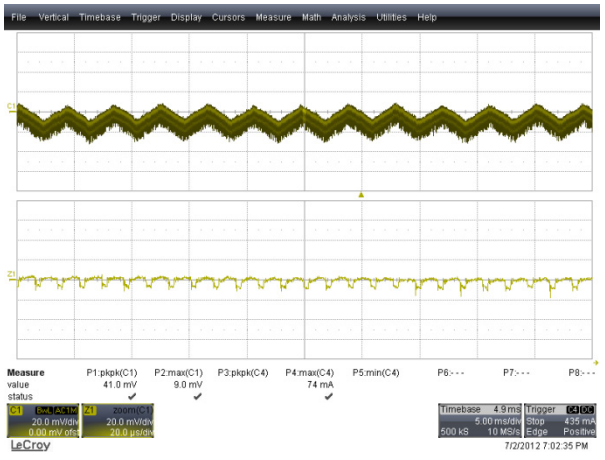

Figure 54 – Output Ripple, 265VAC, Full Load.
Upper: 5 V_{RIPPLE}, 5 ms, 20 mV / div.
Lower: 5 V_{RIPPLE}, 20 µs, 20 mV / div.

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12 Protection Feature

12.1 Auto-Restart under Short-Circuit Condition

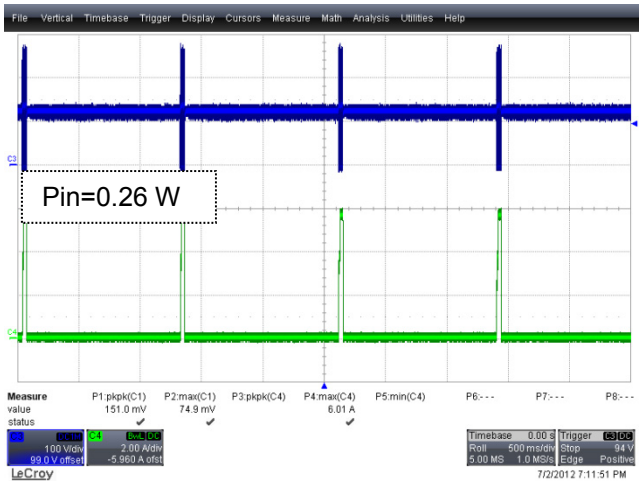

Figure 55 – Short-Circuit, 90 VAC.
Upper: V_{DS}, 100 V / div.
Lower: 5 V_{LOAD}, 500 ms, 2 A / div.

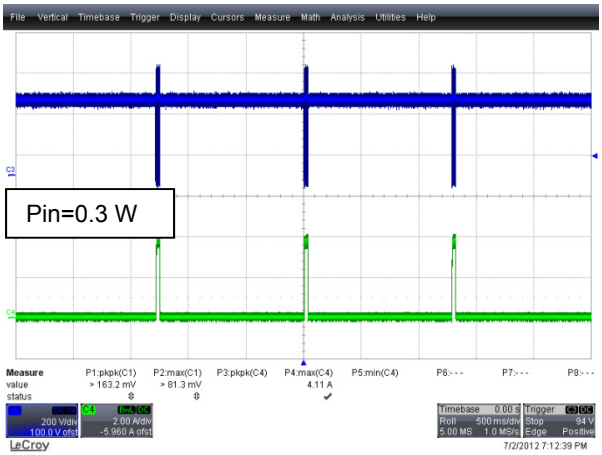

Figure 56 – Short-Circuit, 265 VAC.
Upper: V_{DS}, 200 V / div.
Lower: 5 V_{LOAD}, 500 ms, 2 A / div.

12.2 Output Overvoltage Protection

Output OVP was tested by connecting a 100 kΩ resistor between CP pin and BP pin output.

Figure 57 – Output OVP, 265 VAC, Standby Load.
V_{OUT}, 5 V, 1 V, 500 ms / div.

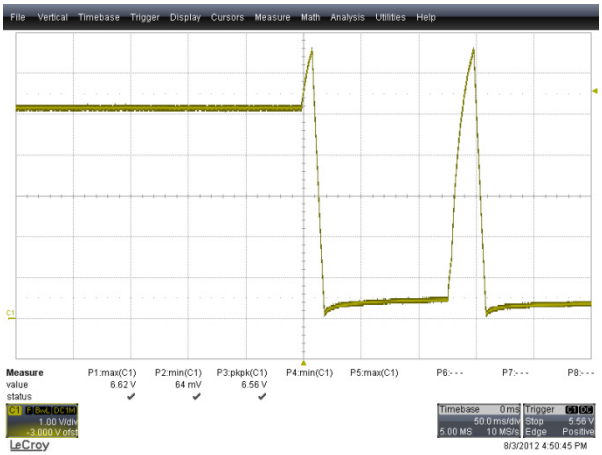

Figure 58 – Output OVP, 265 VAC, Full Load.
V_{OUT}, 5 V, 1 V, 50 ms / div.

12.3 Brown- In and Brown-Out Test

At full load, AC input was transient from 0 VAC to 120 VAC for brown-in test and from 120 VAC to 0 VAC for brown-out test. Slew rate of input voltage is 12 VAC/S for brown-in and brown-out test.

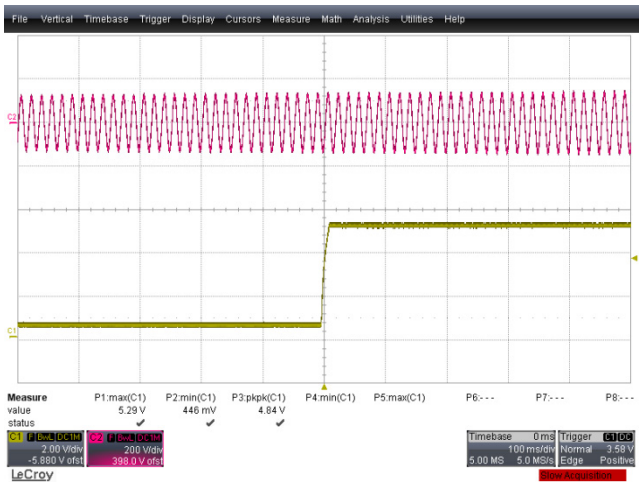

Figure 59 – Brown-In Test, Full Load.
Upper: VAC, 200 V / div.
Lower: 5 V_{OUT}, 2 V, 100 ms / div.

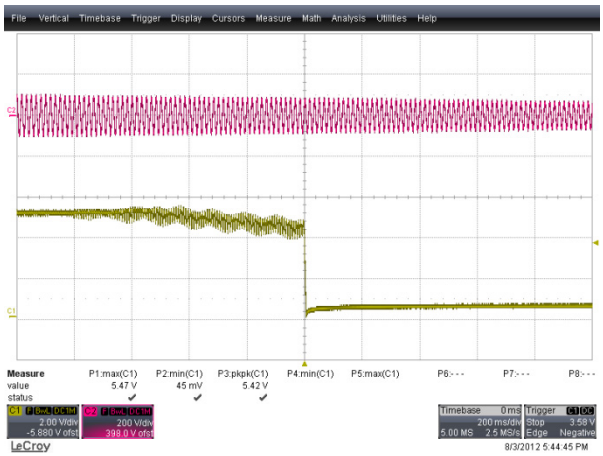

Figure 60 – Brown-In Test, Full Load.
Upper: VAC, 200 V / div.
Lower: 5 V_{OUT}, 2 V, 200 ms / div.

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13 Line Surge

Differential input line 1.2/50 μs surge testing was conducted on a single test unit to IEC61000-4-5. Input voltage was set at 230 VAC. Resistor loads were used for both outputs (5 V/1 A and 18 V/0.67 A). Output regulation was verified after the test.

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Results (Pass/Fail # Strikes)
D.M.		**(2Ω source)**		**10 Strikes each Level**
+1000	230	L1 to L2	90	Pass
–1000	230	L1 to L2	270	Pass
C.M.		**(12Ω source)**		
+2000	230	L1, L2 to PE	90	Pass
–2000	230	L1, L2 to PE	270	Pass

14 ESD

ESD passes at 8 KV for contact discharge and 15kV for air discharge, no output glitch and latch off was found during the test.

Device	Discharge Type	Discharge Location	Voltage	# of Events (1/sec)	Remarks
LNK6774V	Contact	+ Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
		- Output Terminal	+8 kV	10	PASS
			-8 kV	10	PASS
	Air	+ Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS
		- Output Terminal	+15 kV	10	PASS
			-15 kV	10	PASS

15 EMI Tests at Full Load

At 115 VAC and 230 VAC, conducted emissions tests were performed at full load (0.67A DC load for 18 V and 1 A DC load for 5 V). Composite EN55022B / CISPR22B conducted limits are shown. All the tests show excellent EMI performance.

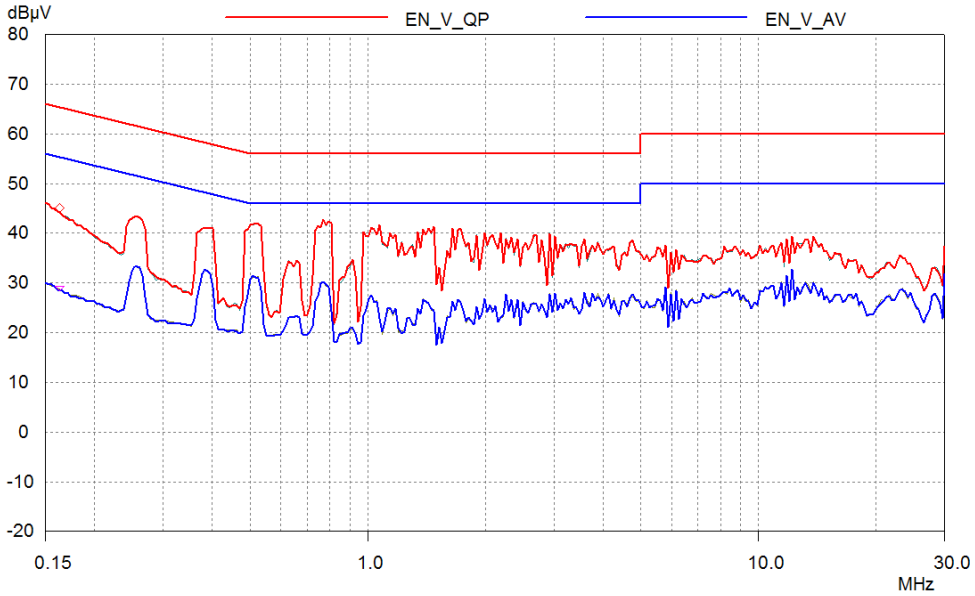

Figure 61 – Conducted EMI at 115 VAC 60 Hz, Full Load, Output Return Connected to Ground.

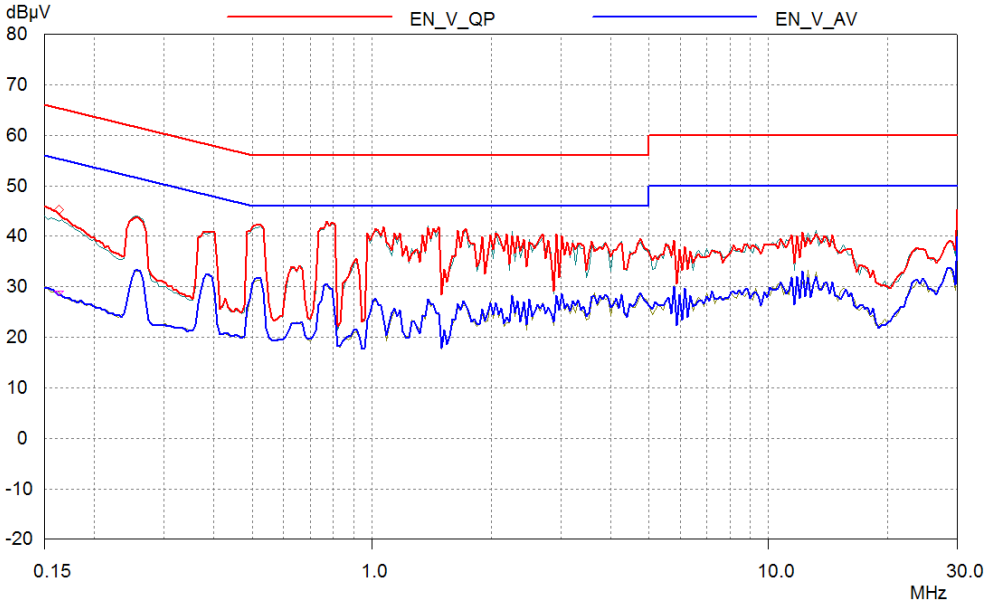

Figure 62 – Conducted EMI at 115 VAC 60 Hz, Full Load, Output Return Connected to Artificial Hand.

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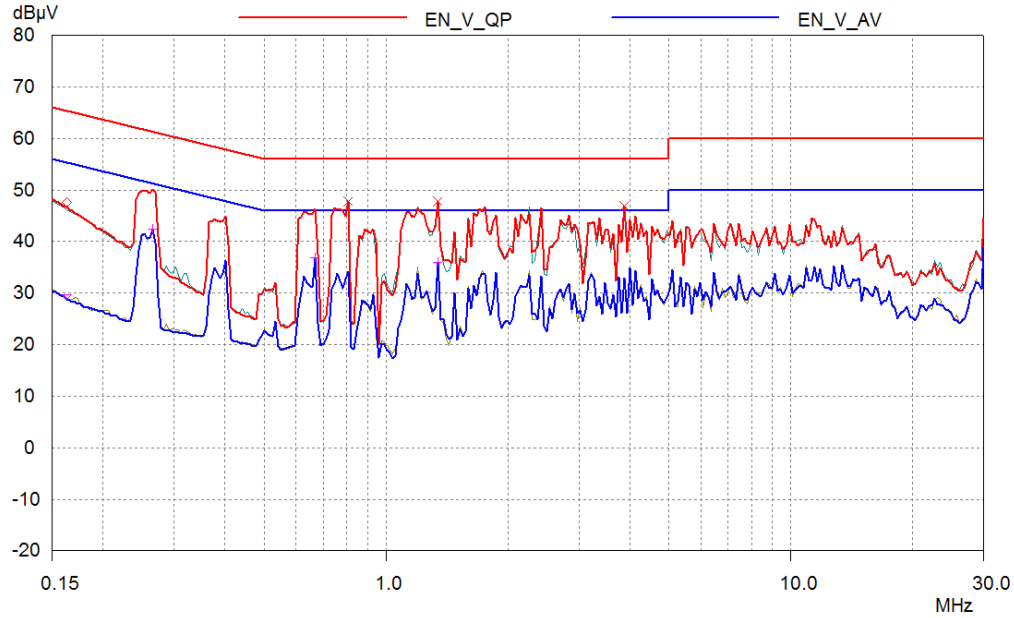

Figure 63 – Conducted EMI at 230 VAC 60 Hz, Full Load, Output Return Connected to Ground.

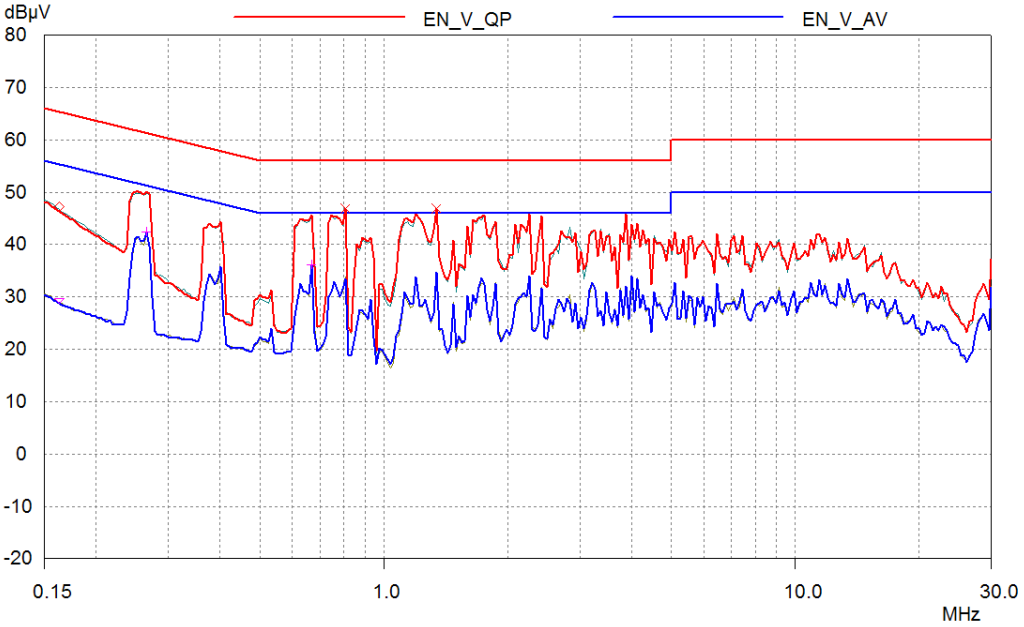

Figure 64 – Conducted EMI at 230 VAC 60 Hz, Full Load, Output Return Connected to Artificial Hand.

16 Revision History

Date	Author	Revision	Description & changes	Reviewed
28-Sep-12	KM	2.2	Initial Release	Marketing and Apps

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