



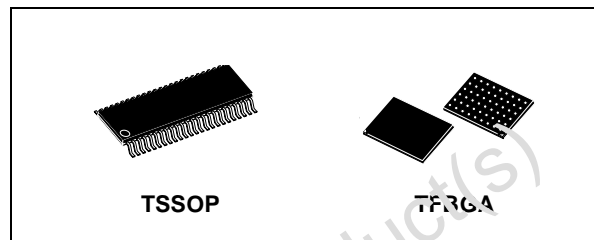
74LVTH16244

LOW VOLTAGE BICMOS 16 BIT BUS BUFFER WITH BUS HOLD AND POWER UP 3-STATE

- HIGH SPEED:
 $t_{PD} = 3.2\text{ns}$ (MAX.) at $T_A = 85^\circ\text{C}$ $V_{CC} = 3.0\text{V}$
- LOW POWER DISSIPATION HIGH LEVEL OUTPUT: $I_{CC} = 190\mu\text{A}$ (MAX.) at $T_A = 85^\circ\text{C}$
- OUTPUT IMPEDANCE:
 $I_{OH} = 32\text{mA}$, $I_{OL} = 64\text{mA}$ (MIN at $V_{CC} = 3.0\text{V}$)
 $I_{OH} = 8\text{mA}$, $I_{OL} = 24\text{mA}$ (MIN at $V_{CC} = 2.7\text{V}$)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- COMPATIBLE WITH TTL OUTPUTS:
 $V_{IH} = 2\text{V}$ (MIN), $V_{IL} = 0.8\text{V}$ (MAX) at $V_{CC} = 2.7$ to 3.6V
- POWER-UP/DOWN 3-STATE: $I_{OZPU} = 100\mu\text{A}$ MAX at $V_{CC} = 0\text{V}$ to 1.5V , $V_{CC} = 1.5\text{V}$ to 0V , $T_A = 85^\circ\text{C}$
- BUS HOLD PROVIDED ON DATA INPUTS
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 2.7\text{V}$ to 3.6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES H16244
- LATCH-UP PERFORMANCE EXCEEDS 500mA (JESD 17)

DESCRIPTION

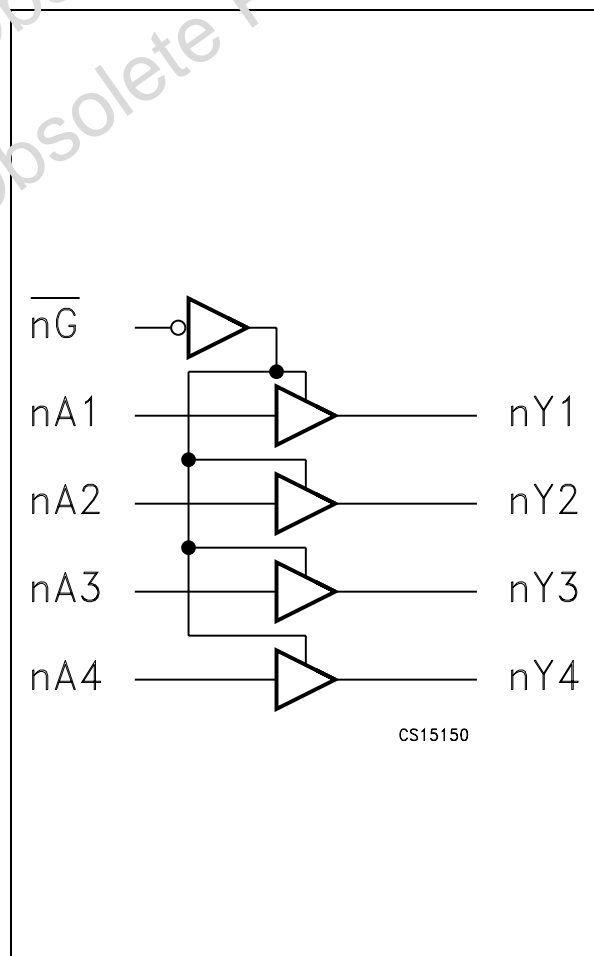
The 74LVTH16244 is a low voltage BiCMOS 16 BIT BUS BUFFER (NON-INVERTED) fabricated with sub-micron silicon gate and five-layer metal wiring BiCMOS technology. It is ideal and full specified for hot-insertion and high speed 3.3V applications; the power-up/down 3-state circuitry places the outputs in the high impedance state during power-up/down, which prevents driver conflict. This function is guaranteed when V_{CC} is between 0 and 1.5V. It can be interfaced to 3.3V signal environment for both inputs and outputs. Any \overline{nG} output control governs four BUS BUFFERS. Output Enable input (\overline{nG}) tied together gives full 16-bit operation. When \overline{nG} is LOW, the outputs are on. When \overline{nG} is HIGH, the output are in high impedance state effectively isolated. Bus hold on data inputs is provided in order to eliminate the need for external pull-up or pull-down resistors. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.



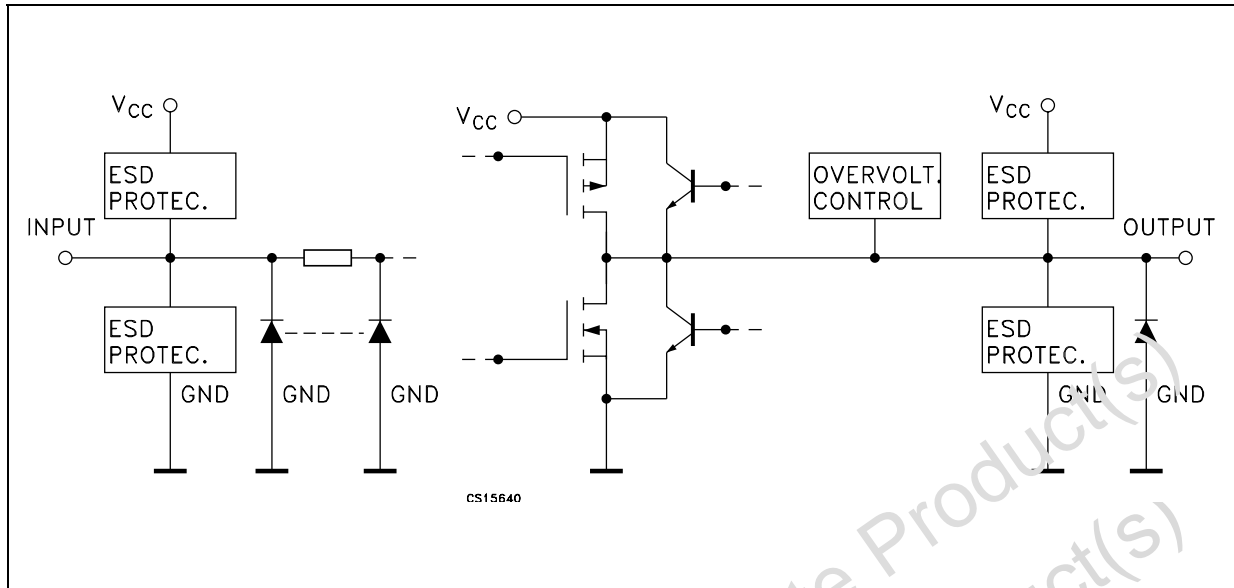
ORDER CODES

PACKAGE	T & R
TSSOP48	74LVTH16244TTR
TFBGA48	74LVTH16244LBR

LOGIC DIAGRAM



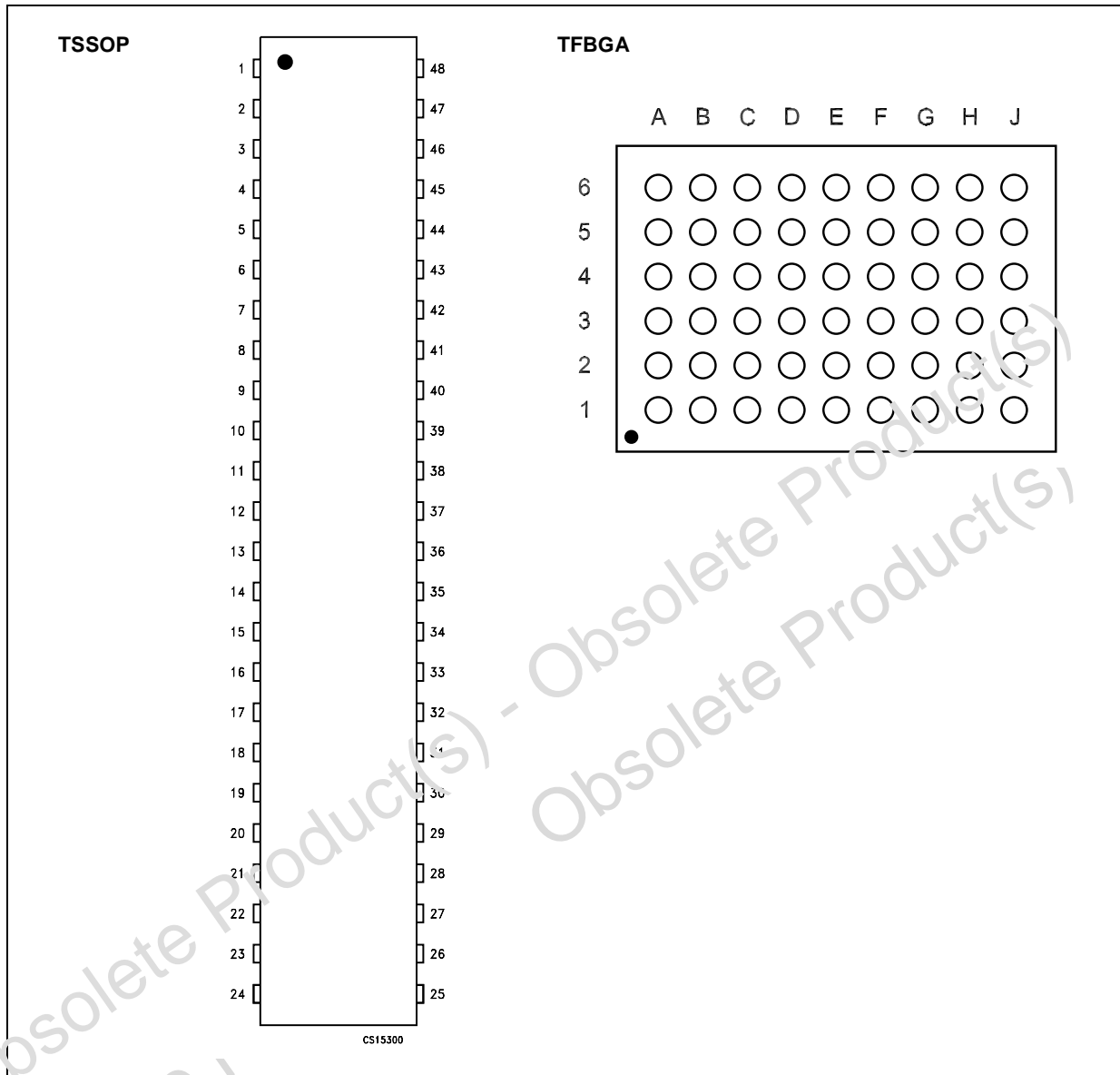
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

TFBGA PIN N°	TSSOP PIN N°	SYMBOL	NAME AND FUNCTION
A3, J3	1, 24	1G, 4G	Output Enable Inputs
A6, B5, B6, C5, C6, D5, D6, E5, E6, F5, F6, G5, G6, H5, H6, J6	47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A1-4, 2A1-4 3A1-4, 4A1-4	Data Inputs
A1, B2, B1, C2, C1, D2, D1, E2, E1, F2, F1, G2, G1, H2, H1, J1	2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Y1-4, 2Y1-4 3Y1-4, 4Y1-4	Data Outputs
J4, A4	25, 48	3G, 2G	Output Enable Inputs
D3, D4, E3, E4, F3, F4	4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
A2, A5, B3, B4, F3, F4, J2, J5	-	NC	No Connected
C4, G4, C3, G3	42, 31, 7, 18	V _{CC}	Positive Supply Voltage

PIN CONNECTION (top view for TSSOP, top through view for BGA)



TRUTH TABLE

INPUTS		OUTPUT
\overline{nG}	xAn	xYn
L	L	L
L	H	H
H	X	Z

Z = High Impedance; X = Don't care, n = 1..4, x = 1..4

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +4.6	V
V_I	DC Input Voltage	-0.5 to +4.6	V
V_O	DC Output Voltage (Output disabled)	-0.5 to +4.6	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current	- 50	mA
I_O	DC Output Current low state	128	mA
I_O	DC Output Current high state	64	mA
I_{CC}	DC V_{CC} or Ground Current	± 100	mA
P_d	Power Dissipation (*)	400	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

(*) 500mW: $\cong 65^\circ\text{C}$ derated to 300mW by 10mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2.7 to 3.6	V
V_I	Input Voltage (An, nG)	0 to 3.6	V
V_O	Output Voltage	V_{CC}	V
V_O	Output Voltage (Output Disabled)	3.6	V
T_{op}	Operating Temperature	-40 to 85	°C
dt/dV_{CC}	Minimum Power-up ramp rate	200	$\mu\text{s/V}$
dt/dv	Input Rise and Fall Time (note 1)	0 to 20	ns/V

1) V_I from 0.8V to 2.0V at $V_{CC} = 2.7$ to 3.6V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{IK}	Input Voltage Clamp (An, nG)	2.7	I _{IK} = -18mA		-0.85			-1.2	V
V _{IH}	High Level Input Voltage (An, nG)	2.7				2.0		2.0	V
		3.3 (*)				2.0		2.0	
V _{IL}	Low Level Input Voltage (An, nG)	2.7		0.8			0.8		V
		3.3 (*)		0.8			0.8		
I _I	Control Input Leakage Current	3.6	V _I = GND or V _{CC}					± 1	μA
	Data Input Leakage Current	3.6	V _I = GND or V _{CC} nG = GND					± 1	μA
I _{I(HOLD)}	Data Input Hold Current	3.0	V _I = 0.8V		135		75		μA
		3.0	V _I = 2.0V		-135		-75		
		3.6	V _I = 0 to 3.6V					± 500	
V _{OH}	High Level Output Voltage	2.7	I _O = -100 μA				2.5		V
		2.7	I _O = -8 mA				2.4		
		3.0	I _O = -32 mA				2.0		
V _{OL}	Low Level Output Voltage	2.7	I _O = 100 μA					0.2	V
		2.7	I _O = 24 mA					0.5	
		3.0	I _O = 16 mA					0.4	
		3.0	I _O = 32 mA					0.5	
		3.6	I _O = 64 mA					0.55	
I _{OZ}	High Impedance Output Leakage Current	3.6	V _O = 0.5V or 3.0V V _I = V _{IL} or V _{IH} nG = V _{CC}					± 5	μA
I _{OZPU}	High Impedance Output Leakage Current	0 to 1.5	V _O = 0.5V or 3.0V V _I = GND or V _{CC} nG = GND or V _{CC}					± 100	μA
I _{OZPD}	High Impedance Output Leakage Current	1.5 to 0	V _O = 0.5V or 3.0V V _I = GND or V _{CC} nG = GND or V _{CC}					± 100	μA
I _{OFF}	Power Off Leakage Current	0	V _I = GND to 3.6V V _O = GND to 3.6V					± 100	μA
I _{CCA}	Quiescent Supply Current	3.6	V _O = High, I _O = 0					0.19	mA
			V _O = Low, I _O = 0					5.0	
			nG = V _{CC} , I _O = 0 V _O = GND or V _{CC}					0.19	
ΔI _{CC}	Maximum Quiescent Supply Current / Input (An or nG)	3.3 (*)	V _I = V _{CC} - 0.6V An, nG = V _{CC} or GND					0.2	mA

(*) Power Supply Range V_{CC} = 3.3±0.3V

AC ELECTRICAL CHARACTERISTICS

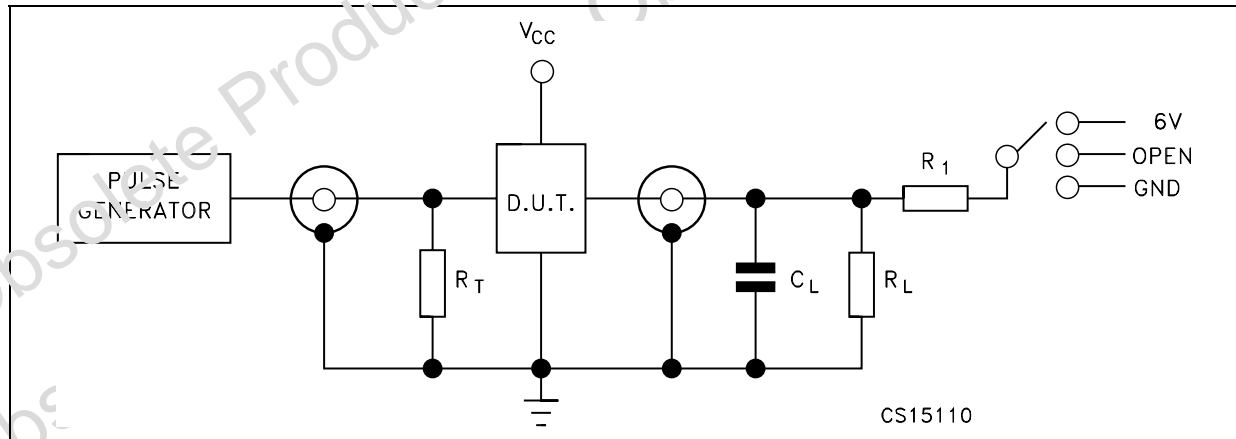
Symbol	Parameter	Test Condition	Value					Unit
			V _{CC} = 2.7V		V _{CC} = 3.3 ± 0.3V			
			Min.	Max.	Min.	Typ.	Max.	
t _{PLH}	Propagation Delay Time An to Yn	T _A = - 40 to 85 °C		3.7	1.2	2.5	3.2	ns
t _{PHL}	Propagation Delay Time An to Yn			3.7	1.2	2.5	3.2	ns
t _{PZL}	Output Enable Time nG to Yn			5.0	1.2	2.7	4.0	ns
t _{PZH}	Output Enable Time nG to Yn			5.0	1.2	2.7	4.0	ns
t _{PLZ}	Output Disable Time nG to Yn			4.4	2.0	3.7	4.2	ns
t _{PHZ}	Output Disable Time nG to Yn			5.0	2.2	4.4	5.1	ns
t _{OSLH} t _{OSHL}	Output To Output Skew Time (note1, 2)						0.5	ns

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|)
 2) Parameter guaranteed by design

CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C _I	Control Input Capacitance	open			6				pF
C _O	Output Capacitance	3.3			15				pF

TEST CIRCUIT



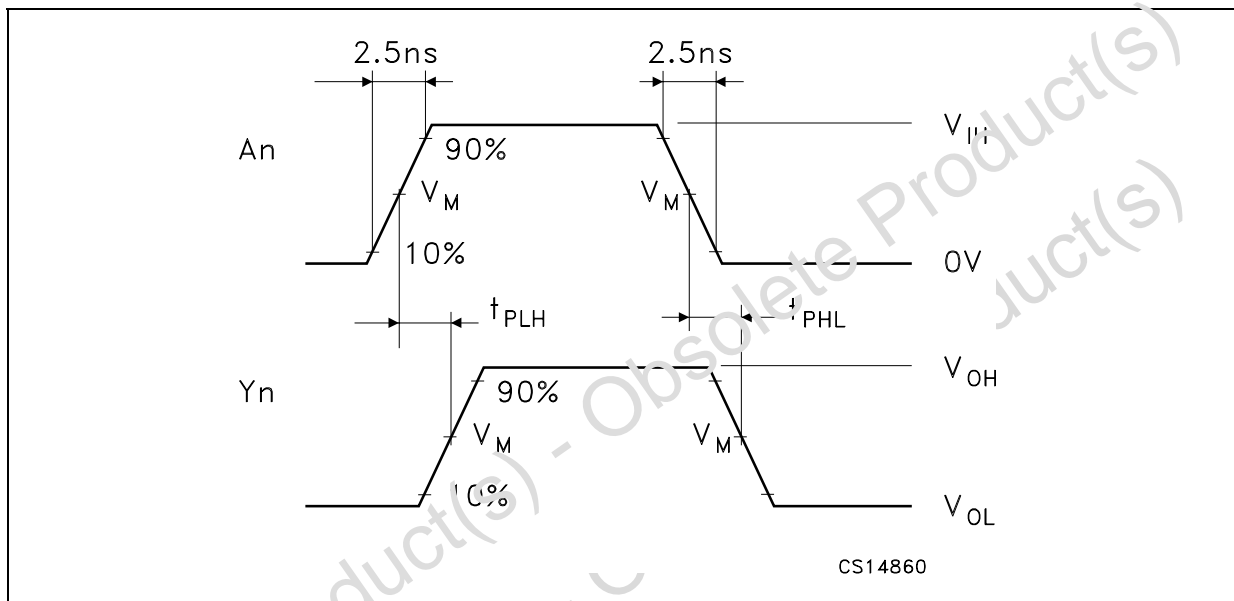
TEST	SWITCH
t _{PLH} , t _{PHL}	Open
t _{PZL} , t _{PLZ} (V _{CC} = 3.0 to 3.6V)	6V
t _{PZL} , t _{PLZ} (V _{CC} = 2.7V)	6V
t _{PZH} , t _{PHZ}	GND

C_I = 50pF or equivalent (includes jig and probe capacitance)
 R_L = R₁ = 500Ω or equivalent
 R_T = Z_{OUT} of pulse generator (typically 50Ω)

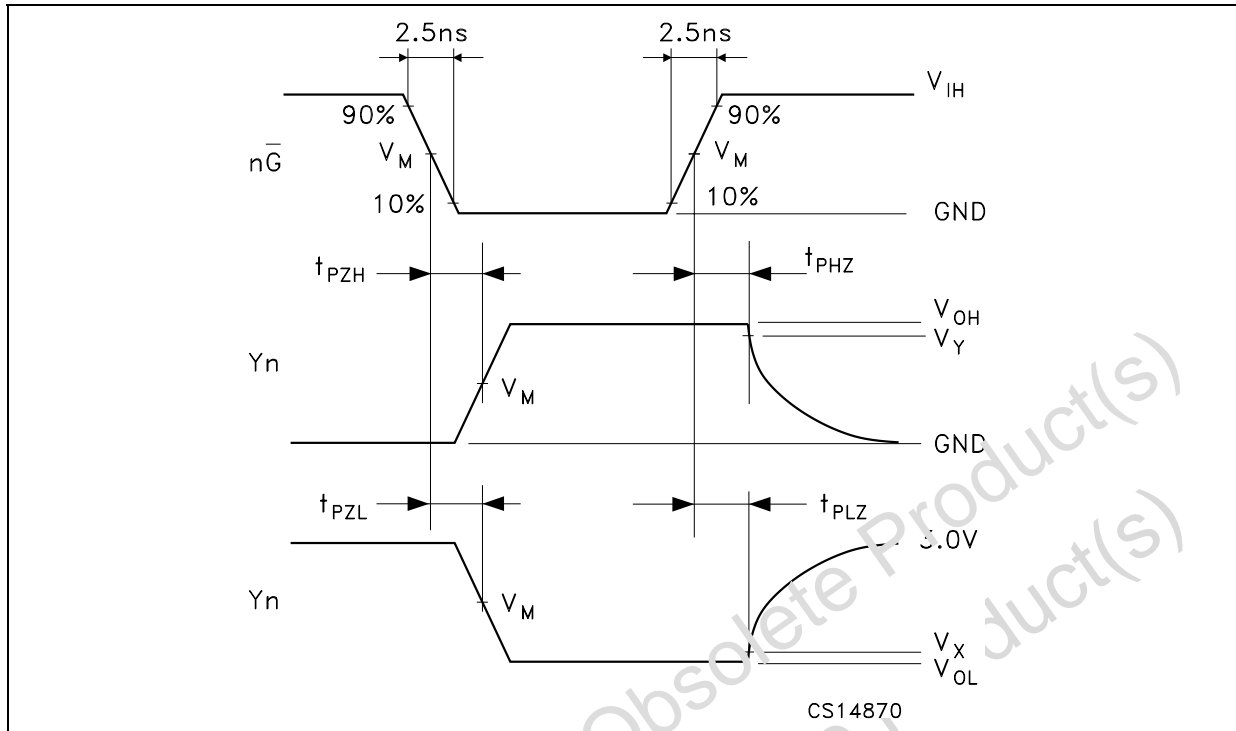
WAVEFORM SYMBOL VALUE

Symbol	V_{CC}	
	3.0 to 3.6V	2.7V
V_{IH}	2.7V	V_{CC}
V_M	1.5V	1.5V
V_X	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_Y	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

WAVEFORM 1: PROPAGATION DELAY (f=1MHz; 50% duty cycle)

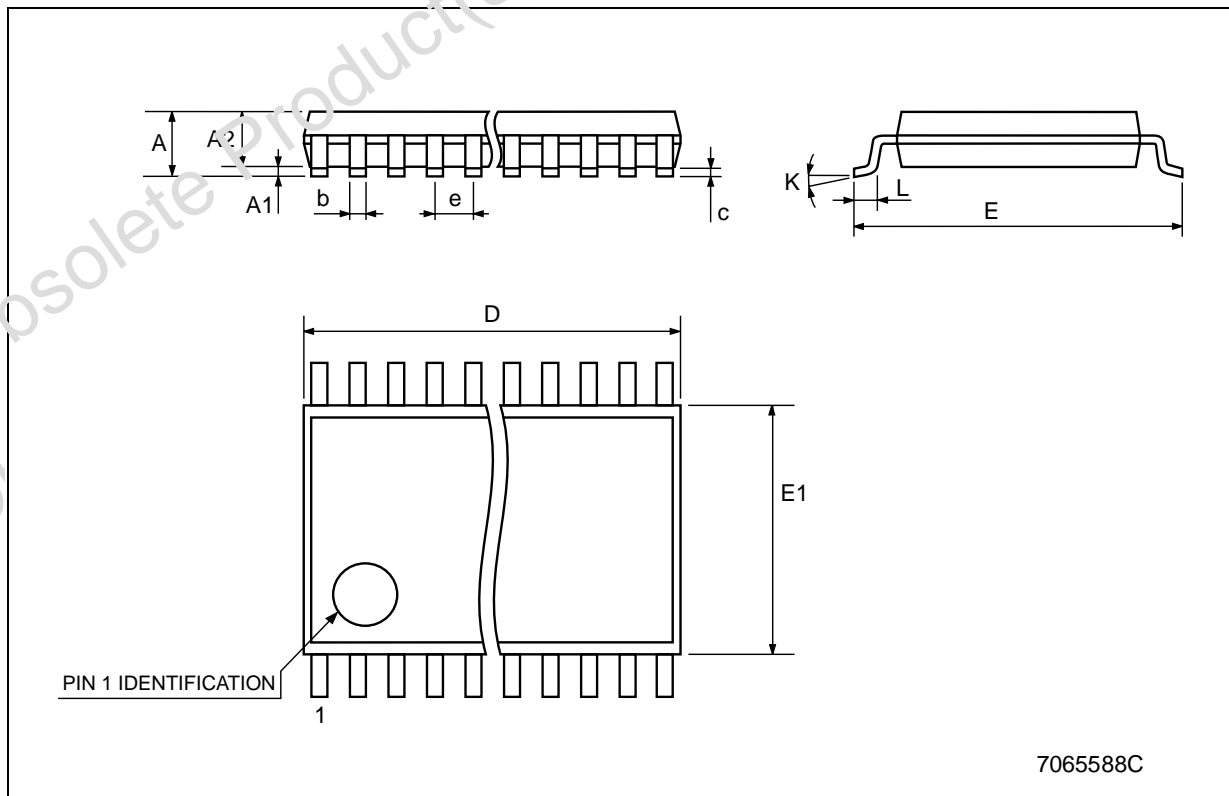


WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)



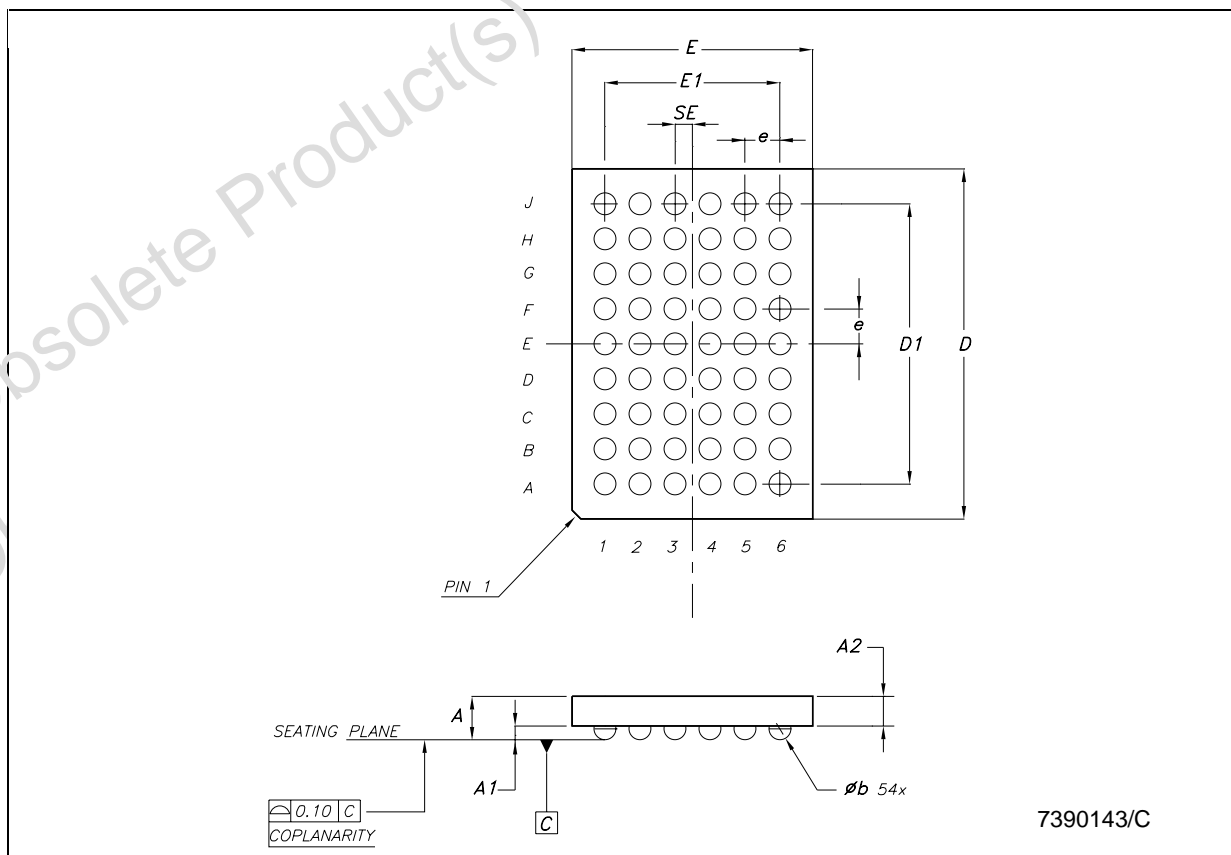
TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



TFBGA54 MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			47.2
A1	0.25			9.8		
A2	0.78		0.86	30.7		33.8
B	0.35	0.4	0.45	13.7	15.7	17.7
D	7.9		8.1	311.0		318.9
D1		6.4			253.0	
E	5.4	5.5	5.6	212.6	216.5	220.5
E1		4			157.5	
e		0.8			31.5	
SE		0.4			15.7	

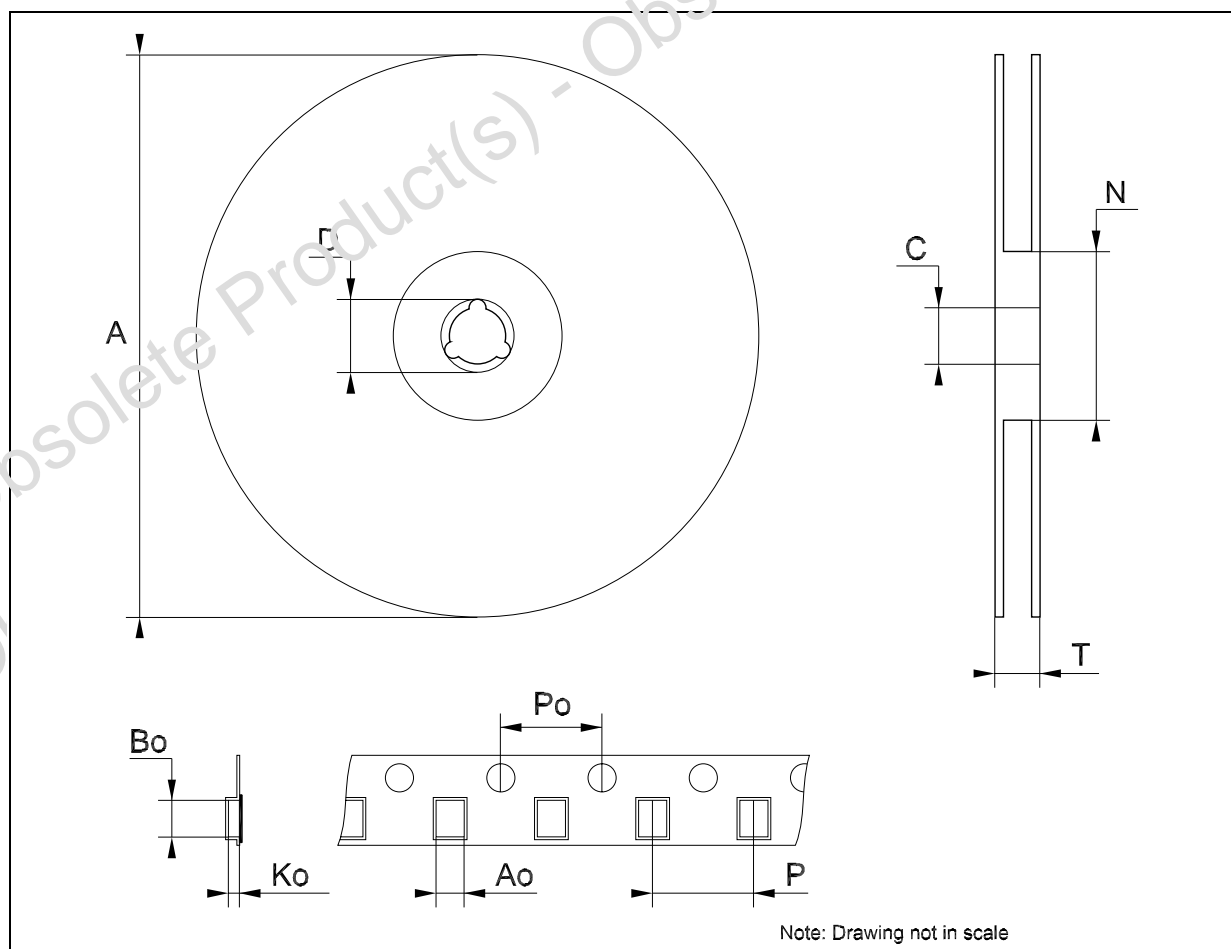


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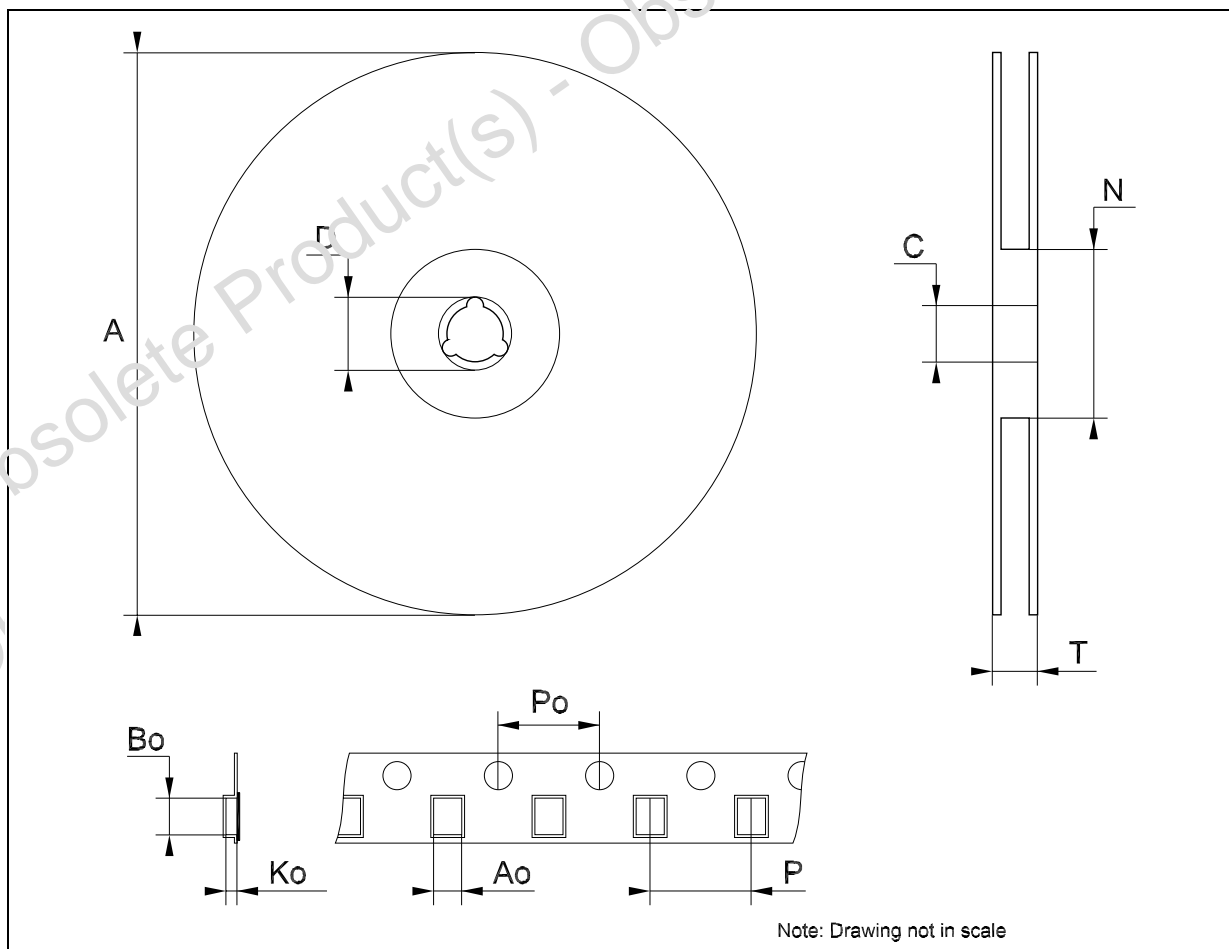
Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Tape & Reel TFBGA54 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.682
Ao		6.1			0.240	
Bo		8.6			0.339	
Ko		1.8			0.071	
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



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