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SEMICONDUCTOR M

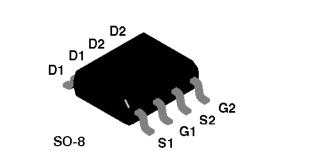
NDS9936 Dual N-Channel Enhancement Mode Field Effect Transistor

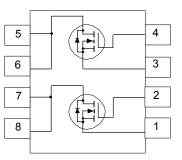
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC/DC conversion, disk drive motor control, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5A, 30V. $R_{DS(ON)} = 0.05\Omega @ V_{GS} = 10V.$
- High density cell design for extremely low R_{DS(ON)}.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





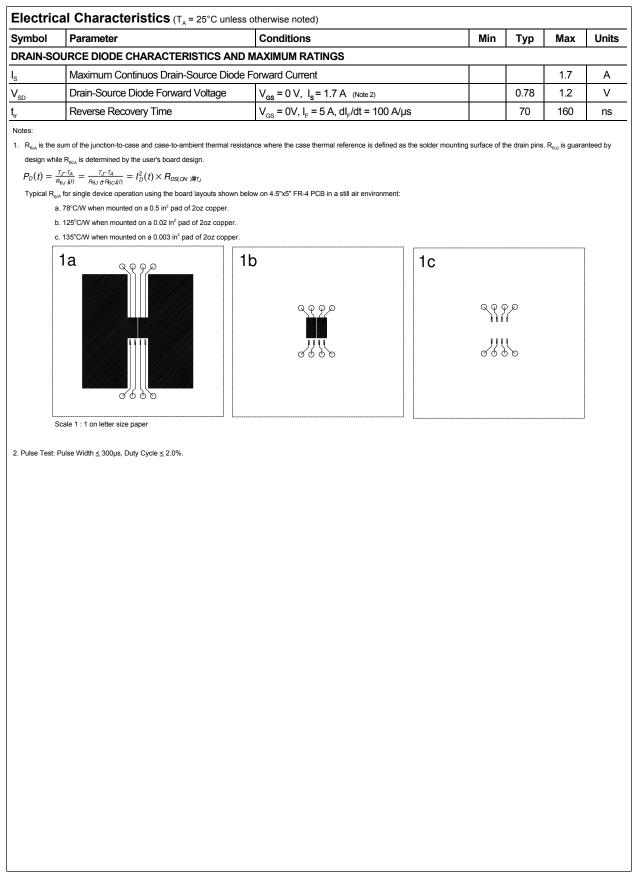
Absolute Maximum Ratings $T_A = 25^{\circ}C$ unless otherwise noted

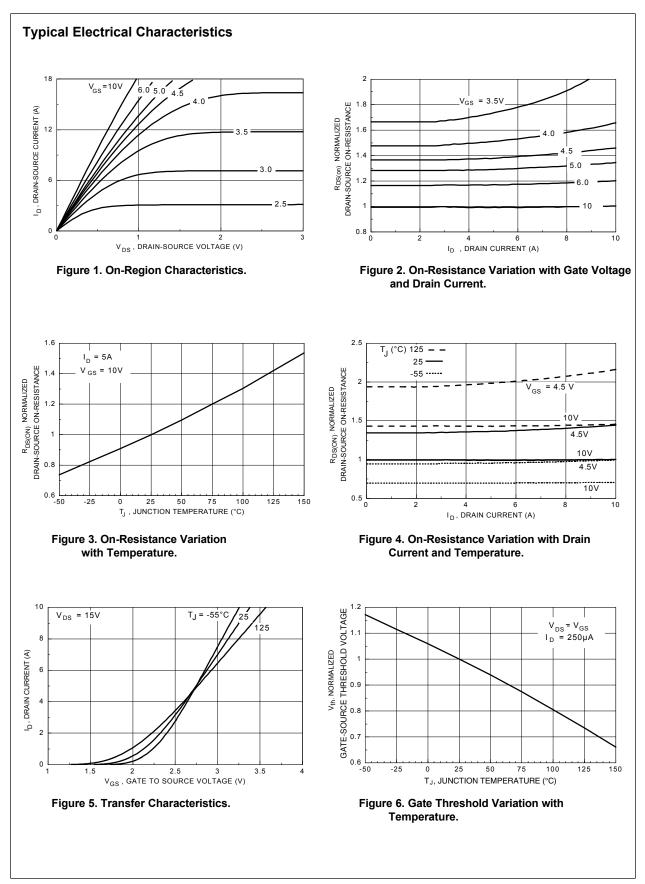
Symbol	Parameter		NDS9936	Units
V _{DSS}	Drain-Source Voltage		30	V
V _{GSS}	Gate-Source Voltage		± 20	V
I _D	Drain Current - Continuous @ $T_A = 25^{\circ}C$	(Note 1a)	± 5.0	А
	- Continuous @ $T_A = 70^{\circ}C$	(Note 1a)	± 4.0	
	- Pulsed $@T_A = 25^{\circ}C$		± 40	
P _D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_,T _{stg}	Operating and Storage Temperature Range		-55 to 150	°C
THERMA	L CHARACTERISTICS			
R _{θJA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

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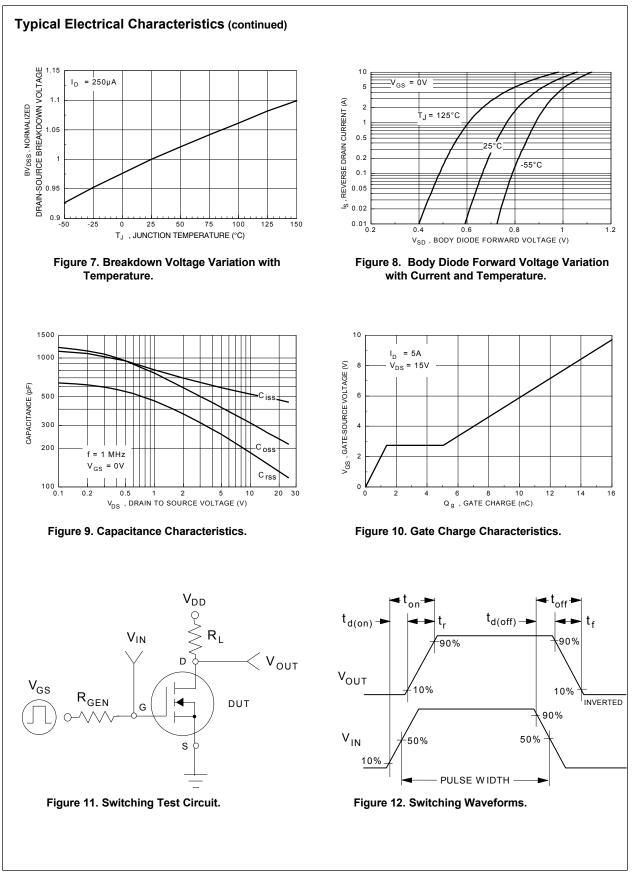
February 1996

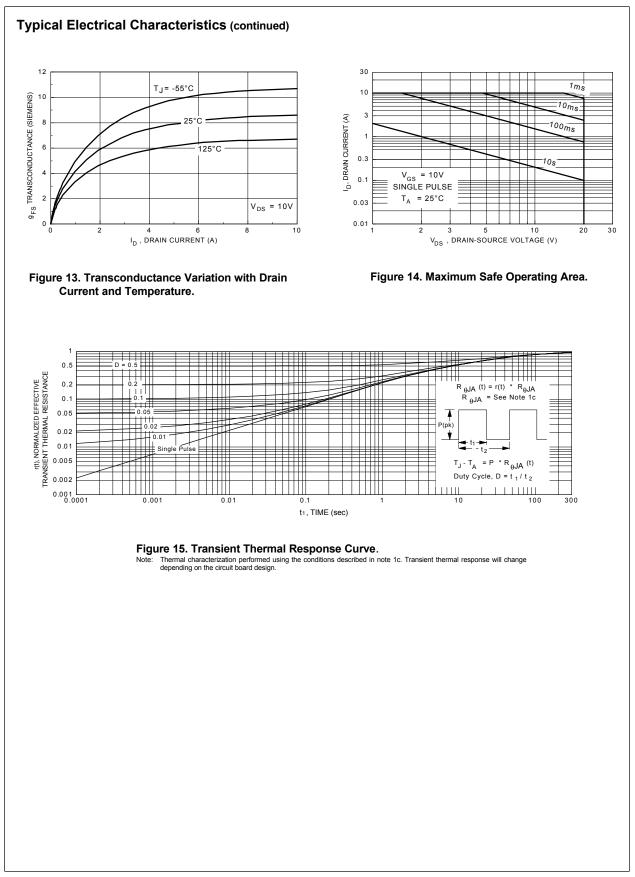
Symbol	Parameter	Conditions		Min	Тур	Max	Units
OFF CHA	RACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{gs} = 0 V, I _D = 250 μA		30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V				2	μA
			T_= 55°C			20	μA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 20 V, V _{DS} = 0 V				100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{gs} = -20 V, V _{ps} = 0 V				-100	nA
ON CHAR	ACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		1	1.4	3	V
			T _J =125°C	0.7	1.1	2.2	1
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{gs} = 10 V, I _p = 5 A			0.044	0.05	Ω
			T_=125°C		0.066	0.1	1
		V _{gs} = 4.5 V, I _p = 3.9 A			0.066	0.08	1
			T _J =125°C		0.099	0.16	1
I _{D(on)}	On-State Drain Current	V _{GS} = 10 V, V _{DS} = 10 V	= 10 V				А
		V_{GS} = 4.5 V, V_{DS} = 10 V		20			1
9 _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 3.5 A		3	8		S
DYNAMIC	CHARACTERISTICS						
C _{iss}	Input Capacitance	$V_{DS} = 15 V, V_{GS} = 0 V,$ f = 1.0 MHz			525		pF
C _{oss}	Output Capacitance				315		pF
C _{rss}	Reverse Transfer Capacitance				185		pF
SWITCHI	NG CHARACTERISTICS (Note 2)						
t _{D(ON)}	Tum - On Delay Time	$V_{DD} = 15 V, I_{D} = 1 A,$			12	30	ns
t,	Turn - On Rise Time	V_{GS} = 10 V, R_{GEN} = 6 Ω			10	25	ns
t _{D(OFF)}	Turn - Off Delay Time				25	50	ns
t _r	Turn - Off Fall Time				10	50	ns
Q _g	Total Gate Charge	V _{DS} = 15 V,			17	35	nC
Q _{gs}	Gate-Source Charge	$I_{\rm D} = 5 \text{A}, V_{\rm GS} = 10 \text{V}$			1.5		nC
Q_{gd}	Gate-Drain Charge				3.7		nC





NDS9936.SAM





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