*User's Guide*

# *TPS65279V Buck Converter Evaluation Module User's Guide*


**ABSTRACT**

This document is provided with the TPS65279V PMIC evaluation module (EVM) as a supplement to the TPS65279V datasheet. This user's guide includes the schematic, hardware setup, software installation and bill of materials (BOM).


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## Trademarks

# 1 Introduction

This document presents the information required to operate the TPS65279V PMIC as well as the support documentation including schematic, layout, hardware setup, software installation and bill of materials.

## 2 Background

The TPS65279V PMIC is designed to provide dual 5 A of continuous currents with an operational range of 4.5 to 18 V. The TPS65279V features $I^2C$ controlled voltage identification (VID) and the output voltage can be set by $I^2C$ from 0.68 V to 1.95 V. Without $I^2C$, voltage can also be programmed by an external resistor divider. The TPS65279V features externally programmed switching frequency ranging from 200 kHz to 1.6 MHz, external compensation, soft-start and enable.

As there are many possible options to set the converters, Table 2-1 presents the performance specification summary for the EVM.

**Table 2-1. Summary of Performance**

| Test Conditions | Performance |
|---|---|
| Vin = 4.5 V to 18 V | Buck1 : 1.0 V, up to 5 A, VID control |
| fsw = 500 kHz (25°C ambient) | Buck2 : 1.1 V, up to 5 A, VID control |

The EVM is designed to provide access to the features of the TPS65279V. Some modifications can be made to this module to test performance at different input and output voltages, current and switching frequency. Please contact TI Field Applications Group for advice on these matters.

# 3 TPS65279V Schematic

Figure 3-1 shows the TPS65279V PMIC EVM schematic.

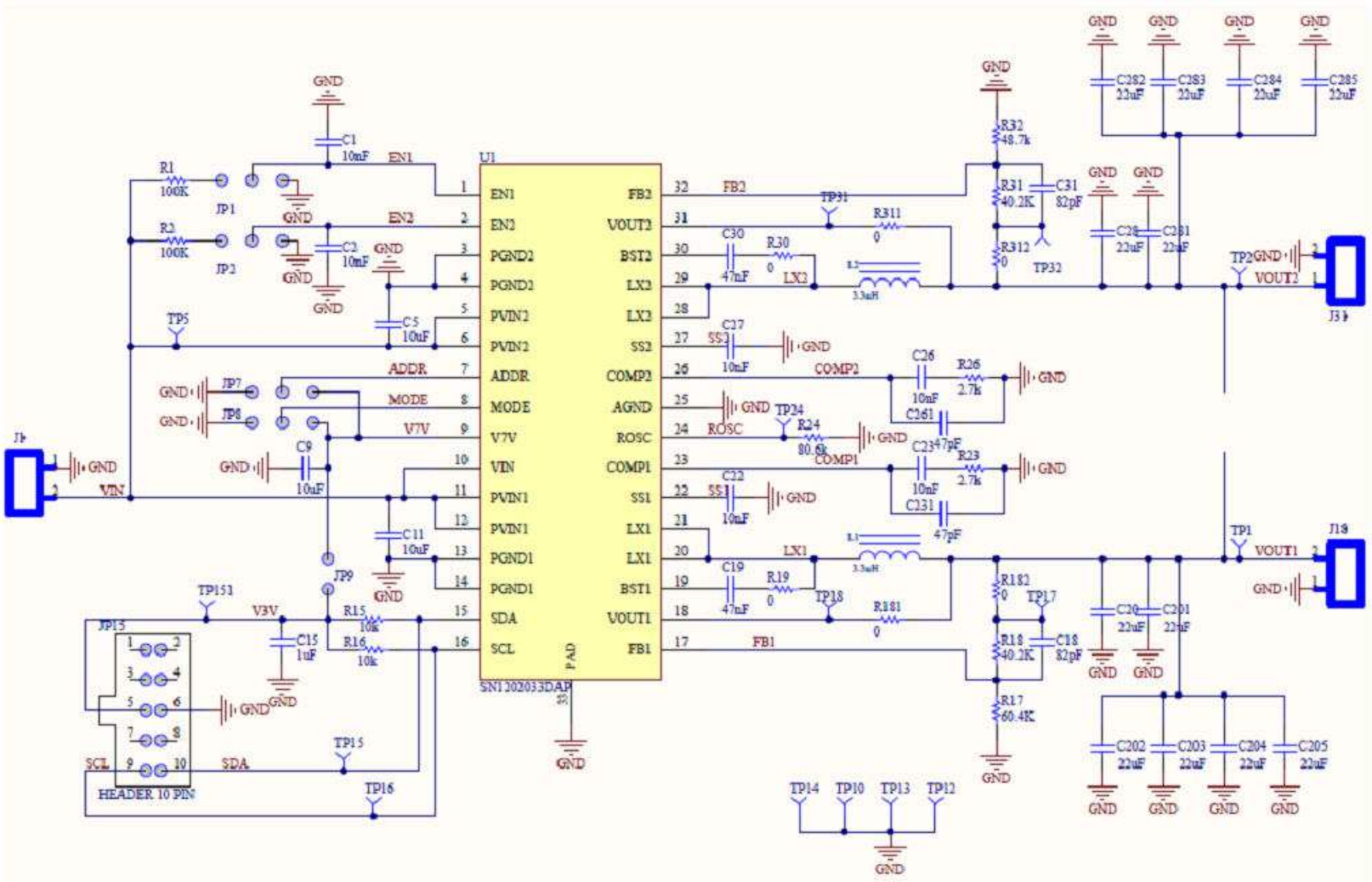



**Figure 3-1. TPS65279V Schematic**

## 4 Board Layout

Figure 4-1 through Figure 4-5 illustrate the printed-circuit boards for this EVM.

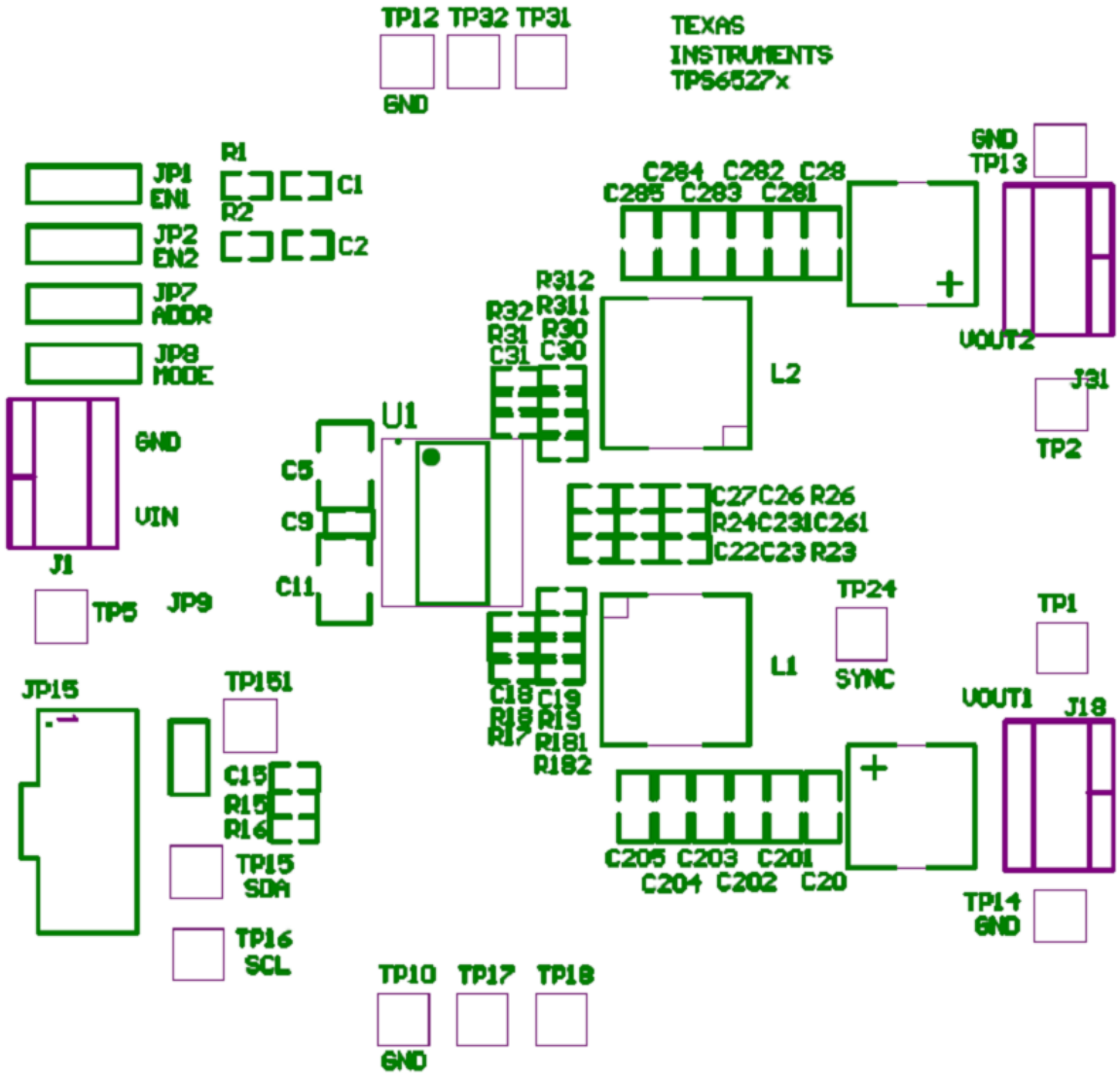



**Figure 4-1. Component Placement (Top Layer)**

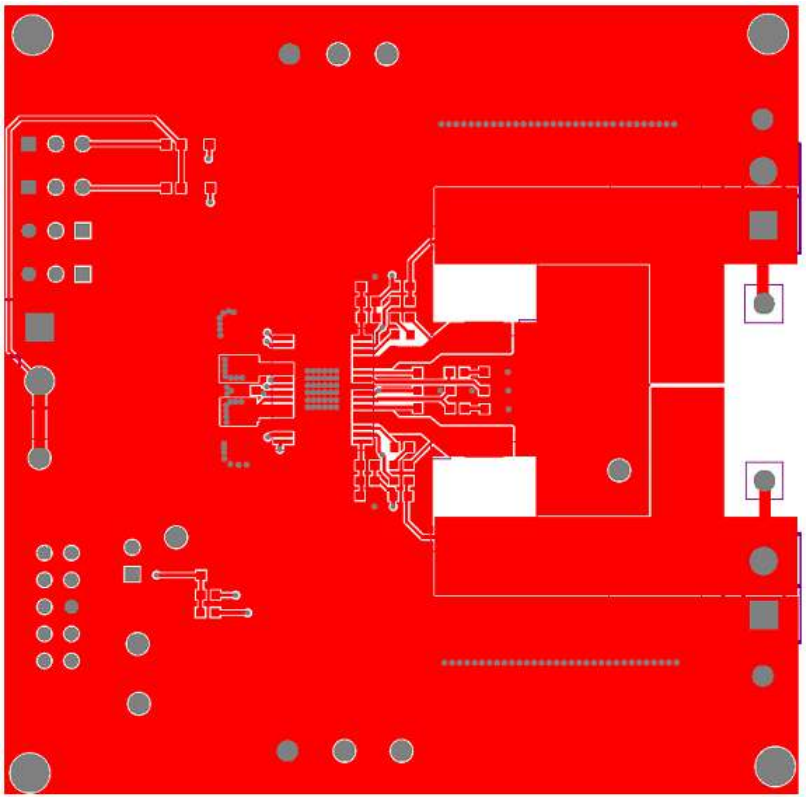


**Figure 4-2. Board Layout (Top Layer)**

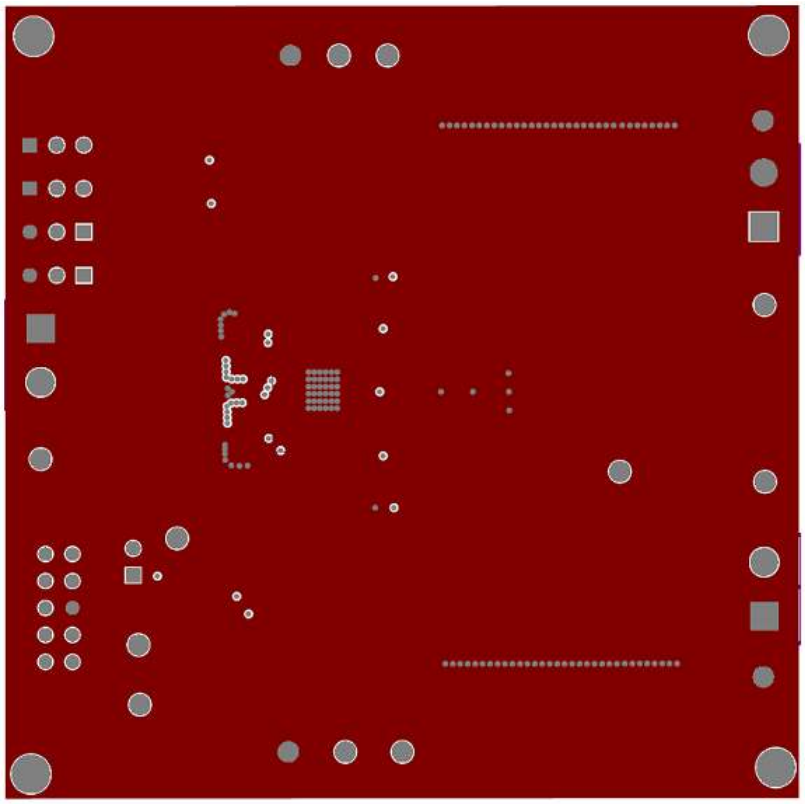


**Figure 4-3. Board Layout (Second Layer)**

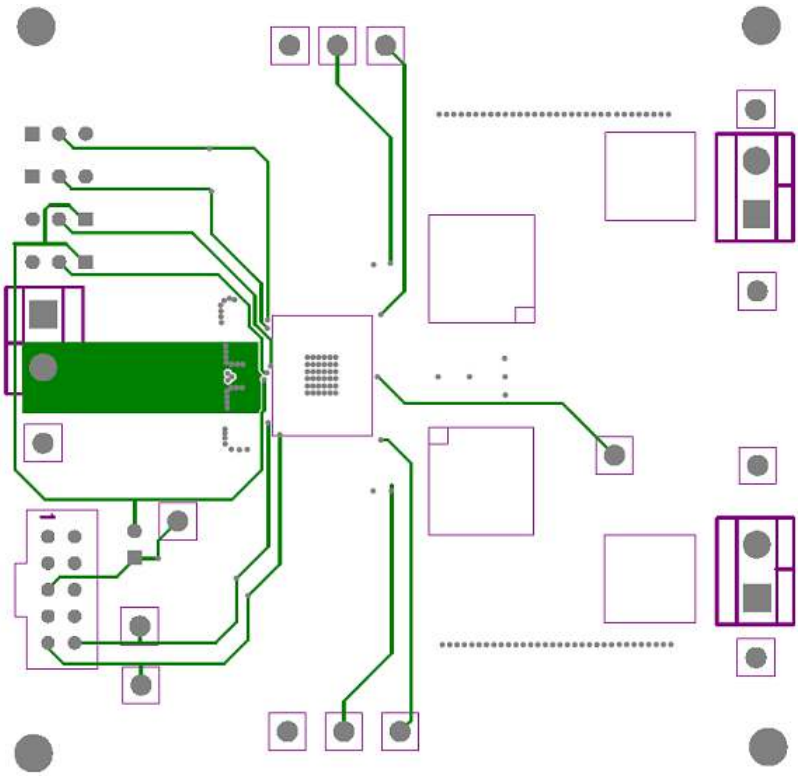


**Figure 4-4. Board Layout (Third Layer)**

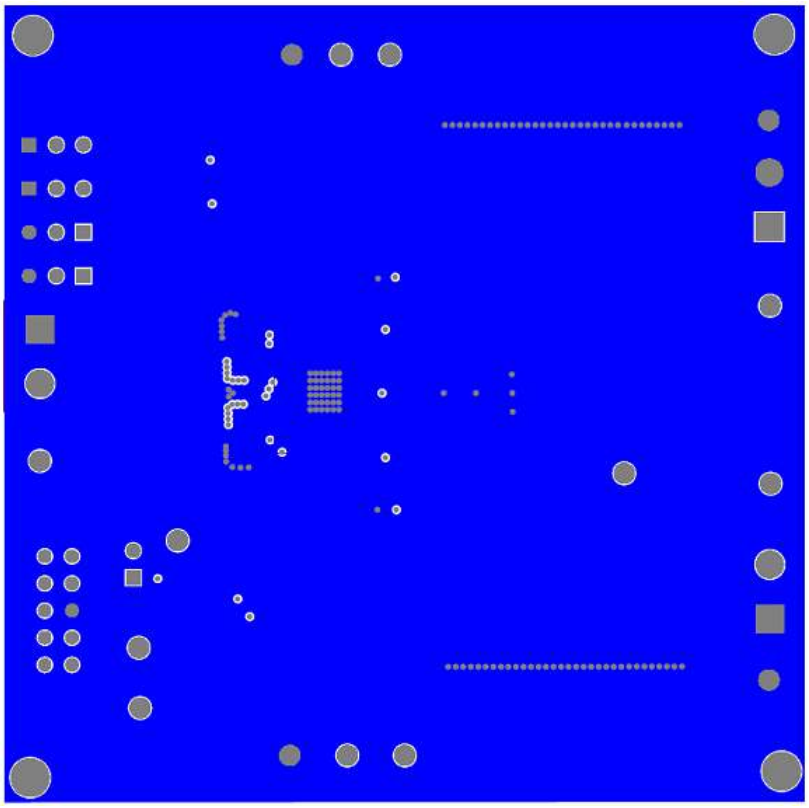
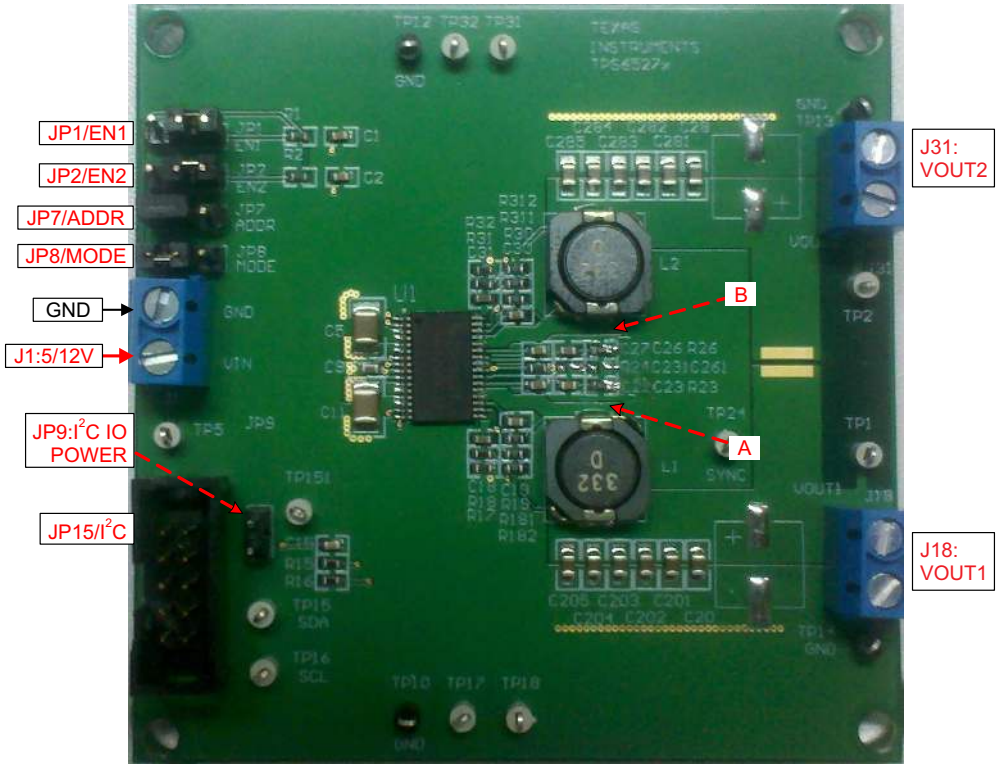


**Figure 4-5. Board Layout (Bottom Layer)**

# 5 Bench Test Setup Conditions

## 5.1 Header Description and Jumper Placement

Figure 5-1 illustrates the header description and jumper placement for the EVM.




**Test points:**
A: LX of Vout1
B: LX of Vout2
Vout1, Vout2

**Figure 5-1. Header Description and Jumper Placement**

Table 5-1 shows the I/O connections for the EVM.

**Table 5-1. Input/Output Connection**

| Jumper Number | Function | Description |
|---|---|---|
| J1 | Vin Connector | Apply power supply to this connector |
| J18 | Buck1 Connector | Output of Buck1 |
| J31 | Buck2 Connector | Output of Buck2 |

Table 5-2 shows the jumpers and switches for the EVM.

**Table 5-2. Jumpers and Switches**

| Jumper Number | Function | Placement | Comment |
|---|---|---|---|
| JP1 | Buck1 enable (EN1) | Connect EN1 to GND to disable Vout1, connect EN1 to Vin through a 100-kΩ resistor to enable Vout1; Leave open to enable Vout1 | |
| JP2 | Buck2 enable (EN2) | Connect EN2 to GND to disable Vout2, connect EN2 to Vin through a 100-kΩ resistor to enable Vout2; Leave open to enable Vout2 | |
| JP7 | $I^2C$ address | $I^2C$ address configuration pin. Connect this pin to GND to set address 0x60H; connect it to Vcc to set address 0x61H; leave it open to set address 0x62H | On board Vcc is 6.25 V |
| JP8 | Mode | Operation mode control pin. Connect this pin to GND to set forced PWM mode; leave the pin open to set auto PSM-PWM; connect this pin to Vcc set the IC to run in current share mode. | |
| JP9 | $I^2C$ Power | Power connected to the $I^2C$ IO pull-up resistor; Leave the two pins un-connected set the power to be 3.3V from the $I^2C$ interface adaptor; short the two pins set the power to be Vcc. | On board Vcc is 6.25 V |
| JP15 | $I^2C$ interface connector | Pin 5 is 3.3 V from adaptor; pin 6 is Ground; pin 9 is SCL, pin 10 is SDA. | |

## 5.2 Hardware Requirement

This EVM requires an external power supply capable of providing 4.5 V to 18 V at 7 A.

A function generator capable of driving the SYNC pin with 0.4- to 3.3-V amplitude and a 200-kHz to 1.6-MHz square wave signal is required for synchronization. The EVM kit includes a USB-TO-GPIO interface box which, when installed on a PC and connected to the EVM, allows communication with the EVM via a GUI interface. The minimum PC requirements are:

- Windows® 2000 or Windows XP operating system
- USB port
- Minimum of 30 MB of free hard disk space (100 MB recommended)
- Minimum of 256 MB of RAM

## 5.3 Hardware Setup

After connecting the power supply to J1, turn on the power supply, and connect JP1 to Vin through a 100-kΩ resistor, connect JP2 to Vin through a 100-kΩ resistor, connect JP7 to GND, connect JP8 to GND, the EVM will regulate the output voltages to the values shown in Table 2-1. Additional input capacitance may be required in order to mitigate the inductive voltage droop that may occur during a load transient event.

The output voltage is changed by sending the digital control signal via a PC running the TPS65279V controller software and USB-TO-GPIO interface box. Change the output voltage with the following steps:

- Connect one end of the USB-TO-GPIO box to the PC using the USB cable and the other end to JP15 of the TPS65279V using the supplied 10-pin ribbon cable as shown in Figure 5-2. The connectors on the ribbon cable are keyed to prevent incorrect installation.
- Connect the power supply on J1, and turn on the power supply.
- Run the software as explained in the next section.

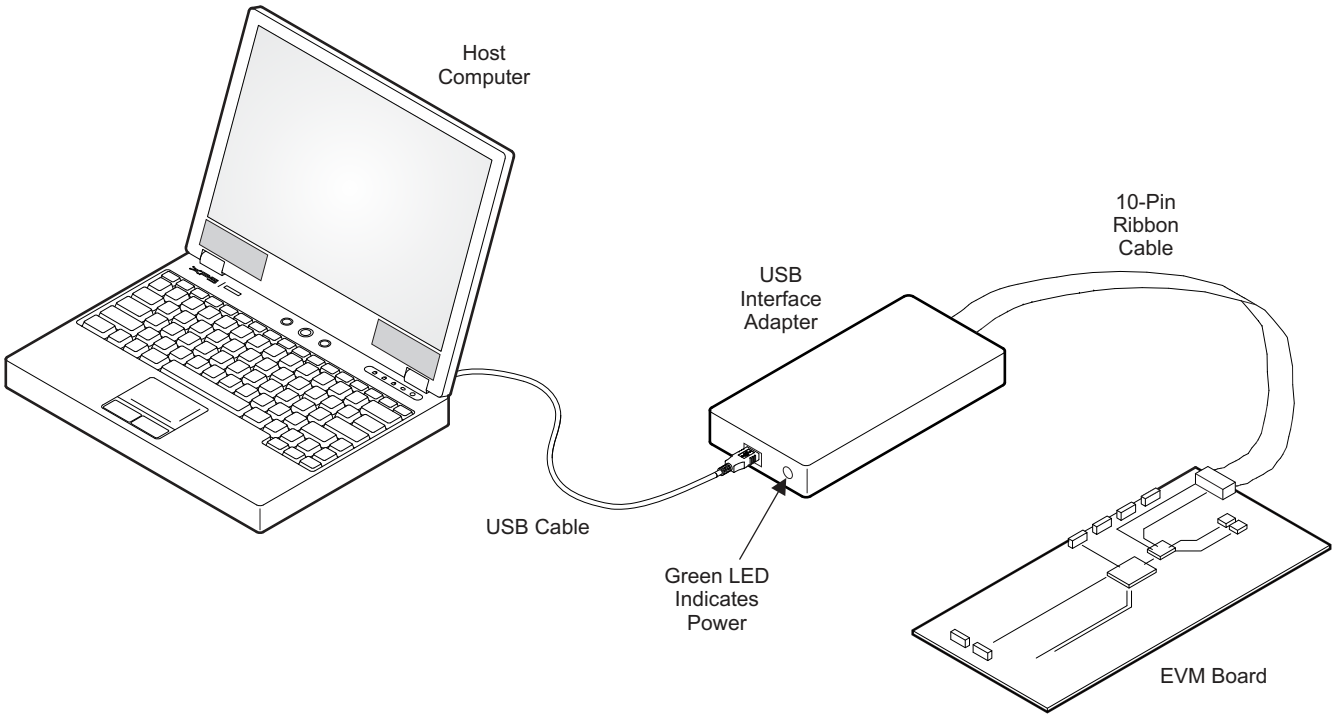



**Figure 5-2. USB Interface Adapter Quick Connection Diagram**

## 5.4 Installing Software

If installing from the TI Web site, go to www.ti.com.

**Note:** This installation page is best viewed with the Microsoft® Internet Explorer® browser (It may not work correctly with other browsers)

Click on the install button; your PC should give you a security warning and ask if you want to install this application. Select Install to proceed. If a pre-release or Beta version is currently installed on your PC, you must uninstall this version of the software before installing the final version.

To run the software after installation, go to Start → All programs → Texas Instruments → TPS65279V EVM Software.

At start-up, the software first checks the firmware version of the USB-TO-GPIO adapter box. If an incorrect firmware version is installed, the software automatically searches on the internet (if connected) for updates. If a new update is available, the software gives notification of the update, and downloads and installs the software. Note that after the firmware is updated the USB cable between the adapter and PC must be disconnected and then reconnected, as instructed during the install process. The host PC software also automatically searches on the internet (if connected) for updates. If a new update is available, the software gives notification of the update and downloads and installs it. During future use of the software, a prompt may be given to install a new version, if one becomes available.

**Note**

VeriSign® Code Signing is used to prevent any malicious code from changing this application. If at any time in the future the binaries are modified, the code will no longer attempt to run.

## 5.5 Software Operation

This section provides descriptions of the EVM software.

The supplied software is used to communicate with the TPS65279V EVM. Click on the icon on the host computer to start the software. The software displays the main control panel for the user interface (Figure 5-3).

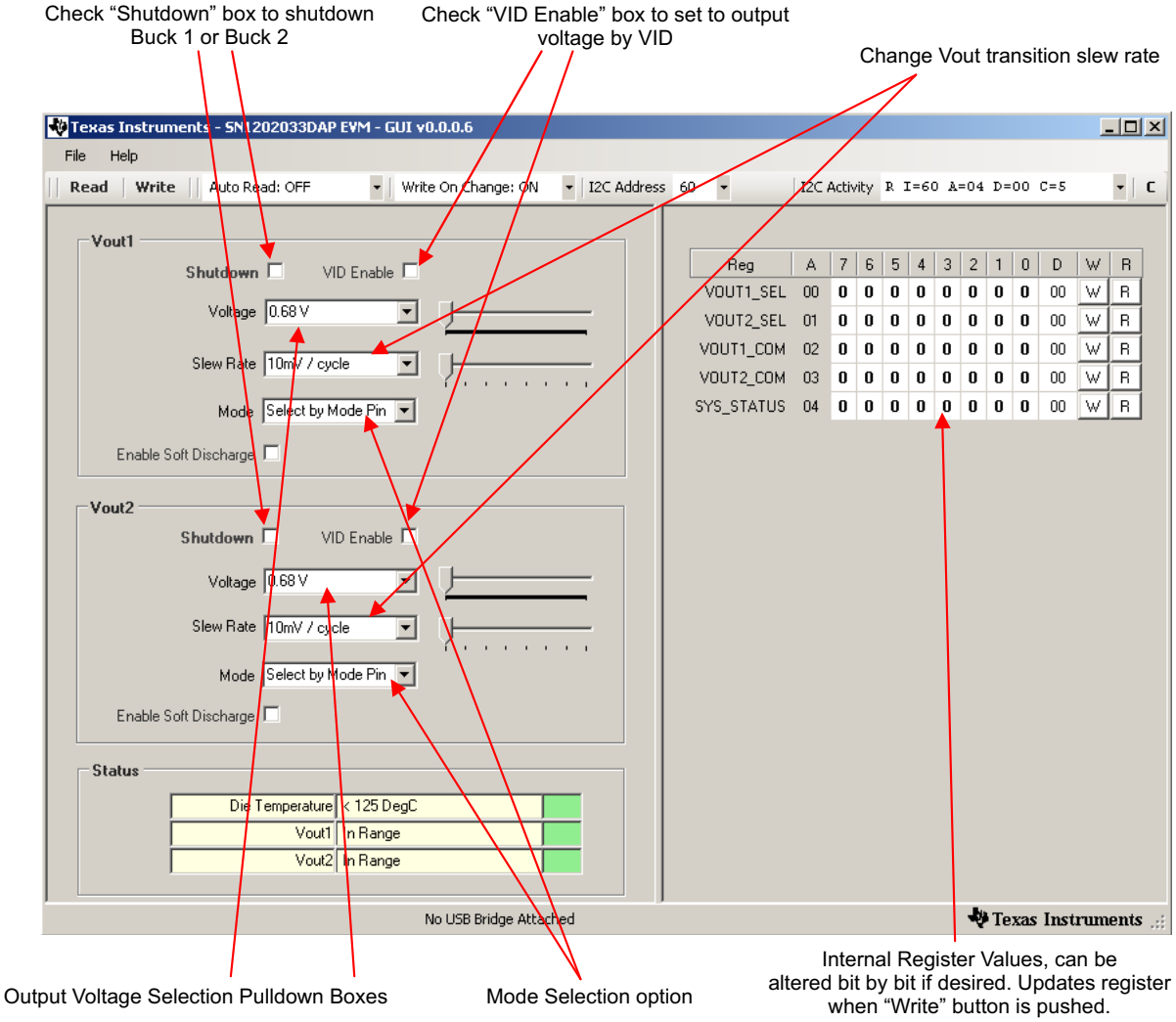



**Figure 5-3. Screen Capture of TPS65279V Software GUI Interface**

Figure 5-3 shows the GUI control interface. There are five 8-bit registers embedded in TPS65279V, two to select the output voltage, two to configure the buck converter’s operation, and one for status feedback. Changes are made by selecting and checking the components in the GUI on the left hand side and can also be made by directly clicking the bits of each register. $I^2C$ address is set to default 0x60H, this address is corresponding to the EVM jumper JP7 to connect to GND. Changing the $I^2C$ address requires that the EVM be configured accordingly.

An option is to “write on change”, if this option is set to ON, any change is sent to the EVM immediately; if this option is set to OFF, “Write” button or “W” button for each register must be clicked to send the control signal.

Register values can be read back from the EVM by clicking “Read” or “R” for each register.

# 6 Power-Up Procedure

Use the following steps to power-up the EVM:

1. Connect $I^2C$ adaptor to JP15
2. Apply 4.5 V to J1
3. Toggle JP1 or JP2 to enable Vout1 and Vout2, respectively
4. Apply loads to the output connectors.

# 7 TPS65279V EVM Bill of Materials

Table 7-1 is the BOM for the EVM.

**Table 7-1. TPS65279V EVM Bill of Materials**

| # | Value | Qty | Designator | Footprint | MFG | MFG Part Number | Description |
|---|---|---|---|---|---|---|---|
| 1 | 10nF | 2 | C1, C2 | 0603 | Generic | | CAP 10nF 50V CERAMIC X7R 0603 |
| 2 | 10nF | 4 | C22, C23, C26, C27 | 0603 | Generic | | CAP 10nF 50V CERAMIC X7R 0603 |
| 3 | 10uF | 2 | C5, C11 | 1210 | Panasonic -ECG | ECJ-4YB1E106M | CAP 10UF 25V CERAMIC X5R 1210 |
| 4 | 10uF | 1 | C9 | 0603 | Panasonic -ECG | ECJ-1VB1A106M | CAP 10UF 10V CERAMIC X5R 0603 |
| 5 | 1uF | 1 | C15 | 0603 | Generic | | CAP 1UF 10V CERAMIC X5R 0603 |
| 6 | 82pF | 2 | C18, C31 | 0603 | Generic | | CAP 82pF 50V CERAMIC X7R 0603 |
| 7 | 47nF | 2 | C19, C30 | 0603 | Generic | | CAP 47nF 50V CERAMIC X7R 0603 |
| 8 | 22uF | 12 | C20, C28, C201, C202, C203, C204, C205, C281, C282, C283, C284, C285 | 0805 | TDK | C2012X6S0J226M | CAP CER 22UF 6.3V 20% X6S 0805 |
| 9(3) | 470uF | DNI | C204, C284 | E_CAP_D8_L6.7 | Nichicon | RHA0J471MCN1GS | CAP ALUM 470UF 6.3V 20% SMD |
| 10 | 47pF | DNI | C231, C261 | 0603 | Generic | | CAP 47pF 50V CERAMIC X7R 0603 |
| 11(3) | ED500/2DS | 3 | J1, J18, J31 | TB_2X5.0MM | OnShore Technology Inc | ED500/2DS | Terminal Block, 2-pin, 15-A, 5.0mm |
| 12 | HEADER 3 PIN | 4 | JP1, JP2, JP7, JP8 | JMP0.3 | Mil-Max | 800-10-064-10-001000 | Three Pin Header |
| 13 | HEADER 2 PIN(4) | 1 | JP9 | JMP0.2 | Mil-Max | 800-10-064-10-001000 | Two Pin Header |
| 14 | HEADER 10 PIN(5) | 1 | JP15, | HEADER10 | 3M | N2510-6002-RB | Ten Pin Header |
| 15 | 3.3uH | 2 | L1, L2 | IND3 | Coilcraft | MSS1048-332NLB | SMT power inductor |
| 16 | 100K | 2 | R1, R2 | 0603 | Generic | | RES 100k OHM 1/10W 1% 0603 SMD |
| 17 | 100K | 1 | R24 | 0603 | Generic | | RES 100k OHM 1/10W 1% 0603 SMD |
| 18 | 10k | 2 | R15, R16 | 0603 | Generic | | RES 10k OHM 1/10W 1% 0603 SMD |
| 19 | 60.4K | 1 | R17 | 0603 | Generic | | RES 60.4k OHM 1/10W 1% 0603 SMD |
| 20 | 40.2K | 2 | R18, R31 | 0603 | Generic | | RES 40.2k OHM 1/10W 1% 0603 SMD |
| 21 | 0 | 6 | R19, R30, R181, R182, R311, R312 | 0603 | Generic | | RES 0 OHM 1/10W 1% 0603 SMD |
| 22 | 3.74k | 2 | R23, R26 | 0603 | Generic | | RES 3.7k OHM 1/10W 1% =0603 SMD |
| 23 | 48.7k | 1 | R32 | 0603 | Generic | | RES 48.7k OHM 1/10W 1% 0603 SMD |
| 24 | Test Point White | 11 | TP1, TP2, TP5, TP15, TP16, TP17, TP18, TP24, TP31, TP32, TP151 | TP | Keystone | 5002 | TEST POINT PC MINI .040"D WHITE |
| 25 | Test Point Black | 4 | TP10, TP12, TP13, TP14 | TP | Keystone | 5001 | TEST POINT PC MINI .040"D BLACK |
| 26(2) | | 4 | | | | | Jumper, 2.54mm, applied on item 13 |
| 27(1) | | 4 | | | 3M | SJ-5303 (CLEAR) | BUMPON HEMISPHERE .44X.20 CLEAR |
| 28 | | 1 | U1 | | Texas Instruments | TPS65279V | |

(1) Install item 27 on bottom at corners
(2) Install item 26 on item 13 no order - be consistent
(3) Item 9, 11: optional
(4) Item 13: split into 3 pins
(5) Item 14: split into 2 pins

# 8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (February 2013) to Revision A (May 2021) | Page |
|---|---|
| • Updated user's guide title | 2 |
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 2 |

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