User's Guide

ISO67xx Triple- and Quad-Digital Isolator Evaluation Module

ABSTRACT

This user's guide describes the ISO67xx triple- and quad-digital isolator evaluation module (EVM). This EVM lets designers evaluate device performance for fast development and analysis of isolated systems. The EVM supports evaluation of any of the TI triple- and quad-channel digital isolators in a 16-pin WB SOIC package.

CAUTION

This evaluation module is made available for isolator parameter performance evaluation only and is not intended for isolation voltage testing. To prevent damage to the EVM, any voltage applied as a supply or digital input/output must be maintained within the 0-V to 5.5-V recommended operating range.

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Trademarks

1 Introduction

This user's guide describes EVM operation with respect to the ISO67xx triple- and quad-digital isolators. However, the EVM may be reconfigured for evaluation of any of TI's triple- and quad-channel digital isolators in a 16-pin WB SOIC package. This guide also describes the available channel configurations within the ISO67xx family, the EVM schematic, and typical laboratory setup. A typical input and output waveform is also presented.

2 Overview

The ISO67xx is TI's new digital isolator family capable of galvanic isolations up to 5000 V_{RMS}. These isolators provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. The ISO67xx digital isolators have logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier. Used with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents on a data bus or other circuits from entering the local ground and interfering with, or damaging sensitive circuitry.

3 Pin Configurations of the ISO67xx Triple- and Quad-Channel Digital Isolators

Figure 3-1 shows the ISO67xx triple-channel digital isolator pin configurations.

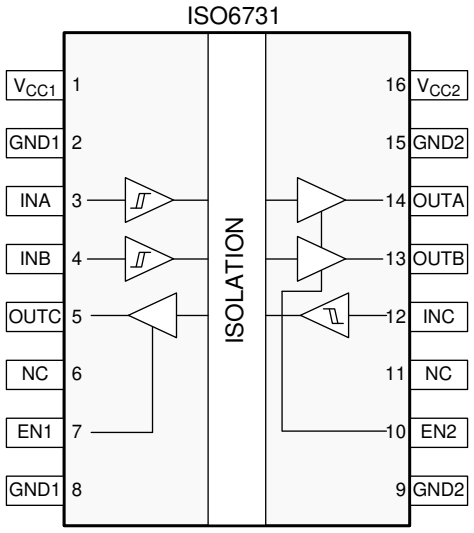

Figure 3-1. ISO67xx Triple-Channel Digital Isolator Pin Configurations

Figure 3-2 shows the ISO67xx quad-channel digital isolator pin configurations.

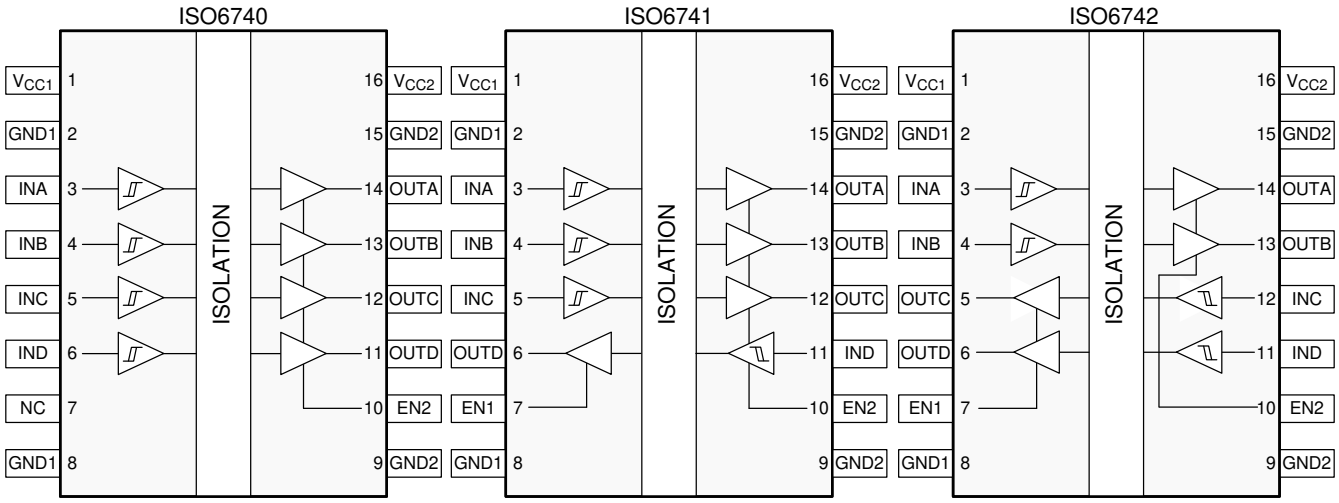

Figure 3-2. ISO67xx Quad-Channel Digital Isolator Pin Configurations

4 ISO6741 Board Block Diagram and Image

Figure 4-1 shows the board configuration for evaluation of the ISO6741 digital isolator.

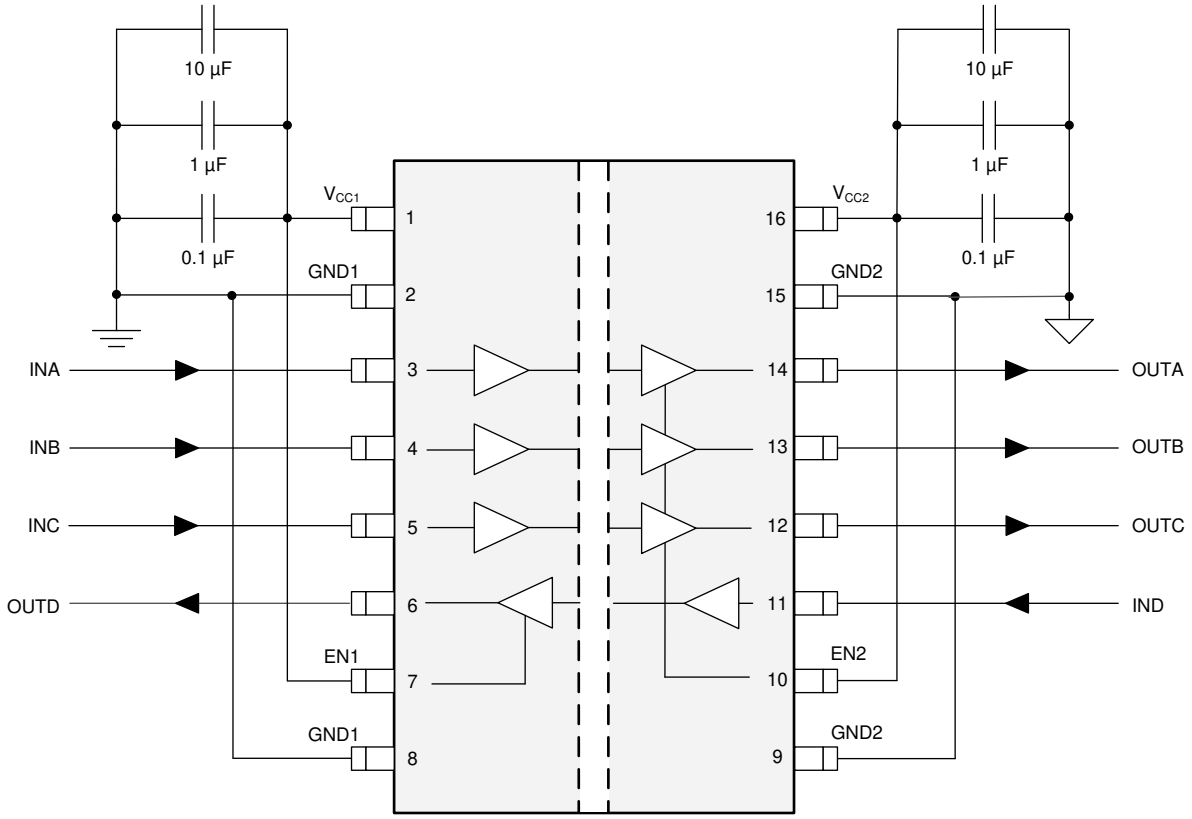

Figure 4-1. ISO6741 EVM Configuration

Figure 4-2 shows the 3D diagram of the EVM.

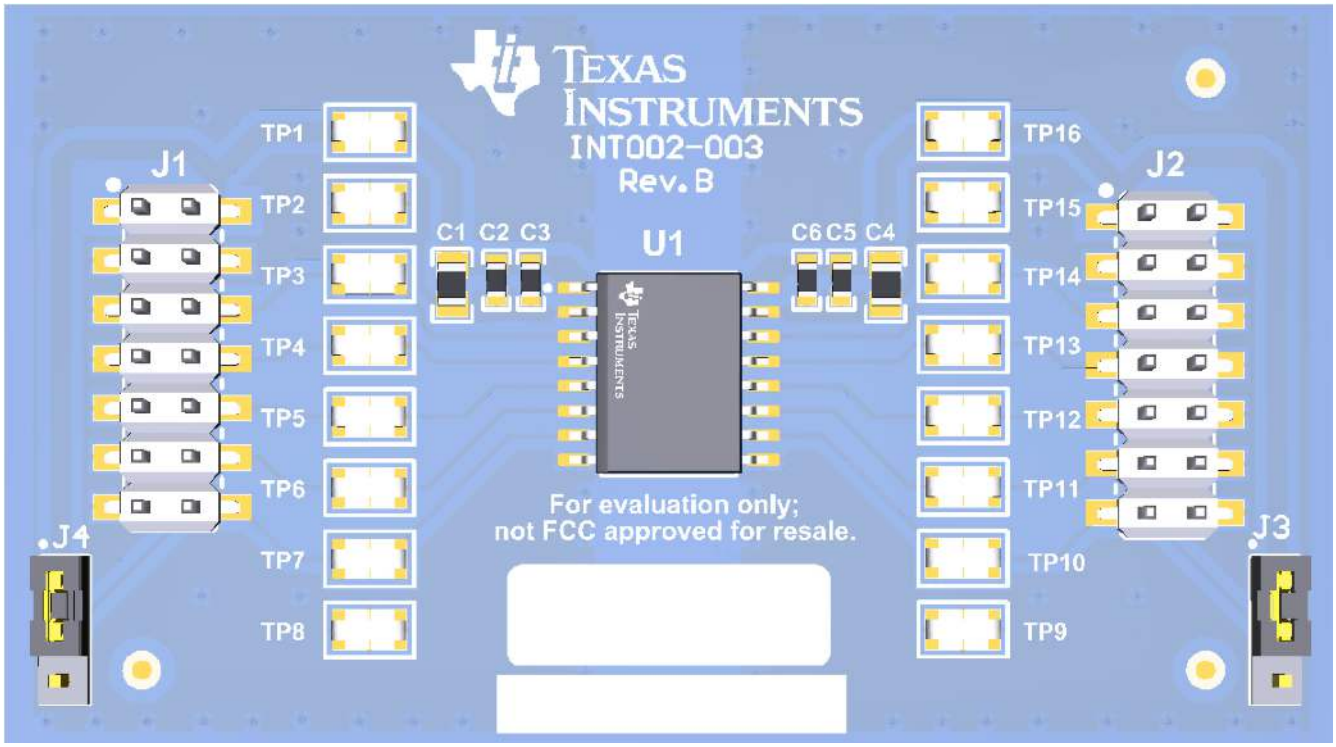

Figure 4-2. ISO6741DWEVM 3D Diagram

5 EVM Setup and Operation

This section describes the setup and operation of the EVM for parameter performance evaluation. Figure 5-1 shows the configuration for operating the ISO6741 dual-digital isolator EVM using two power supplies.

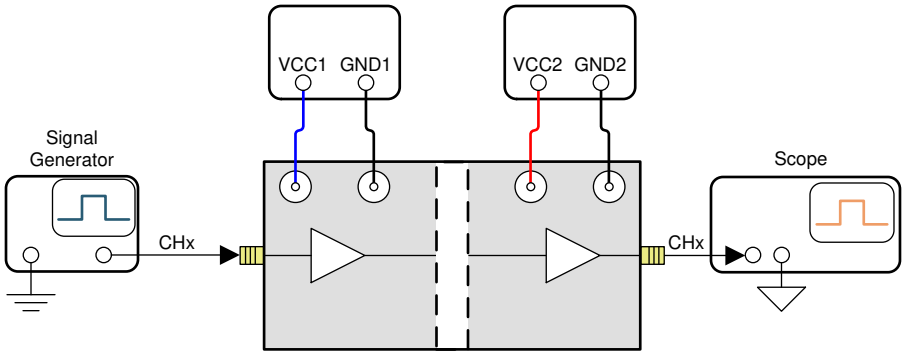

Figure 5-1. Basic EVM Operation

Figure 5-2 shows typical input and output waveforms of the EVM for a 1-MHz clock. The input is shown as channel 1, and the output is shown as channel 2.

Figure 5-2. Typical Input and Output Waveform

6 Bill of Materials

Table 6-1 lists the bill of materials (BOM) for this EVM.

Table 6-1. Bill of Materials

Item	Designator	Description	Manufacturer	Part Number	QTY
1	C1, C4	CAP, CERM, 10 µF, 35 V, ±10%, X5R, 0805	MuRata	GRM21BR6YA106KE43L	2
2	C2, C5	CAP, CERM, 1 µF, 25 V, ±10%, X7R, 0603	MuRata	GCJ188R71E105KA01D	2
3	C3, C6	CAP, CERM, 0.1 µF, 25 V, ±5%, X7R, 0603	AVX	06033C104JAT2A	2
4	H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
5	J1, J2	Header, 100mil, 7 × 2, SMT	Molex	0015912140	2
6	J3, J4	Header, 100mil, 3 × 1, Gold, TH	Samtec	HTSW-103-07-G-S	2
7	SH-J1, SH-J2	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G	2
8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16	Test Point, Miniature, SMT	Keystone	5019	16
9	U1	Low Speed, General Purpose, Quad-Channel Digital Isolator	Texas Instruments	ISO6741QDWRQ1	1

7 EVM Schematics and Layout

The ISO6741DWEVM is designed to accommodate any of the ISO67xx triple- and quad-channel devices in a 16-pin WB SOIC package. To evaluate any of the ISO67xx triple- and quad-channel devices in a 16-pin WB SOIC package, replace ISO67xx with the device of interest on the ISO6741DWEVM PCB. No other component requires any modification. Figure 7-1 shows the ISO67xx EVM schematic and Figure 7-2 shows the printed-circuit board (PCB) layout.

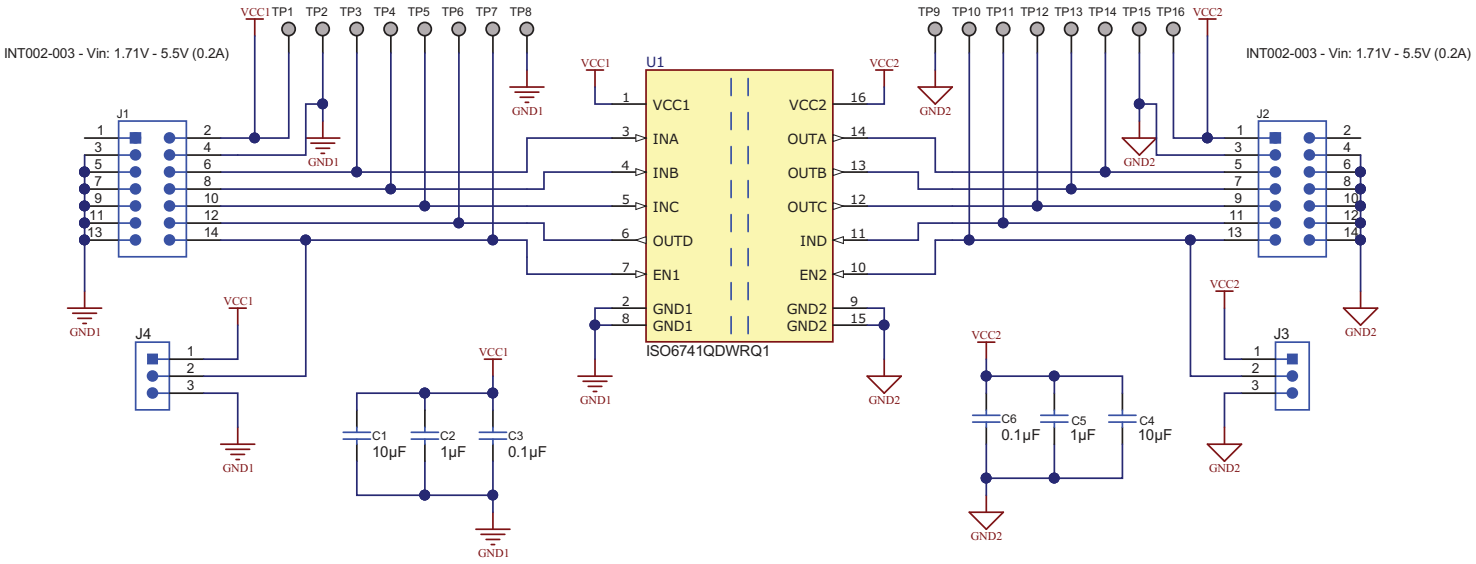

Figure 7-1. ISO6741DWEVM EVM Schematic

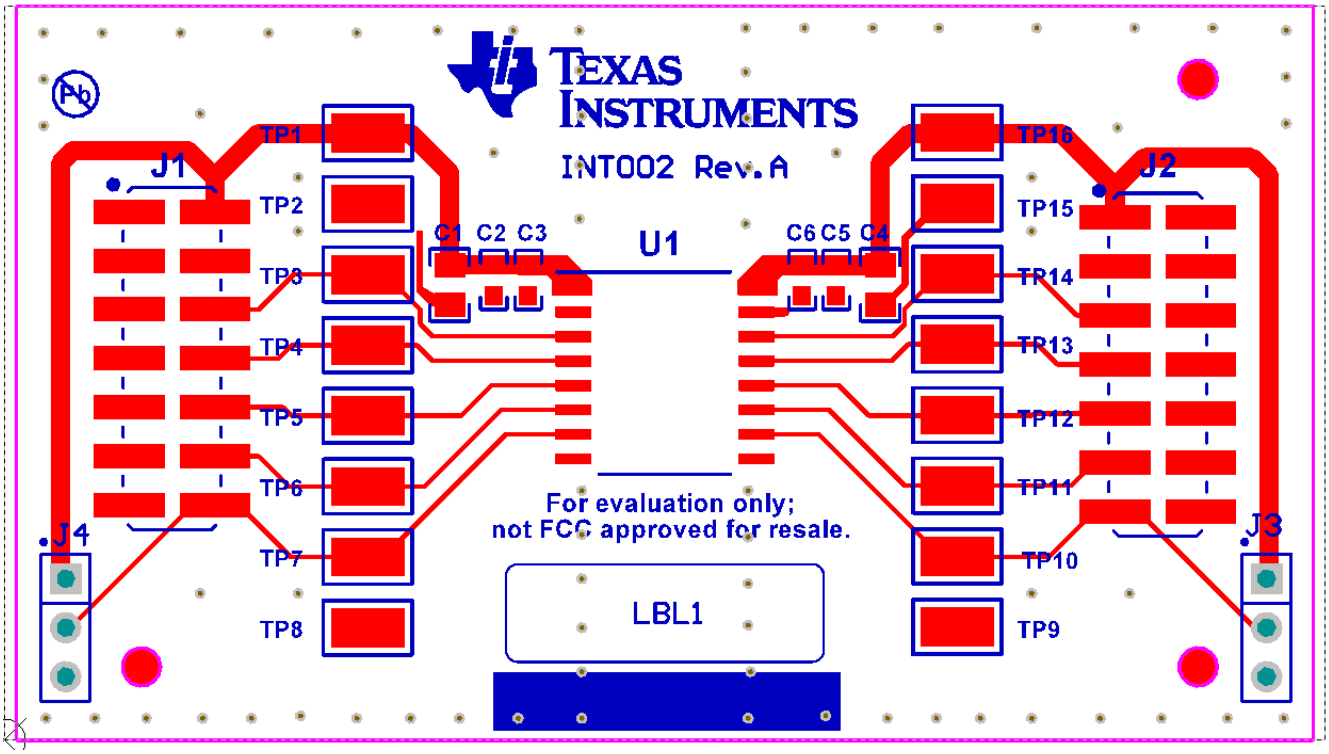

Figure 7-2. PCB Layout

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