

## N-channel 600 V, 0.440 $\Omega$ typ., 8 A MDmesh™ DM2 Power MOSFET in a TO-220FP package

Datasheet - production data

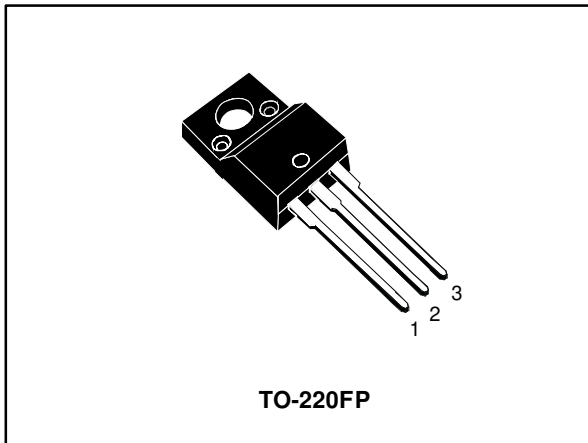
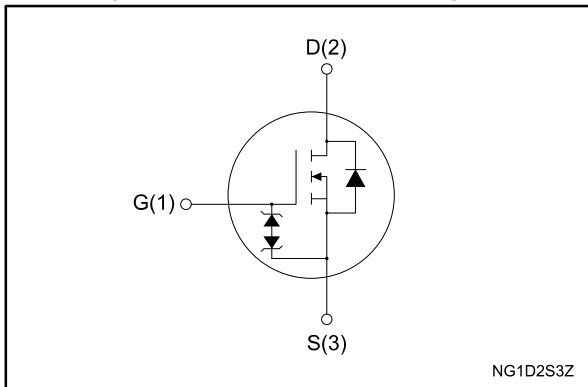


Figure 1: Internal schematic diagram



### Features

Order code	$V_{DS}$ @ $T_{Jmax.}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STF10N60DM2	650 V	0.530 $\Omega$	8 A	25 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STF10N60DM2	10N60DM2	TO-220FP	Tube

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	8	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	5	
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ °C}$	25	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$V_{ISO}^{(4)}$	Insulation withstand voltage (RMS) from all three leads to external heat sink	2.5	kV
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_j$	Operating junction temperature range		

**Notes:**

- (1) Pulse width is limited by safe operating area.  
 (2)  $I_{SD} \leq 8\text{ A}$ ,  $di/dt=900\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$   
 (3)  $V_{DS} \leq 480\text{ V}$ .  
 (4)  $t = 1\text{ s}$ ;  $T_C = 25\text{ °C}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	2	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	300	mJ

**Notes:**

- (1) pulse width limited by  $T_{jmax}$   
 (2) starting  $T_j = 25\text{ °C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$			1.5	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$ , $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 4\text{ A}$		0.440	0.530	$\Omega$

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	529	-	$\text{pF}$
$C_{\text{oss}}$	Output capacitance		-	28	-	
$C_{\text{riss}}$	Reverse transfer capacitance		-	0.72	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	47	-	$\text{pF}$
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	6.5	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 480\text{ V}$ , $I_{\text{D}} = 8\text{ A}$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> )	-	15	-	$\text{nC}$
$Q_{\text{gs}}$	Gate-source charge		-	3.7	-	
$Q_{\text{gd}}$	Gate-drain charge		-	8	-	

**Notes:**

<sup>(1)</sup>  $C_{\text{oss eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$ , $I_{\text{D}} = 4\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	11	-	$\text{ns}$
$t_{\text{r}}$	Rise time		-	5	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	28	-	
$t_{\text{f}}$	Fall time		-	11.5	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		8	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 8 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	90		ns
$Q_{rr}$	Reverse recovery charge		-	225		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	190		ns
$Q_{rr}$	Reverse recovery charge		-	684		nC
$I_{RRM}$	Reverse recovery current		-	7.2		A

**Notes:**

- (1) Limited by maximum junction temperature.  
(2) Pulse width is limited by safe operating area.  
(3) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 250 \mu\text{A}$ , $I_D = 0 \text{ A}$	$\pm 30$	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

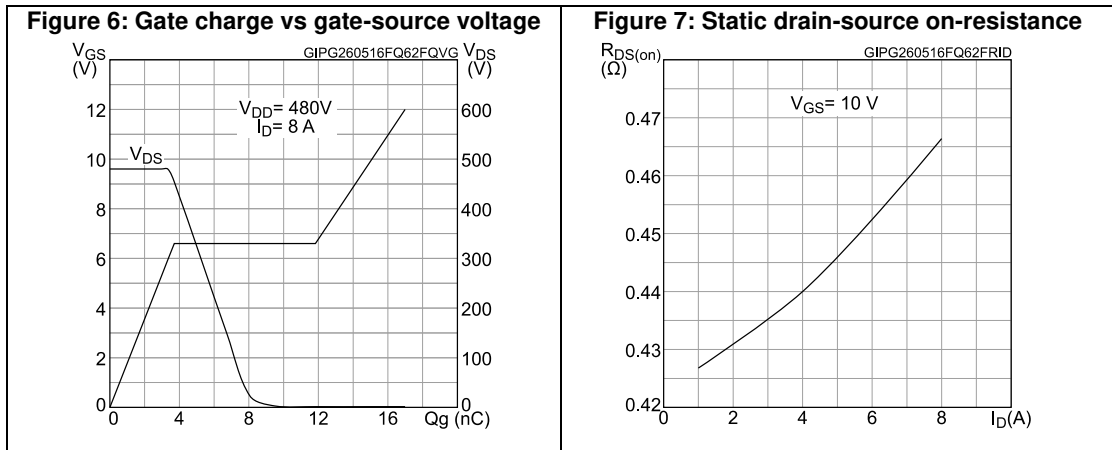
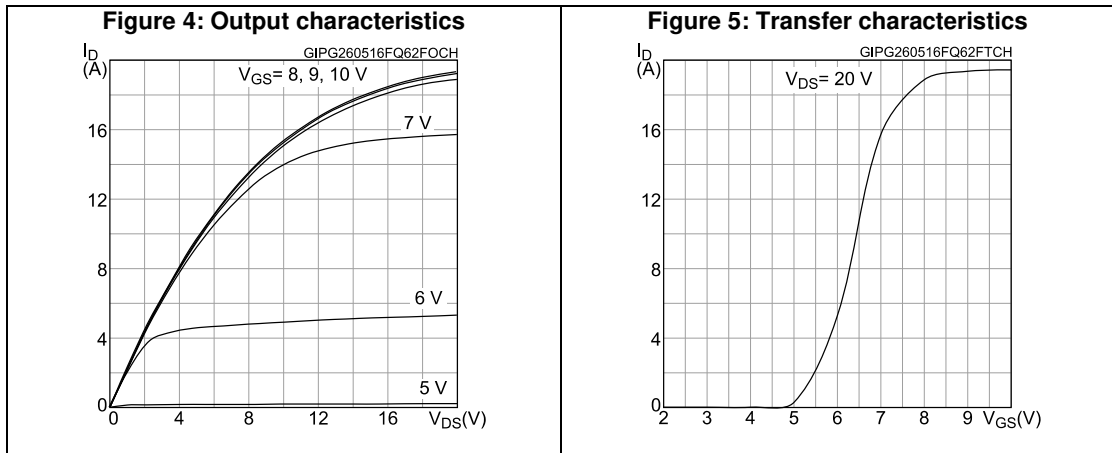
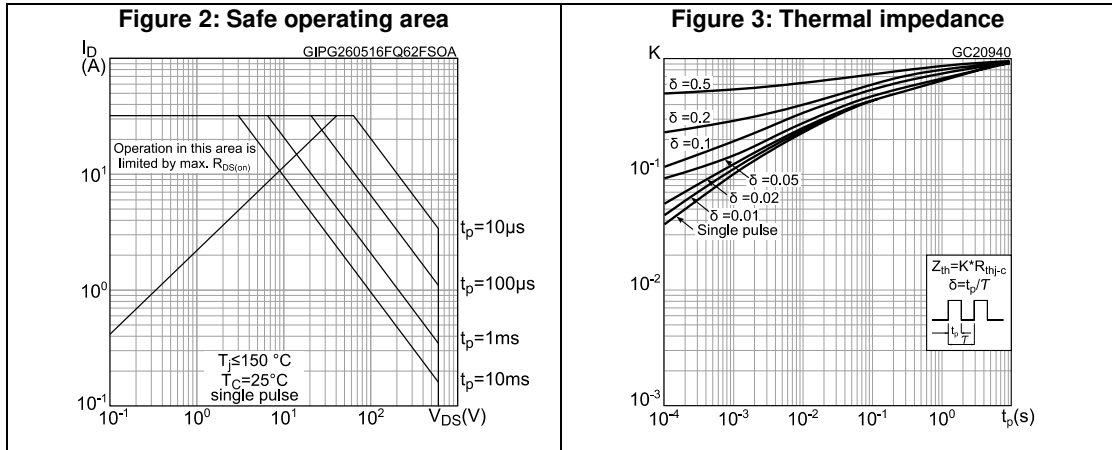


Figure 8: Capacitance variations

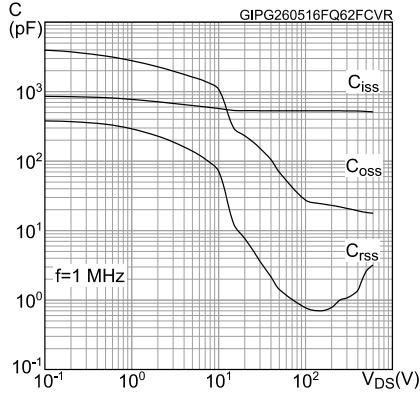


Figure 9: Normalized gate threshold voltage vs temperature

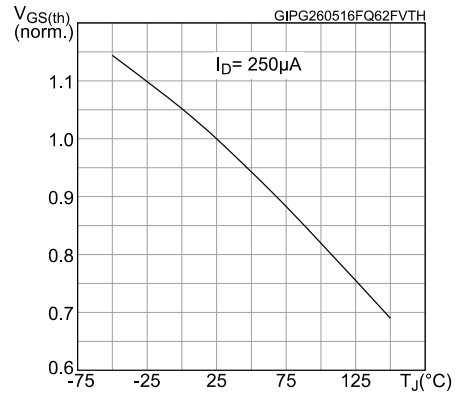


Figure 10: Normalized on-resistance vs temperature

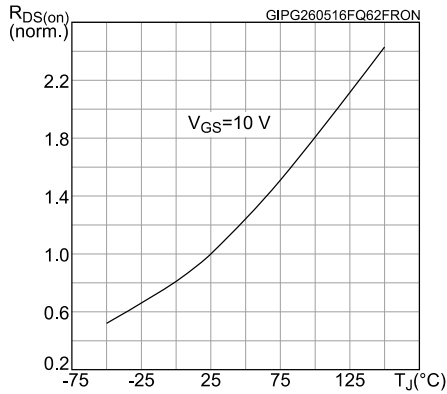


Figure 11: Normalized V(BR)DSS vs temperature

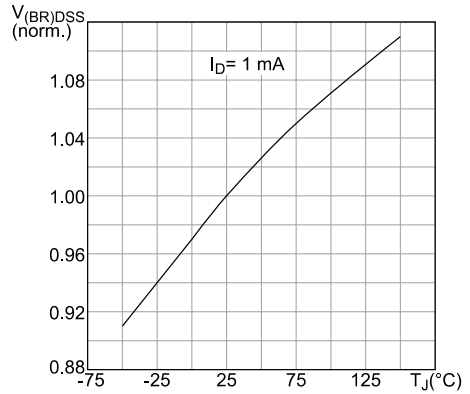


Figure 12: Output capacitance stored energy

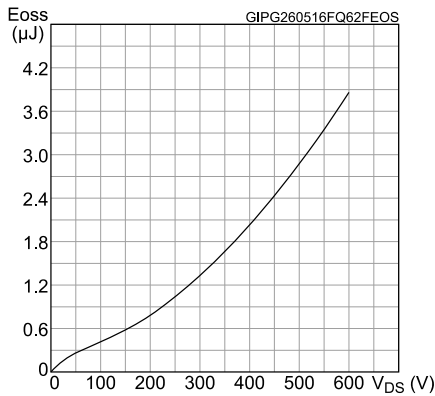
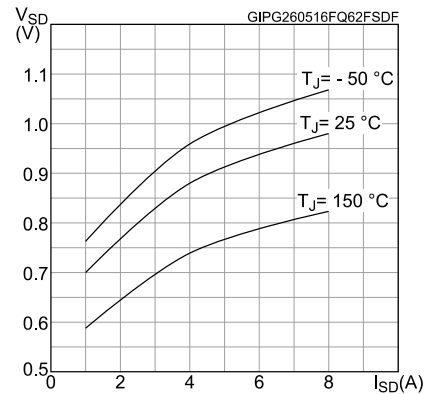
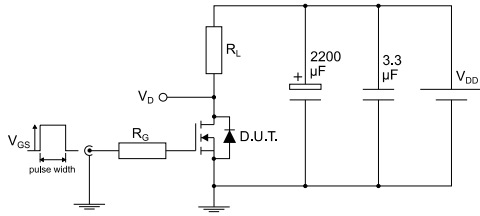


Figure 13: Source-drain diode forward characteristics



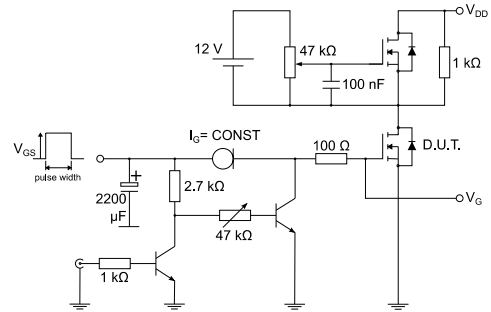
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



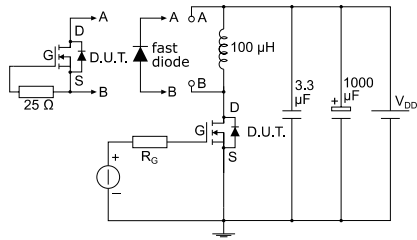
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**Figure 15: Test circuit for gate charge behavior**



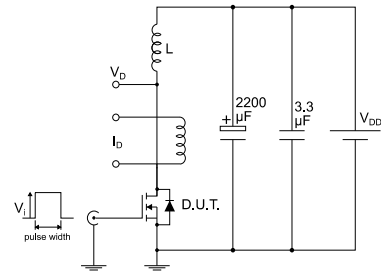
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**Figure 16: Test circuit for inductive load switching and diode recovery times**



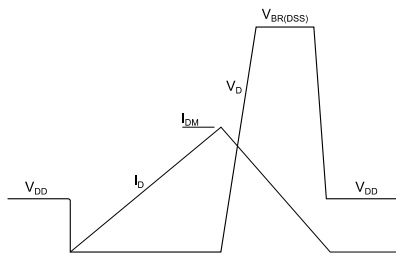
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**Figure 17: Unclamped inductive load test circuit**



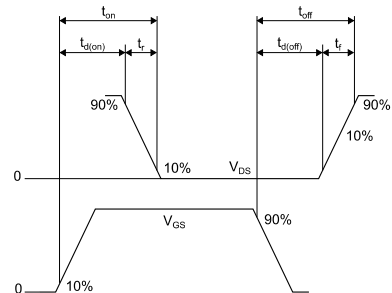
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**Figure 18: Unclamped inductive waveform**



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**Figure 19: Switching time waveform**



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## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220FP package information

Figure 20: TO-220FP package outline

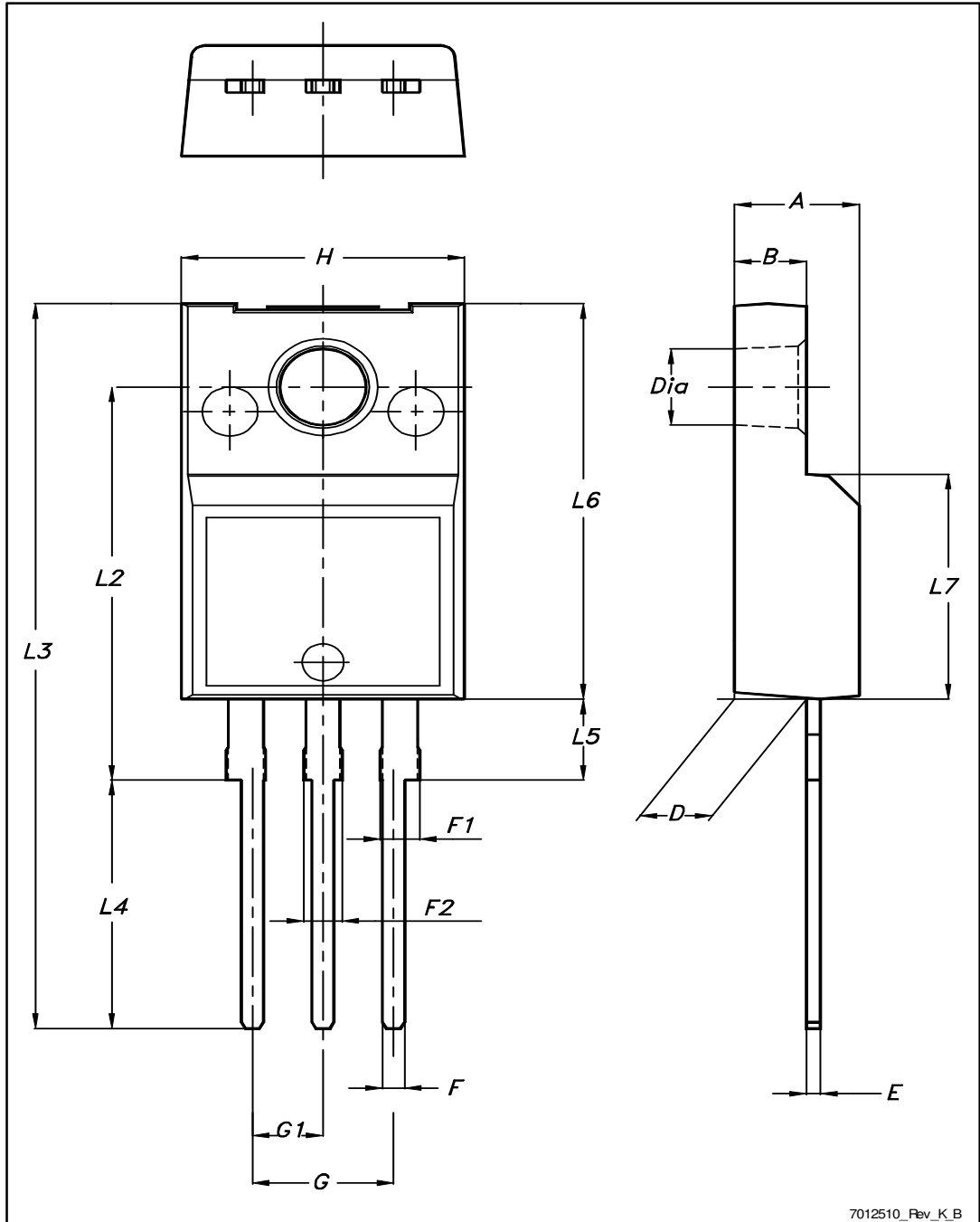


Table 10: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
17-Jun-2016	1	First release.

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