SCDS078D - JULY 1998 - REVISED NOVEMBER 2001

 Member of the Texas Instruments Widebus™ Family 	DGG, DGV, OR DL PACKAGE (TOP VIEW)					
 25-Ω Switch Connection Between Two Ports 	NC [1A1 [] V _{CC}] 10E		
TTL-Compatible Input Levels	1A1 L 1A2 L			10E 1B1		
Latch-Up Performance Exceeds 100 mA Per	1A3 🛛	4	45	1B2		
JESD 78, Class II	1A4 [1B3		
ESD Protection Exceeds JESD 22	1A5 [] 1B4		
 2000-V Human-Body Model (A114-A) 200 V Machine Model (A115 A) 	1A6 [1A7 [] 1B5] 1B6		
 200-V Machine Model (A115-A) 	1A7 L 1A8 L			1B0 1B7		
description	1A8 L 1A9 L			1B7 1B8		
	1A9 L			1B0 1B9		
The SN74CBTR16861 provides 20 bits of	GND			1B10		
high-speed TTL-compatible bus switching. The				V _{CC}		
low on-state resistance of the switch allows				20E		
connections to be made with minimal propagation	2A2 🛛		34	2B1		
delay.	2A3 🛛	16	33] 2B2		
The device is organized as one dual 10-bit switch	2A4 [17	32] 2B3		
with separate output-enable (\overline{OE}) inputs. When	2A5 🛛] 2B4		
OE is low, the switch is on, and port A is connected	2A6 🛛			2B5		
to port B. When \overline{OE} is high, the switch is open, and				2B6		
the high-impedance state exists between the two	2A8 [2B7		
ports.	2A9 L	22	27	2B8		

The device has equivalent $25 \cdot \Omega$ series resistors to reduce signal-reflection noise. This eliminates the need for external terminating resistors.

NC - No internal connection

26 2B9

25 2B10

2A10

GND [

23

24

TA	PACK	AGE [†]	T ORDERABLE PART NUMBER						
SSOP – DL		Tube	SN74CBTR16861DL	CBTR16861					
–40°C to 85°C	330F - DL	Tape and reel	SN74CBTR16861DLR	CBIRI0001					
	TSSOP – DGG	Tape and reel	SN74CBTR16861DGGR	CBTR16861					
	TVSOP – DGV	Tape and reel	SN74CBTR16861DGVR	CZ861					
-40°C to 85°C				-					

ORDERING INFORMATION

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(each 10-bit bus switch)						
INPUT OE	FUNCTION					
L	A port = B port					

Н

FUNCTION TABLE

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Disconnect

Widebus is a trademark of Texas Instruments.

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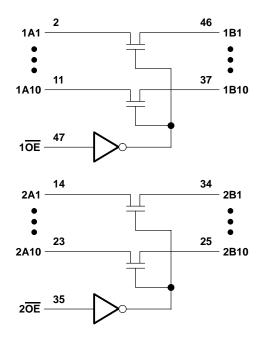
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SN74CBTR16861 20-BIT FET BUS SWITCH

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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V _{CC} Input voltage range, V _I (see Note 1)		
Continuous channel current		
Input clamp current, I _{IK} (V _{I/O} < 0)		–50 mA
Package thermal impedance, θ_{JA} (see Note 2):	: DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
VCC	Supply voltage	4	5.5	V
VIH	High-level control input voltage	2		V
V_{IL}	Low-level control input voltage		0.8	V
Т _А	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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TEST CONDITIONS TYP[†] PARAMETER MIN MAX UNIT -1.2 VIK $V_{CC} = 4.5 V,$ $I_{I} = -18 \text{ mA}$ V $V_{CC} = 0,$ VI = 5.5 V 10 Ιı μΑ $V_{CC} = 5.5 V_{,}$ $V_I = 5.5 V \text{ or } GND$ ±1 3 ICC V_{CC} = 5.5 V, IO = 0, $V_I = V_{CC} \text{ or } GND$ μA ∆lcc‡ Control inputs $V_{CC} = 5.5 V_{,}$ One input at 3.4 V, Other inputs at V_{CC} or GND 2.5 mΑ Control inputs $V_{I} = 3 V \text{ or } 0$ 3.5 pF Ci $\overline{OE} = V_{CC}$ V_O = 3 V or 0, 5 pF Cio(OFF) $V_{CC} = 4 V,$ $V_{I} = 2.4 V,$ $I_{I} = 15 \text{ mA}$ 20 37 50 TYP at V_{CC} = 4 V 20 47 $I_{I} = 64 \text{ mA}$ 33 ron§ Ω $V_{I} = 0$ 47 V_{CC} = 4.5 V $I_1 = 30 \text{ mA}$ 20 33 $V_{I} = 2.4 V_{,}$ $I_{I} = 15 \text{ mA}$ 20 35 48

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†] All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

[‡] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

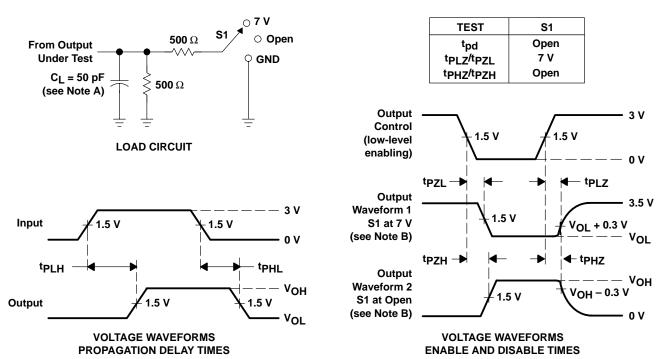
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} :	= 4 V	= V _{CC} ± 0.	UNIT	
			MIN	MAX	MIN	MAX	
t _{pd} ¶	A or B	B or A		1.25		1.25	ns
t _{en}	OE	A or B	3.1	9	2.7	8.6	ns
^t dis	OE	A or B	2.7	6.3	2.3	6.9	ns

The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).



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PARAMETER MEASUREMENT INFORMATION

NOTES: A. $C_{\mbox{L}}$ includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, Z_Q = 50 Ω , t_f \leq 2.5 ns, t_f \leq 2.5 ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms



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PACKAGING INFORMATION

RUMENTS

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74CBTR16861DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTR16861DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTR16861DGVRE4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTR16861DGVRG4	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74CBTR16861DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTR16861DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTR16861DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74CBTR16861DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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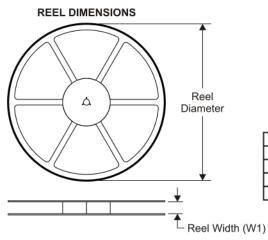
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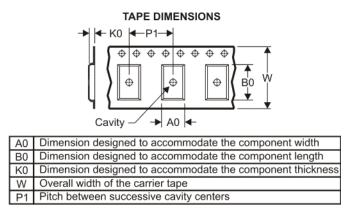
PACKAGE MATERIALS INFORMATION

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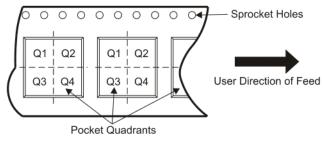
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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CBTR16861DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74CBTR16861DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74CBTR16861DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TEXAS INSTRUMENTS

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PACKAGE MATERIALS INFORMATION

11-Aug-2009



*All dimensions are nominal

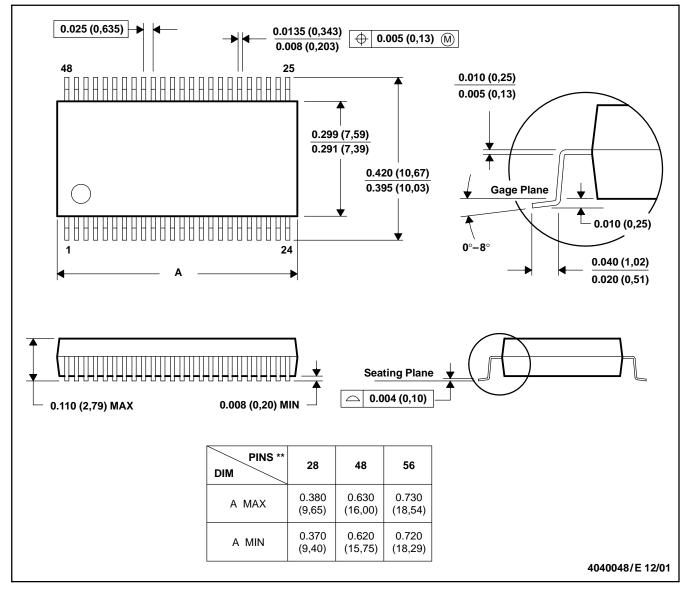
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CBTR16861DGGR	TSSOP	DGG	48	2000	346.0	346.0	41.0
SN74CBTR16861DGVR	TVSOP	DGV	48	2000	346.0	346.0	33.0
SN74CBTR16861DLR	SSOP	DL	48	1000	346.0	346.0	49.0

MECHANICAL DATA

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE PACKAGE

DL (R-PDSO-G**) 48 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MO-118



MECHANICAL DATA

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153



MECHANICAL DATA

PLASTIC SMALL-OUTLINE

MPDS006C - FEBRUARY 1996 - REVISED AUGUST 2000

DGV (R-PDSO-G**)

24 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153

14/16/20/56 Pins – MO-194



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