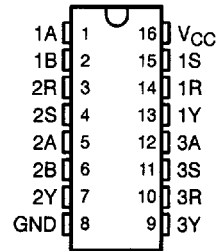


# SN75124 TRIPLE LINE RECEIVER

SLLS058B - SEPTEMBER 1973 - REVISED MAY 1995

- Meets or Exceeds the Requirements of IBM™ System 360 Input/Output Interface Specification
- Operates From Single 5-V Supply
- TTL Compatible
- Built-In Input Threshold Hysteresis
- High Speed . . . Typical Propagation Delay Time = 20 ns
- Independent Channel Strobes
- Input Gating Increases Application Flexibility
- Designed for Use With Dual Line Driver SN75123
- Designed to Be Interchangeable With Signetics N8T24

D OR N PACKAGE  
(TOP VIEW)



## description

The SN75124 triple line receiver is specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

The SN75124 has receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. An open line affects the receiver input as does a low-level input voltage, and the receiver input can withstand a level of  $-0.15\text{ V}$  with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, hold the output low. The third receiver has only an A input that, if high, holds the output low.

See the SN751730 for new IBM 360/370 interface designs.

The SN75124 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

† B input and last two lines of the function table are applicable to receivers 1 and 2 only.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

  
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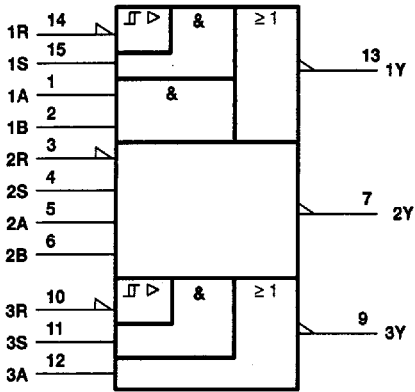
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# SN75124 TRIPLE LINE RECEIVER

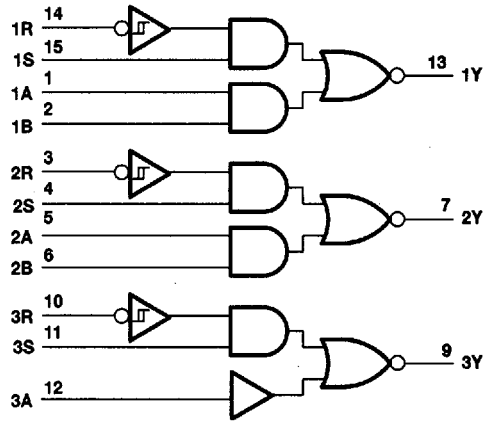
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## logic symbol†

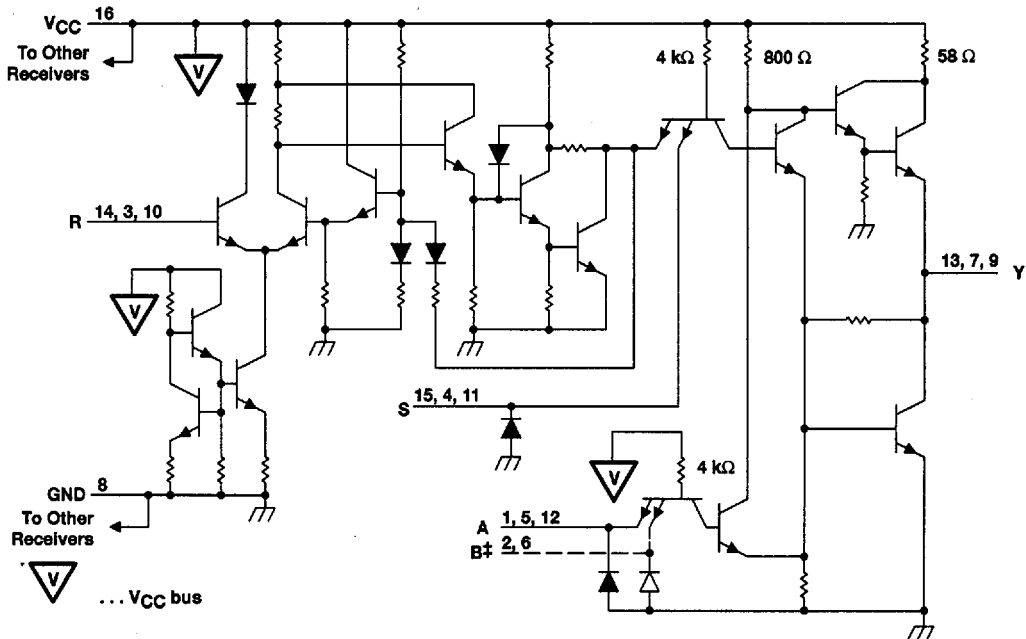


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram



## schematic (each receiver)



‡ B input is provided on receivers 1 and 2 only  
Resistor values shown are nominal.

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# SN75124 TRIPLE LINE RECEIVER

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**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )	R	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$	0.2	0.5		V
$V_{IK}$	Input clamp voltage	A, B, or S	$V_{CC} = 5\text{ V}$ , $I_I = 12\text{ mA}$			-1.5	V
$V_{I(BR)}$	Input breakdown voltage	A, B, or S	$V_{CC} = 5\text{ V}$ , $I_I = 10\text{ mA}$	5.5			V
$V_{OH}$	High-level output voltage		$V_{IH} = V_{IHmin}$ , $I_{OH} = -800\ \mu\text{A}$ , $V_{IL} = V_{ILmax}$ , See Note 2	2.6			V
$V_{OL}$	Low-level output voltage		$V_{IH} = V_{IHmin}$ , $I_{OL} = 16\text{ mA}$ , $V_{IL} = V_{ILmax}$ , See Note 2			0.4	V
$I_I$	Input current at maximum input voltage	R	$V_I = 7\text{ V}$			5	mA
			$V_I = 6\text{ V}$ , $V_{CC} = 0$			5	
$I_{IH}$	High-level input current	A, B, or S	$V_I = 4.5\text{ V}$			40	$\mu\text{A}$
		R	$V_I = 3.11\text{ V}$			170	
$I_{IL}$	Low-level input current	A, B, or S	$V_I = 0.4\text{ V}$ , $V_{IR} = 0.8\text{ V}$	-0.1		-1.6	mA
$I_{OS}$	Short-circuit output current†			-50		-100	mA
$I_{CC}$	Supply current		All inputs = 0.8 V			72	mA
			All inputs = 2 V			100	

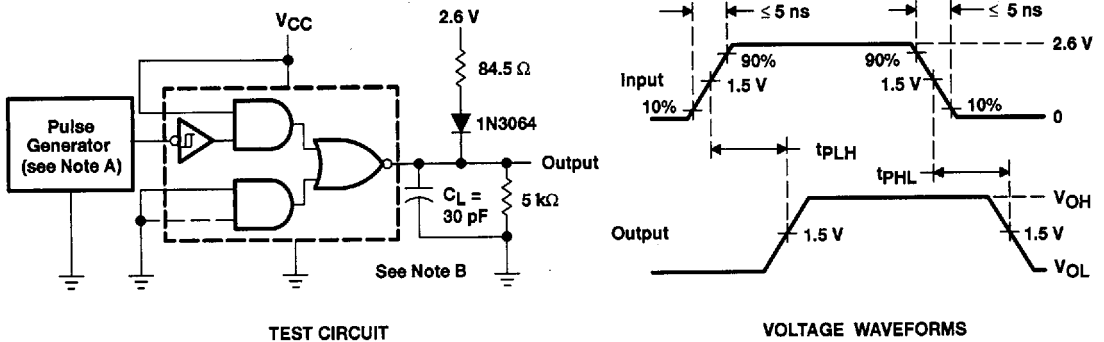
† Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTE 2: The output voltage and current limits are characterized for any appropriate combination of high and low inputs specified by the function table for the desired output.

## switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pLH}$	Propagation delay time, low-to-high-level output from R input		See Figure 1		20	30	ns
$t_{pHL}$	Propagation delay time, high-to-low-level output from R input				20	30	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:  $Z_O \approx 50 \Omega$ ,  $PRR \leq 5 \text{ MHz}$ , duty cycle = 50%.  
B.  $C_L$  includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

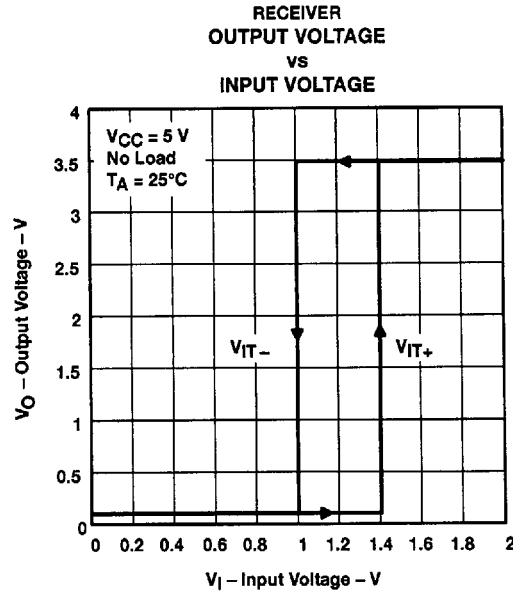


Figure 2

# SN75124 TRIPLE LINE RECEIVER

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## APPLICATION INFORMATION

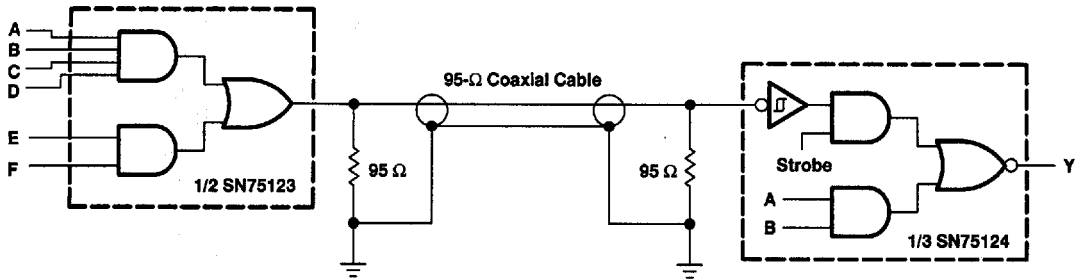


Figure 3. Unbalanced Line Communication Using SN75123 and SN75124

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