

CD74LPT16501

December 1996

Fast CMOS 18-Bit Registered Transceiver

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input Can Be 3V or 5V
 - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- · Excellent Output Drive Capability:
 - Balanced Drives (24mA Sink and Source)
- · Pin Compatible with Industry Standard **Double-Density Pinouts**
- Low Ground Bounce Outputs
- · Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins **Minimizing Switching Noise**

Ordering Information

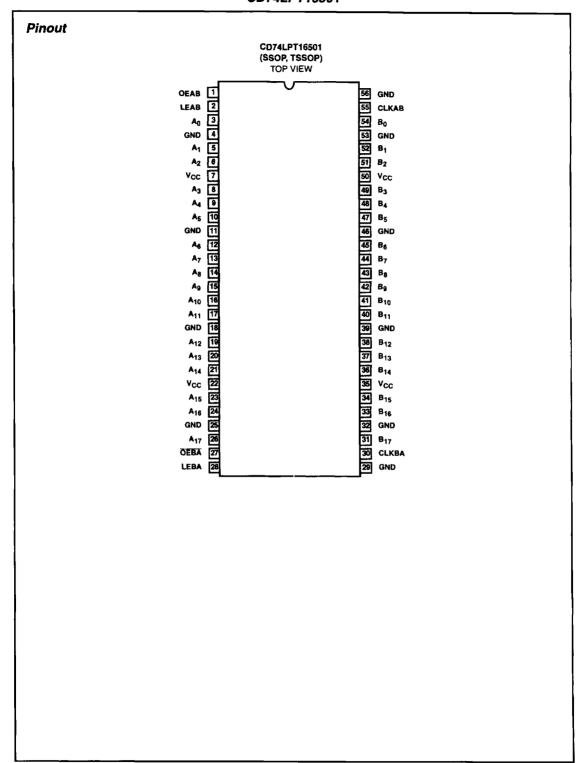
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16501AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16501ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16501MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16501SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

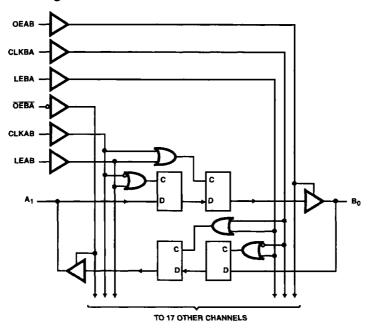
Description

The CD74LPT16501 is an 18-bit registered bus transceiver designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and OEBA), Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flipflop on the LOW-to-HIGH transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using OEBA, LEBA and CLKBA. This high-speed, low power device offers a flow-through organization for ease of board layout.

The CD74LPT16501 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3V/5.0V system.



Functional Block Diagram



TRUTH TABLE (NOTES 1, 4)

	INP	UTS		OUTPUTS
OEAB	LEAB	CLKAB	A _X	₽X
L	×	х	×	Z
н	н	х	L	L
н	Н	х	Н	Н
н	L	Ť	L	L
Н	L	1	н	Н
н	L	L	x	B (Note 2)
Н	L	Н	X	B (Note 3)

NOTES:

- 1. A-to-B data flow is shown. B-to-A data flow is similar but uses OEBA, LEBA, and CLKBA.
- 2. Output level before the indicated steady-state input conditions were established.
- Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
- 4. H = High Voltage Level
 - L = Low Voltage Level
 - Z = High Impedance
 - ↑ = LOW-to-HIGH Transition

CD74LPT16501

Pin Descriptions

PIN NAME	DESCRIPTION
OEAB	A-to-B Output Enable Input
OEBA	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A _X	A-to-B Data Inputs or B-to-A Three-State Outputs
Вχ	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V _{CC}	Power

Absolute Maximum Ratings	Thermal Information
DC Input Voltage -0.5V to 7.0V DC Output Current 120mA	Thermal Resistance (Typical, Note 5) θ _{JA} (°C/W) TSSOP Package 85
Operating Conditions Operating Temperature Range	SSOP Package

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDIT	ONS	MIN	(NOTE 7) TYP	MAX	UNITS
DC ELECTRICAL SPE	CIFICATIO	NS Over the Operating Range, Ta	= -40°C to 85°C, V	_{CC} = 2.7V to 3	3.6V		-
Input HIGH Voltage (Input Pins)	V _{IH}	Guaranteed Logic HIGH Level		2.2	•	5.5	٧
Input HIGH Voltage (I/O Pins)	V _{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	٧
Input LOW Voltage (Input and I/O Pins)	V _{IL}	Guaranteed Logic LOW Level		-0.5	-	8.0	٧
Input HIGH Current (Input Pins)	IIH	V _{CC} = Max	V _{IN} = 5.5V	-	-	±1	μА
Input HIGH Current (I/O Pins)	lін	V _{CC} = Max	V _{IN} = V _{CC}	-	-	±1	μА
Input LOW Current (Input Pins)	IIL	V _{CC} = Max	V _{IN} = GND	-	-	±1	μА
Input LOW Current (I/O Pins)	I _{IL}	V _{CC} = Max	V _{IN} = GND	-	-	±1	μА
High Impedance	l _{OZH}	V _{CC} = Max	V _{OUT} = 5.5V		-	±1	μА
Output Current (Three-State Output Pins)	put I _{OZL} V _{CC} = Max	V _{OUT} = GND	-	-	±1	μА	
Clamp Diode Voltage	VIK	V _{CC} = Min, I _{IN} = -18mA		-	-0.7	-1.2	٧
Output HIGH Current	looh	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL} , $V_{O} = 1.5V$ (Note 8)		-36	-60	-110	mA
Output LOW Current	IODL	/ _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V (Note 8)		50	90	200	mA
Output HIGH Voltage	V _{OH}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -0.1mA	V _{CC} - 0.2	-	-	٧
			I _{OH} = -3mA	2.4	3.0	-	٧
		$V_{CC} = 3.0V$, $V_{IN} = V_{IH}$ or V_{IL}	I _{OH} ≈ -8mA	2.4 (Note 10)	3.0	-	٧
			I _{OH} = -24mA	2.0	- 1	-	٧
Output LOW Voltage	V _{OL}	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1mA	-		0.2	٧
			I _{OL} ≈ 16mA		0.2	0.4	٧
			I _{OL} = 24mA	-	0.3	0.5	٧
Short Circuit Current (Note 9)	los	V _{CC} = Max (Note 8), V _{OUT} = G	ND	-60	-85	-240	mA
Power Down Disable	OFF	V _{CC} = 0V, V _{IN} or V _{OUT} ≤4.5V		-	-	±100	μА

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Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	мах	UNITS
Input Hysteresis	VΗ			•	150	-	mV
CAPACITANCE T _A =	25°C, f = 1MI	Hz					
Input Capacitance (Note 11)	C _{IN}	V _{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 11)	C _{OUT}	V _{OUT} = 0V		-	5.5	8	рF
POWER SUPPLY SP	ECIFICATION	NS			·		
Quiescent Power Supply Current	lcc	V _{CC} = Max	V _{IN} = GND or V _{CC}	-	0.1	10	μА
Quiescent Power Supply Current TTL Inputs HIGH	ΔlCC	V _{CC} = Max	V _{IN} = V _{CC} - 0.6V (Note 12)	-	2.0	30	μА
Dynamic Power Supply Current (Note 13)	ICCD	V _{CC} = Max, Outputs Open OEAB = OEBA = V _{CC} or GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	-	50	75	μΑ/ MHz
Total Power Supply Current (Note 15)	lc	V _{CC} = Max, Outputs Open f _{CP} = 10MHz (CLKAB), 50% Duty Cycle OEAB = OEBA = V _{CC} LEAB = GND, f ₁ = 5MHz One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} - 0.6V V _{IN} = GND	-	0.6	2.3	mA
		V _{CC} = Max, Outputs Open f _{CP} = 10MHz (CLKAB), 50% Duty Cycle OEAB = OEBA = V _{CC} LEAB = GND, f ₁ = 2.5MHz Eightteen Bits Toggling 50% Duty Cycle	V _{IN} = V _{CC} - 0.6V V _{IN} = GND	-	2.1	4.7 (Note 14)	mA

Switching Specifications Over Operating Range (Note 16)

		(NOTE 17)	CD74LPT16501		CD74LPT16501A		
PARAMETER	SYMBOL	TEST CONDITIONS	(NOTE 18) MIN	MAX	(NOTE 18) MIN	MAX	UNITS
CLKAB or CLKBA frequency	t _{MAX}	$C_L = 50 pF$ $R_L = 500 \Omega$		100		150	ns
Propagation Delay A _X to B _X or B _X to A _X	t _{PLH,} t _{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	6.5	1.5	5.1	ns
Propagation Delay LEBA to A _X , LEAB to B _X	tplH, tpHL	C _L = 50pF R _L = 500Ω	1.5	7.5	1.5	5.6	ns
Propagation Delay CLKBA to A_{χ} , CLKAB to B_{χ}	t _{РLН,} t _{РHL}	C _L = 50pF R _L = 500Ω	1.5	8.0	1.5	5.6	ns
Output Enable Time OEBA to A _X . OEAB to Bx	^t PZH. ^t PZL	$C_L = 50pF$ $R_L = 500\Omega$	1.5	8.0	1.5	6.0	ns
Output Disable Time (Note 19) OEBA to A _X . OEAB to B _X	tpHZ tpLZ	$C_L = 50pF$ $R_L = 500\Omega$	1.5	7.5	1.5	5.6	ns

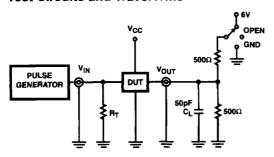
Switching Specifications Over Operating Range (Note 16) (Continued)

		(NOTE 17)	CD74LF	T16501	CD74LP	T16501A	
PARAMETER	SYMBOL	TEST CONDITIONS	(NOTE 18) MIN	MAX	(NOTE 18) MIN	MAX	UNITS
Setup Time HIGH or LOW A _X to CLKAB, B _X to CLKBA	ts∪	C _L = 50pF R _L = 500Ω	4.0	-	3.0	• •	ns
Hold Time HIGH or LOW A _X to CLKAB, B _X to CLKBA	tн	C _L = 50pF R _L = 500Ω	0	•	0	· ·	ns
Setup Time HIGH or LOW, A _X to LEAB, B _X to LEBA, Clock HIGH	tsu	C _L = 50pF R _L = 500Ω	4.0	-	3.0	•	ns
Setup Time HIGH or LOW, A _X to LEAB, B _X to LEBA, Clock LOW	tsu	C _L = 50pF R _L = 500Ω	1.5	-	1.5	-	ns
Hold Time HIGH or LOW, Ax to LEAB, Bx to LEBA	tн	C _L = 50pF R _L = 500Ω	1.5	-	1.5	-	ns
LEAB or LEBA Pulse Width HIGH (Note 19)	tw	C _L = 50pF R _L = 500Ω	3.0	•	3.0	-	ns
CLKAB or CLKBA Pulse Width HIGH or LOW (Note 19)	t _W	C _L = 50pF R _L = 500Ω	3.0	-	3.0	-	ns
Output Skew (Note 20)	tsk(O)	C _L = 50pF R _L = 500Ω		0.5		0.5	ns

NOTES:

- 6. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
- Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading, except as noted.
- 8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
- 9. This parameter is guaranteed but not tested.
- 10. VOH = VCC 0.6V at rated current.
- 11. This parameter is determined by device characterization but is not production tested.
- 12. Per TTL driven input; all other inputs at V_{CC} or GND.
- 13. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- 14. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- 15. IC = QUIESCENT + INPUTS + IDYNAMIC
 - IC = ICC + AICC DHNT + ICCD (ICP/2 + IN)
 - I_{CC} = Quiescent Current
 - ΔI_{CC} = Power Supply Current for a TTL High Input
 - DH = Duty Cycle for TTL Inputs High
 - NT = Number of TTL Inputs at DH
 - I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 - f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 - f_I = Input Frequency
 - N_i = Number of Inputs at f_i
 - All currents are in milliamps and all frequencies are in megahertz.
- 16. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
- 17. See test circuit and wave forms.
- 18. Minimum limits are guaranteed but not tested on Propagation Delays.
- 19. This parameter is guaranteed but not production tested.
- 20. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



NOTE:

21. Pulse Generator for All Pulses: Rate \leq 1.0MHz; $Z_{OUT} \leq$ 50 Ω ; $t_{\rm f}, t_{\rm f} \leq$ 2.5ns.

FIGURE 1. TEST CIRCUIT

TEST SWITCH t_{PLZ}, t_{PZL}, Open Drain 6V t_{PHZ}, t_{PZH} GND t_{PLH}, t_{PHL} Open

SWITCH POSITION

DEFINITIONS:

 C_L = Load capacitance, includes jig and probe capacitance. R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

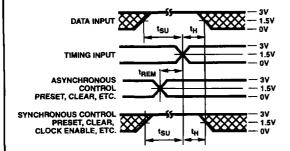


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

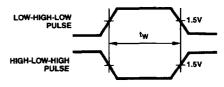


FIGURE 3. PULSE WIDTH

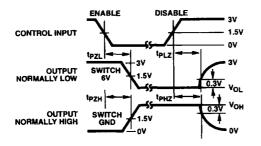


FIGURE 4. ENABLE AND DISABLE TIMING

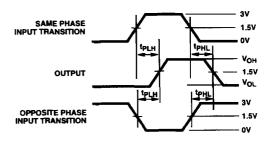


FIGURE 5. PROPAGATION DELAY