Dual 1A, 1.5MHz PWM Step-down DC-DC Converter with OVP AUR9717

General Description

The AUR9717 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized using constant frequency, peak-current mode architecture with built-in synchronous power MOSFET switchers and internal compensators to reduce external part counts. It is automatically switching between the normal PWM mode and LDO mode to offer improved system power efficiency covering a wide range of loading conditions.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use of small surface mount inductors and capacitors for portable product implementations. Additional features including Soft Start (SS), Under Voltage Lock Out (UVLO), Input Over Voltage Protection (IOVP) and Thermal Shutdown Detection (TSD) are integrated to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 1V to 3.3V, and is able to deliver up to 1A.

The AUR9717 is available in WDFN-3×3-10 package.

Features

- Dual Channel High Efficiency Buck Power Converter
- Low Quiescent Current
- Output Current: 1A
- Adjustable Output Voltage from 1V to 3.3V
- Wide Operating Voltage Range: 2.5V to 5.5V
- Built-in Power Switchers for Synchronous Rectification with High Efficiency
- Feedback Voltage: 600mV
- 1.5MHz Constant Frequency Operation
- Automatic PWM/LDO Mode Switching Control
- Thermal Shutdown Protection
- Low Drop-out Operation at 100% Duty Cycle
- No Schottky Diode Required
- Internal Input Over Voltage Protection
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
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Applications

- Mobile Phone, Digital Camera and MP3 Player
- Headset, Radio and Other Hand-held Instruments
- Post DC-DC Voltage Regulation
- PDA and Notebook Computer

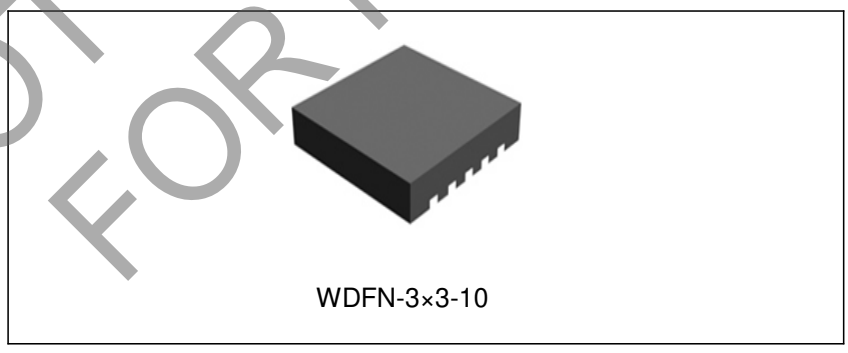


Figure 1. Package Type of AUR9717

Pin Configuration

D Package
(WDFN-3×3-10)

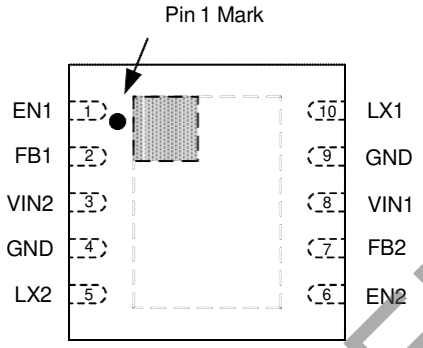


Figure 2. Pin Configuration of AUR9717 (Top View)

Pin Description

Pin Number	Pin Name	Function
1	EN1	Enable signal input of channel 1, active high
2	FB1	Feedback voltage of channel 1
3	VIN2	Power supply input of channel 2
4, 9	GND	This pin is the GND reference for the NMOSFET power stage. It must be connected to the system ground
5	LX2	Connection from power MOSFET of channel 2 to inductor
6	EN2	Enable signal input of channel 2, active high
7	FB2	Feedback voltage of channel 2
8	VIN1	Power supply input of channel 1
10	LX1	Connection from power MOSFET of channel 1 to inductor

Functional Block Diagram

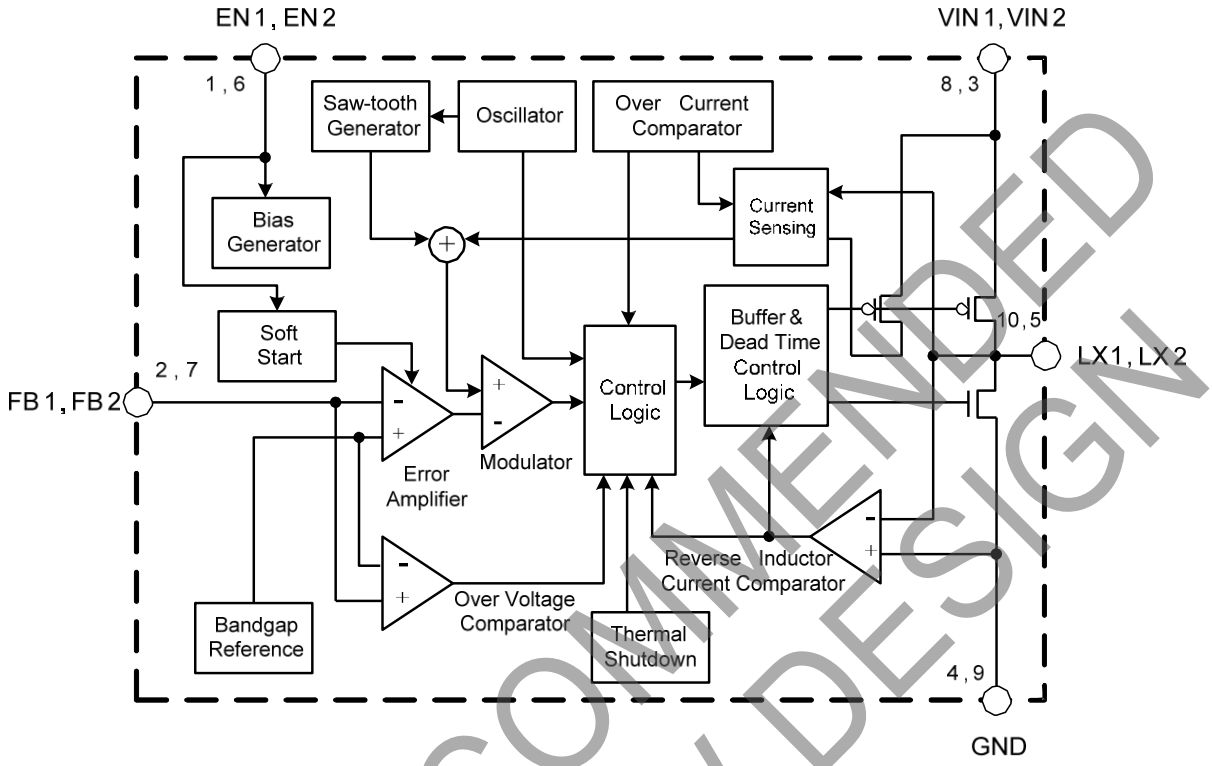
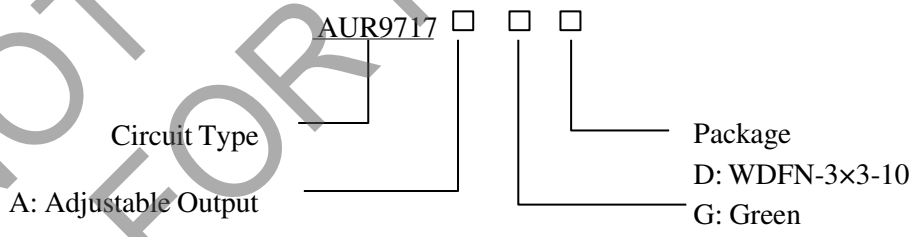


Figure 3. Functional Block Diagram of AUR9717

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
WDFN-3×3-10	-40 to 80°C	AUR9717AGD	9717A	Tape & Reel

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Supply Input Voltage	V_{IN1}, V_{IN2}	0 to 6.5	V
Enable Input Voltage	V_{EN1}, V_{EN2}	-0.3 to V_{IN1}(V_{IN2})+0.3	V
Switch Output Voltage	V_{LX1}, V_{LX2}	-0.3 to V_{IN1}(V_{IN2})+0.3	V
V_{IN1}-V_{IN2} Voltage (Note 2)	V_{DF}	-0.3 to 0.3	V
Power Dissipation (On PCB, T_A=25°C)	P_D	2.22	W
Thermal Resistance (Junction to Ambient, Simulation)	θ_{JA}	45.13	°C/W
Thermal Resistance (Junction to Case, Simulation)	θ_{JC}	6.97	°C/W
Operating Junction Temperature	T_J	160	°C
Operating Temperature	T_{OP}	-40 to 85	°C
Storage Temperature	T_{STG}	-55 to 150	°C
ESD (Human Body Model)	V_{HBM}	2000	V
ESD (Machine Model)	V_{MM}	200	V

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Note 2: The absolute voltage difference between V_{IN1} and V_{IN2} can not exceed 0.3V.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Input Voltage	V_{IN1}, V_{IN2}	2.5	5.5	V
Junction Temperature Range	T_J	-20	125	°C
Ambient Temperature Range	T_A	-40	80	°C

Electrical Characteristics

V_{IN}=V_{EN1}=V_{EN2}=5V, V_{FB1}=V_{FB2}=0.6V, L1=L2=2.2μH, C_{IN1}=C_{IN2}=4.7μF, C_{OUT1}=C_{OUT2}=10μF, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	V_{IN}=V_{IN1}=V_{IN2}	2.5		5.5	V
Shutdown Current	I_{OFF}	V_{EN1}=V_{EN2}=0V		0.1	1	μA
Regulated Feedback Voltage	V_{FB}	For Adjustable Output Voltage	0.585	0.6	0.615	V
Regulated Output Voltage Accuracy	$\Delta V_{OUT1}/V_{OUT1}$, $\Delta V_{OUT2}/V_{OUT2}$	V_{IN}=2.5V to 5.5V, I_{OUT1}=I_{OUT2}=0 to 1A	-3		3	%
Peak Inductor Current	I_{PK}	V_{FB1}=V_{FB2}=0.5V		1.5		A
Oscillator Frequency	f_{OSC}		1.2	1.5	1.8	MHz
PMOSFET R_{ON}	$R_{ON(P)}$	I_{OUT1}=I_{OUT2}=200mA		0.28		Ω
NMOSFET R_{ON}	$R_{ON(N)}$	I_{OUT1}=I_{OUT2}=200mA		0.25		Ω
LX Leakage Current	I_{LX}	V_{EN1}=V_{EN2}=0V, V_{LX1}=V_{LX2}=0V or 5V		0.01	0.1	μA
Feedback Current	I_{FB1}, I_{FB2}				30	nA
Input Over Voltage Protection	V_{IOVP}			6		V
EN Leakage Current	I_{EN1}, I_{EN2}			0.01	0.1	μA
EN High-level Input Voltage	V_{EN_H1}, V_{EN_H2}	V_{IN}=2.5V to 5.5V	1.5			V
EN Low-level Input Voltage	V_{EN_L1}, V_{EN_L2}	V_{IN}=2.5V to 5.5V			0.6	V
Under Voltage Lock Out	V_{UVLO}	Rising		1.8		V
Hysteresis		Hysteresis		0.1		V
Thermal Shutdown	T_{SD}			160		°C

Typical Performance Characteristics

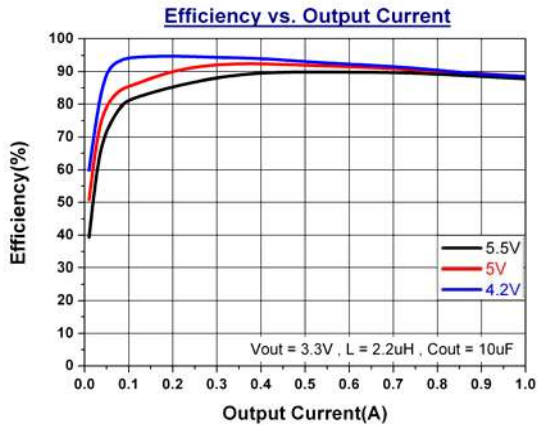


Figure 4. Efficiency vs. Output Current

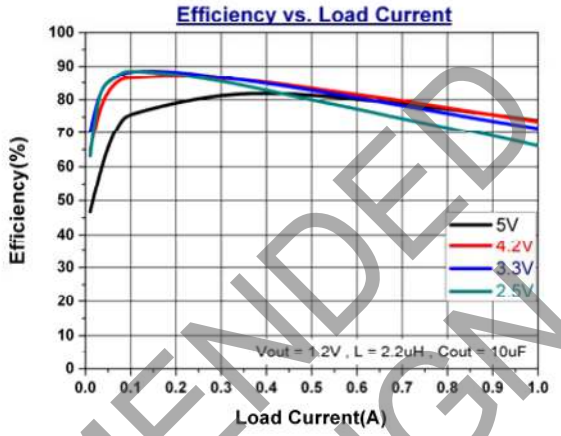


Figure 5. Efficiency vs. Load Current

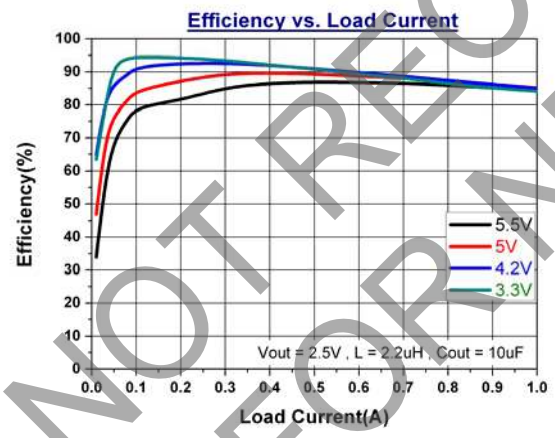


Figure 6. Efficiency vs. Load Current

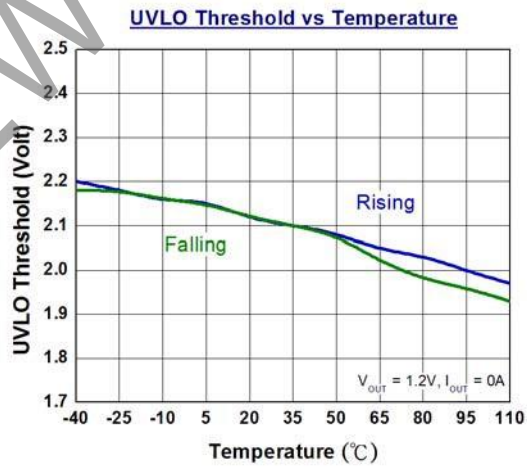


Figure 7. UVLO Threshold vs. Temperature

Typical Performance Characteristics (Continued)

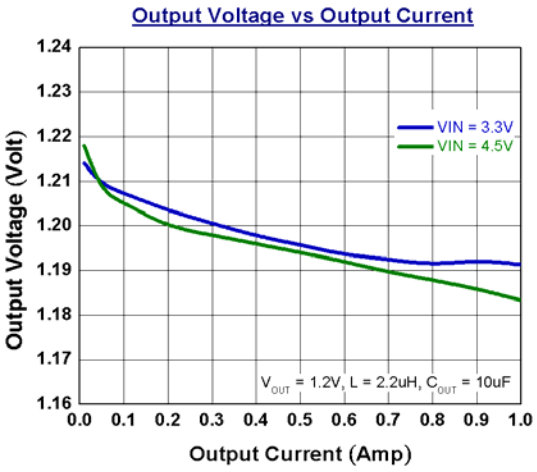


Figure 8. Output Voltage vs. Output Current

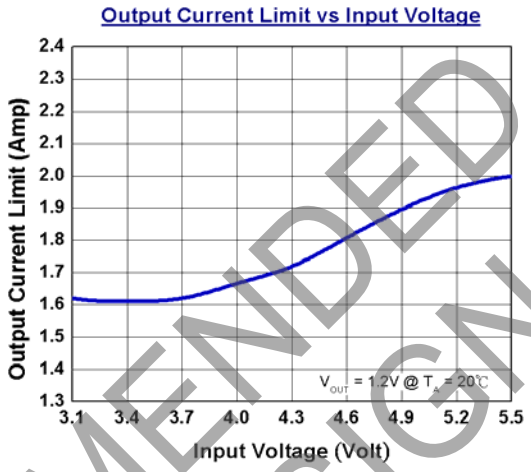


Figure 9. Output Current Limit vs. Input Voltage

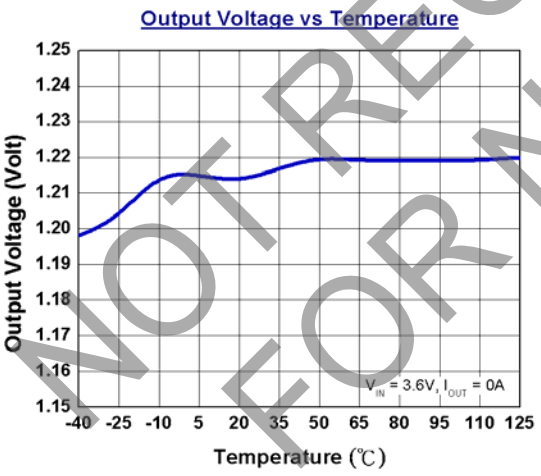


Figure 10. Output Voltage vs. Temperature

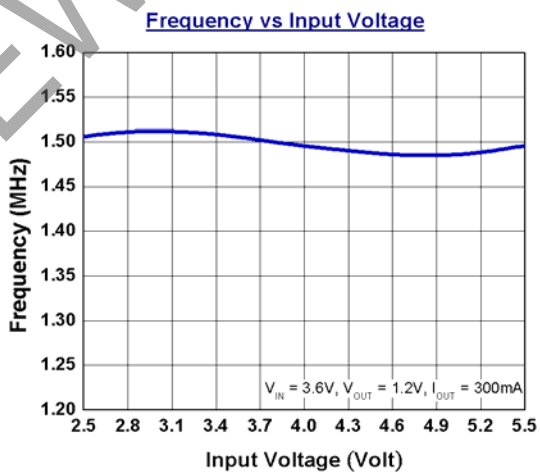


Figure 11. Frequency vs. Input Voltage

Typical Performance Characteristics (Continued)

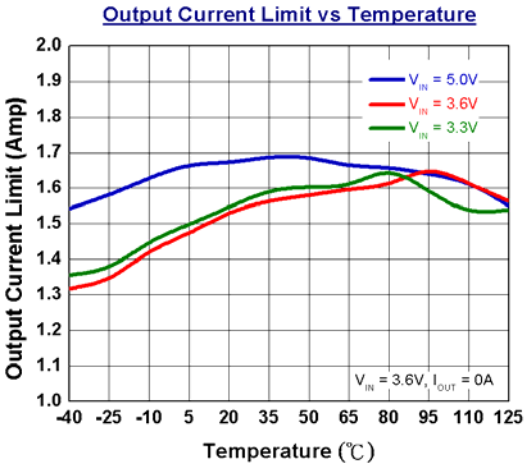


Figure 12. Output Current Limit vs. Temperature

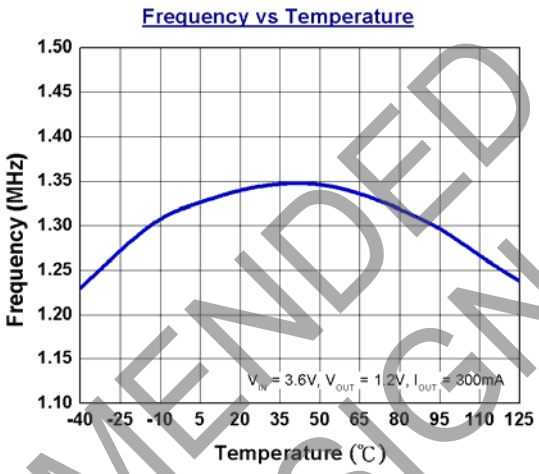


Figure 13. Frequency vs. Temperature

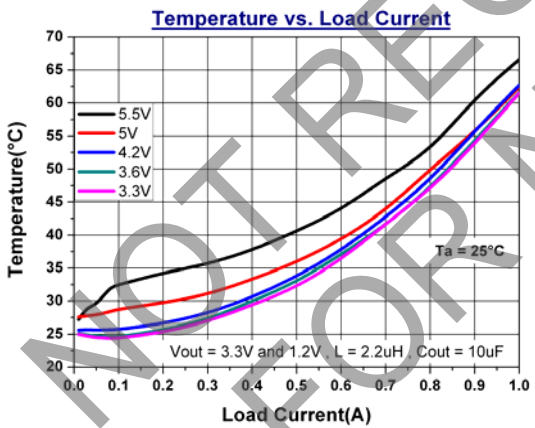


Figure 14. Temperature vs. Load Current

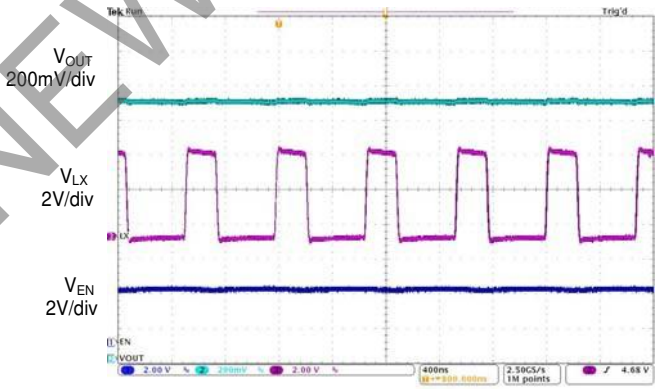


Figure 15. Waveform of V_{IN}=4.5V, V_{OUT}=1.5V, L=2.2μH

Typical Performance Characteristics (Continued)

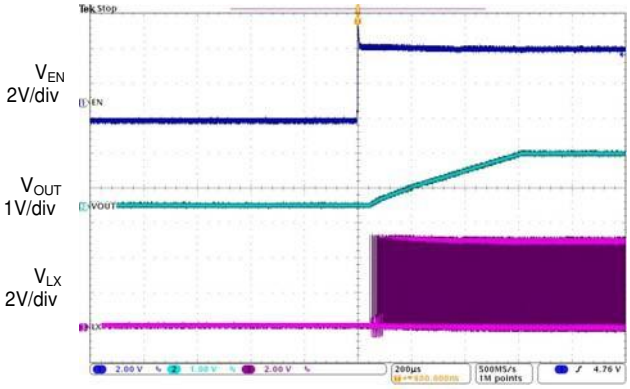


Figure 16. Soft Start

Application Information

The basic AUR9717 application circuit is shown in Figure 18.

1. Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 2.2μH to 4.7μH.

$$\Delta I_L = \frac{1}{f \times L} V_{OUT} (1 - \frac{V_{OUT}}{V_{IN}})$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, larger value inductors will be required. A reasonable starting point for ripple current setting is $\triangle I_L$=40%I_{MAX}. For a maximum ripple current stays below a specified value, the inductor should be chosen according to the following equation:

$$L = [\frac{V_{OUT}}{f \times \Delta I_L (MAX)}][1 - \frac{V_{OUT}}{V_{IN}(MAX)}]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, a lower DC-resistance inductor should be selected.

2. Capacitor Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at V_{IN}=2V_{OUT}, where I_{RMS}=I_{OUT}/2. This simple worse-case condition is commonly used for design because even significant deviations do not much relieve. The selection of C_{OUT} is determined by the Effective Series Resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure that the control loop is stable. Loop stability can be also checked by viewing the load step transient response as described in the following section. The output ripple, $\triangle V_{OUT}$, is determined by:

$$\Delta V_{OUT} \leq \Delta I_L [ESR + \frac{1}{8 \times f \times C_{OUT}}]$$

The output ripple is the highest at the maximum input voltage since $\triangle I_L$ increases with input voltage.

3. Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\triangle I_{LOAD}$×ESR, where ESR is the effective series resistance of output capacitor. $\triangle I_{LOAD}$ also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During the recovery time, V_{OUT} can be monitored for overshoot or ringing that would

4. Output Voltage Setting

The output voltage of AUR9717 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{FB} \times (1 + \frac{R_1}{R_2}) = 0.6V \times (1 + \frac{R_1}{R_2})$$

The resistive divider senses the fraction of the output voltage as shown in Figure 17.

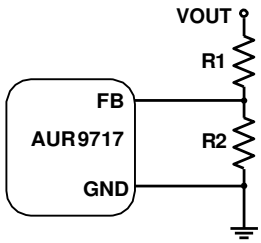


Figure 17. Setting the Output Voltage

Application Information (Continued)

5. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

Efficiency=100%-L1-L2-…..

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses: V_{IN} quiescent current and I^2R losses. The V_{IN} quiescent current loss dominates the efficiency loss at very light load currents and the I^2R loss dominates the efficiency loss at medium to heavy load currents.

5.1 The V_{IN} quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge, dQ moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the internal DC bias current. In continuous mode,

$$I_{GATE} = f \times (Q_P + Q_N)$$

Where Q_P and Q_N are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the V_{IN} and this effect will be more serious at higher input voltages.

5.2 I^2R losses are calculated from internal switch resistance, R_{SW} and external inductor resistance R_L. In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the LX pin is a function of both PMOSFET $R_{DS(ON)P}$ and NMOSFET $R_{DS(ON)N}$ resistance and the duty cycle (D):

$$R_{SW} = R_{DS(ON)P} \times D + R_{DS(ON)N} \times (1 - D)$$

Therefore, to obtain the I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% of total additional loss.

6. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high $R_{DS(ON)}$ resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

7. PC Board layout considerations

When laying out the printed circuit board, the following checklist should be used to optimize the performance of AUR9717.

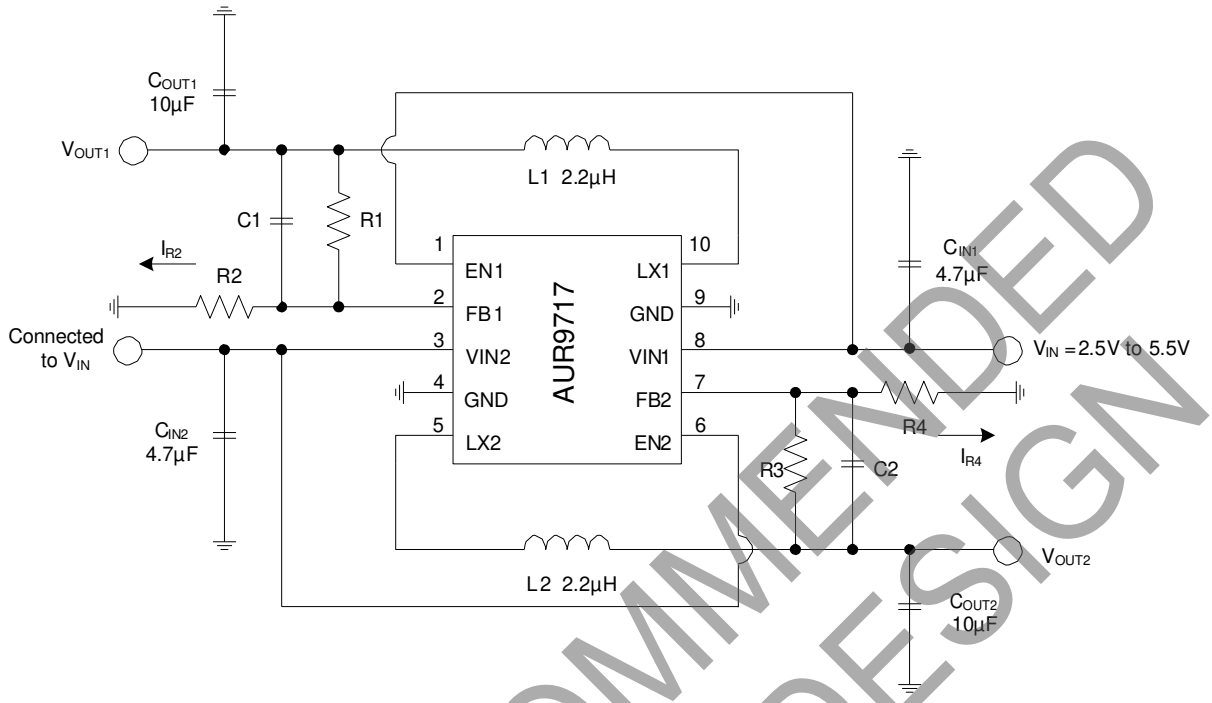
1. The power traces, including the GND trace, the LX trace and the VIN trace should be kept direct, short and wide.

2. Put the input capacitor as close as possible to the VIN and GND pins.

3. The FB pin should be connected directly to the feedback resistor divider.

4. Keep the switching node LX away from the sensitive FB pin and the node should be kept small area.

Typical Application



Note 3: $V_{OUT1} = V_{FB1} \times (1 + \frac{R_1}{R_2})$; $V_{OUT2} = V_{FB2} \times (1 + \frac{R_3}{R_4})$

When R2 or R4=300kΩ to 60kΩ, the I_{R2} or I_{R4}=2µA to 10µA, and R1×C1 or R3×C2 should be in the range between 3×10^{-6} and 6×10^{-6} for component selection.

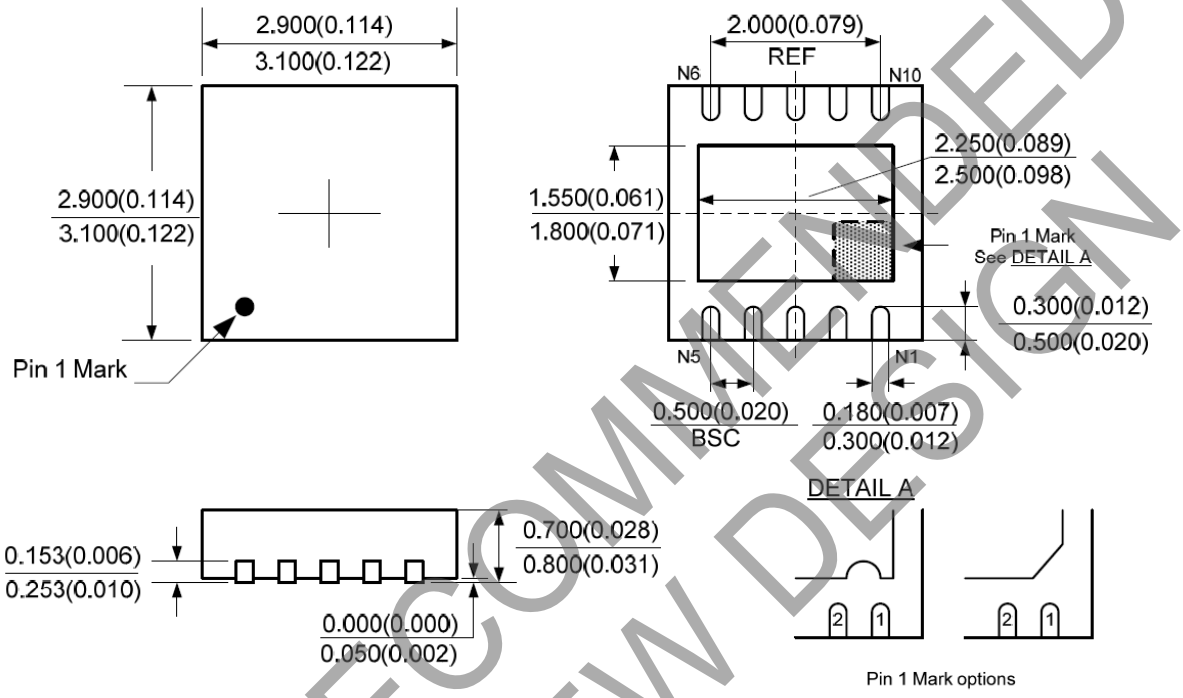
Figure 18. Typical Application Circuit of AUR9717 (Note 3)

Table 1. Component Guide

V_{OUT1} or V_{OUT2} (V)	R1 or R3 (kΩ)	R2 or R4 (kΩ)	C1 or C2 (pF)	L1 or L2 (µH)
3.3	453	100	13	2.2
2.5	320	100	18	2.2
1.8	200	100	30	2.2
1.2	100	100	56	2.2
1.0	68	100	82	2.2

Mechanical Dimensions

WDFN-3×3-10 **Unit: mm(inch)**



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