19-4564; Rev 0; 4/09

EVALUATION KIT AVAILABLE

7-Bit, Programmable VCOM Reference with 30x MOTP Memory

MAX9660

General Description

The MAX9660 provides a programmable reference voltage for VCOM adjustment in TFT-LCD panels. A 7-bit, current digital-to-analog converter (DAC) sinks current from an external resistor-divider string to create the VCOM reference voltage, which then serves as the input to a voltage buffer capable of driving out high current.

The MAX9660 includes multiple one-time programmable (MOTP) memory to store the DAC code on the chip, eliminating the need for external EEPROM. The chip supports up to 30 write operations to MOTP memory.

The MAX9660 has an I²C interface to set the VCOM reference voltage and write into MOTP memory.

Applications

TFT-LCD Panels

Instrumental Control Voltage Source

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9660ATA+	-40°C to +125°C	8 TDFN-EP*

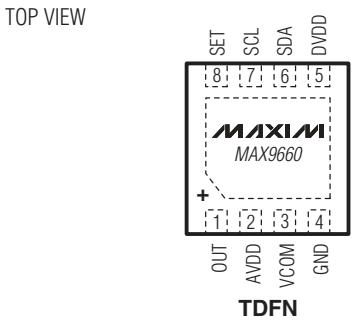
+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Features

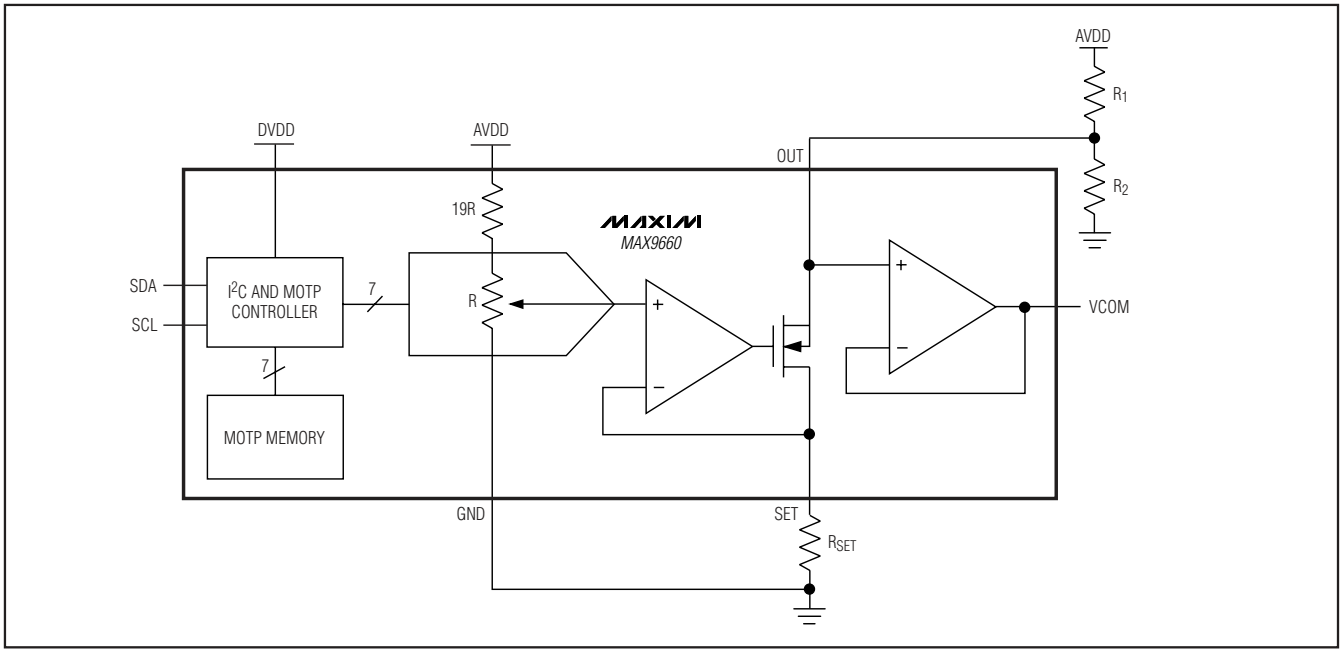
- **VCOM Amplifier with 900mA Peak Output Current**
- **Integrated Nonvolatile Memory to Store VCOM Setting**
- **7-Bit, Adjustable Sink-Current Device**
- **Resistor-Adjustable, Full-Scale Range**
- **2.5V to 3.6V Logic Supply Range**
- **8V to 20V Analog Supply Range**

Pin Configuration



TDFN

Functional Diagram



7-Bit, Programmable VCOM Reference with 30x MOTP Memory

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- DVDD, SET, SCL, and SDA to GND .....-0.3V to +4V
- AVDD to GND .....-0.3V to +22V
- OUT to GND .....-0.3V to +22V
- VCOM to GND .....-0.3V to AVDD + 0.3V

Continuous Current
- SDA 10mA
- VCOM .....±100mA

Continuous Power Dissipation (T_A = +70°C)
- 8-Pin TDFN-EP (derate 18.5mW/°C above +70°C)
  - Single-Layer Board 1481mW
- 8-Pin TDFN-EP (derate 24.4mW/°C above +70°C)
  - Multilayer Board 1951mW

Operating Temperature Range .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DVDD} = 3.3V, V_{AVDD} = 16V, V_{GND} = 0, R_{SET} = 6.8kΩ, no load, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLIES						
Digital Supply Voltage Range	V_{DVDD}		2.5	3.3	3.6	V
Analog Supply Voltage Range	V_{AVDD}		8		20	V
Analog Quiescent Current	I_{AVDD}			4.5	10	mA
Analog Supply Current Range for Programming MOTP	I_{AVDD}	T_A = +25°C		15	20	mA
		T_A = +85°C			45	
Digital Quiescent Current	I_{DVDD}			200	500	µA
MOTP Programming Times	$MOTP_{SET}$		30			Times
VCOM OUTPUT (VCOM)						
Common-Mode Range			0.2		V_{AVDD} - 0.2	V
Total Output Error	V_{ERR}	T_A = +25°C, V_{VCOM} from 2V to V_{AVDD} - 2V	-22		+22	mV
Output Voltage Swing Low	V_{OL}	I_L = -5mA, V_{OUT} = 0			150	mV
Output Voltage Swing High	V_{OH}	I_L = +5mA, V_{OUT} = V_{AVDD}	V_{AVDD} - 150			mV
Output Load Regulation	LR	I_L = -80mA to +80mA		±0.2		mV/mA
Short-Circuit Current (Note 2)	I_{SC}	VCOM = AVDD		-900		mA
		VCOM = GND		+900		
Power-Supply Rejection Ratio	PSRR	8V ≤ V_{AVDD} ≤ 20V, V_{OUT} = 5V	70			dB
Slew Rate	SR	4V_{P-P} at VCOM, 10% to 90%, R_L = 10kΩ, C_L = 20pF		45		V/µs
Bandwidth	dB	R_L = 10kΩ, C_L = 20pF, V_{VCOM} = 100mV_{P-P}		20		MHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = 3.3V, V_{AVDD} = 16V, V_{GND} = 0, R_{SET} = 6.8kΩ, no load, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DVR						
OUT Voltage Range	V_{OUT}		V_{SET} + 0.5V		20	V
Resolution	RES		7			Bits
Integral Nonlinearity Error	INL			0.125		LSB
Differential Nonlinearity Error	DNL			0.125		LSB
AVDD to V_{SET} Ratio	AVDD/V_{SET}			20:1		V/V
Set External Resistance	R_{SET}	V_{AVDD} = 8V	3.35		67	kΩ
		V_{AVDD} = 18V	6.75		135	
Set Current	I_{SET}	Through R_{SET}			134	µA
Set Zero-Scale Error	SET_{ZSE}				±2	LSB
Set Full-Scale Error	SET_{FSE}				±4	LSB
LOGIC INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
SDA Output Low Voltage	V_{OL}	I_{SINK} = 6mA			0.4	V
Input Leakage Current	I_{IH}, I_{IL}	0V or V_{DVDD}	-3	0.01	+3	µA
Input Capacitance				5		pF
I²C TIMING CHARCTERISTICS						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time START Condition	$t_{HD, STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$		0		900	ns
Data Setup Time	$t_{SU, DAT}$	(Note 3)	100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 4)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 4)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	(Note 4)	20 + 0.1C_B		250	ns

7-Bit, Programmable VCOM Reference with 30x MOTP Memory

ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = 3.3V, V_{AVDD} = 16V, V_{GND} = 0, R_{SET} = 6.8kΩ, no load, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Short-circuit current is for a 1µs pulsed current only, not to exceed thermal characteristics of package.
Note 3: Data hold time is tested in receive mode only.
Note 4: C_B is in pF.

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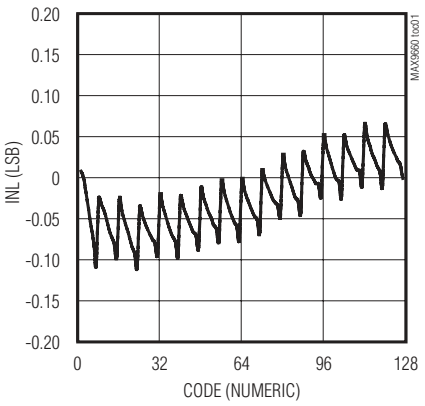
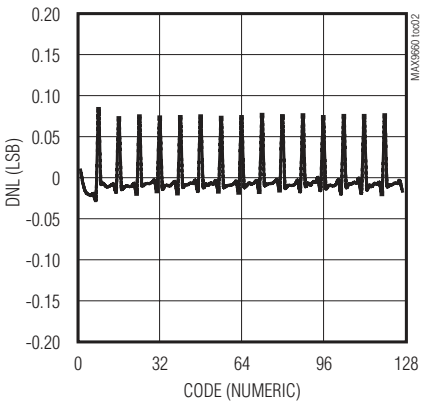
Typical Operating Characteristics

(*Typical Application Circuit*, V_{DVDD} = 3.3V, V_{AVDD} = 16V, R_{SET} = 7kΩ, R_1 = R_2 = 35kΩ, T_A = +25°C, unless otherwise noted.)

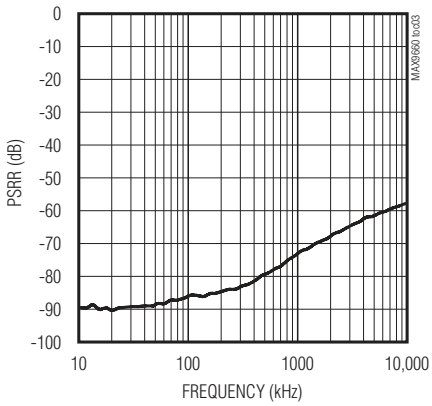
INL vs. CODE



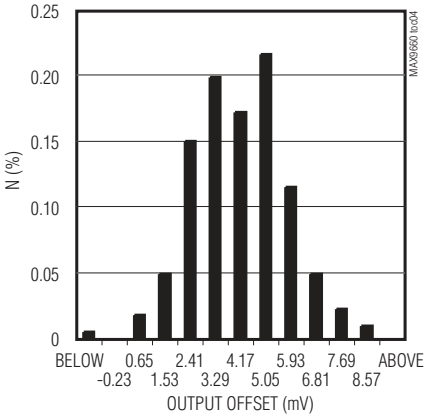
DNL vs. CODE



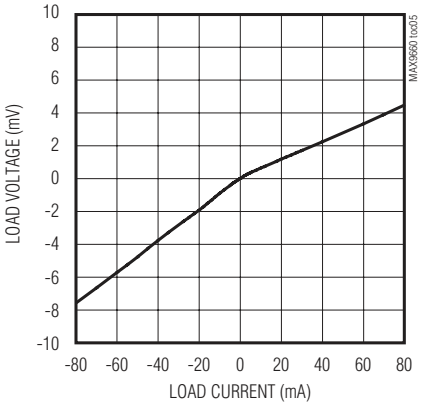
DAC PSRR vs. FREQUENCY



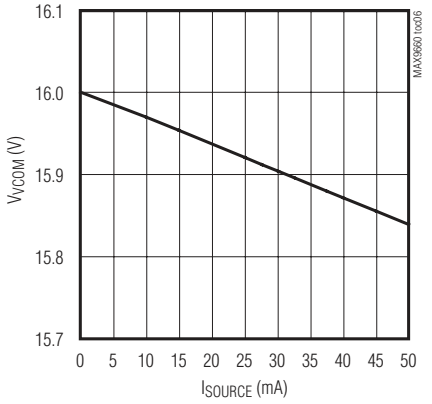
OUTPUT OFFSET VOLTAGE DISTRIBUTION



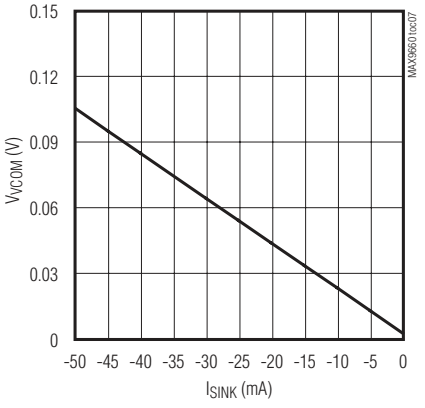
VCOM LOAD REGULATION



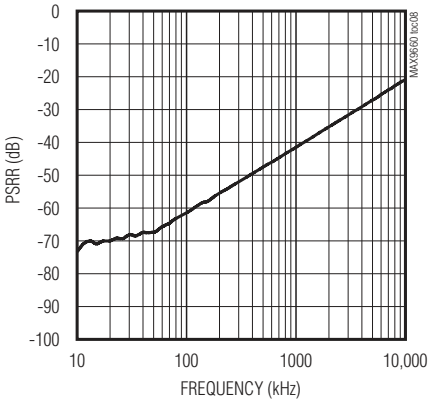
V_{VCOM} vs. I_{SOURCE}



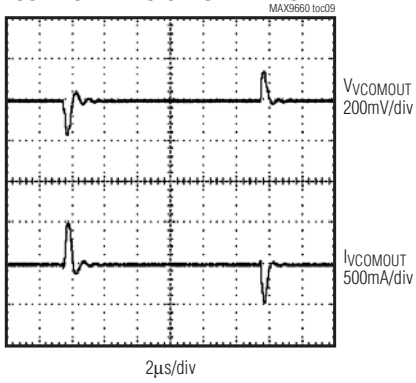
V_{VCOM} vs. I_{SINK}



VCOM PSRR vs. FREQUENCY



VCOM BUFFER PULSE LOAD TRANSIENT



7-Bit, Programmable VCOM Reference with 30x MOTP Memory

Pin Description

PIN	NAME	FUNCTION
1	OUT	Adjustable Sink Current for Integrated VCOM Voltage Buffer. OUT connects to the resistive voltage-divider between AVDD and GND.
2	AVDD	Analog Power Supply. Bypass AVDD with 0.1µF and 10µF capacitors in parallel to GND.
3	VCOM	VCOM Output
4	GND	Ground
5	DVDD	Digital Power Supply. Bypass DVDD with 0.1µF capacitor to GND.
6	SDA	I²C-Compatible Serial-Data Input/Output
7	SCL	I²C-Compatible Serial-Clock Input
8	SET	Full-Scale Sink-Current Adjustment Input. Connect a resistor, R_{SET}, from SET to GND to set the full-scale adjustable sink current. The full-scale adjustable sink current is equal to: $\left(\frac{V_{AVDD}}{20 \times R_{SET}}\right)$
—	EP	Exposed Pad. Connect EP to GND.

Detailed Description

The MAX9660, a programmable VCOM buffer, replaces the mechanical potentiometer that is used for adjusting the VCOM voltage with an electrical solution (see the *Typical Application Circuit*). The MAX9660 attaches to an external resistor-divider (resistors R_1 and R_2) and sinks a programmable current I_{OUT} to create the VCOM reference voltage. The resolution of the current DAC that generates I_{OUT} is 7 bits. The DAC is ratiometric relative to V_{AVDD} and is monotonic over all operating conditions. The external resistor R_{SET} sets the full-scale sink current and the minimum value of the VCOM reference voltage. The external resistor-divider and the AVDD supply set the maximum value of the VCOM reference voltage.

The VCOM reference voltage is the input to the integrated voltage buffer, which can source and sink 900mA so that VCOM can quickly recover after a polarity inversion or a horizontal line change. The MAX9660 features output short-circuit protection and soft-start to reduce inrush current.

The user can store the DAC setting in a type of nonvolatile memory known as MOTP. On power-up, MOTP sets the DAC register to the last stored setting. The DAC register and the MOTP can be programmed through the I²C interface.

7-Bit DAC

An internal 7-bit DAC sinks current I_{OUT}. The following equations determine the value of I_{OUT}:

$$I_{OUT} = \left(\frac{CODE+1}{2^N}\right) \times \left(\frac{V_{AVDD}}{20 \times R_{SET}}\right)$$

where CODE is the numeric value of the DAC's binary input code and N is the bits of resolution. For the MAX9660, N = 7 and CODE ranges from 0 to 127.

The MAX9660 pulls I_{OUT} through the external resistor-divider comprised of R_1 and R_2. The resulting voltage V_{OUT} is given by the following formula:

$$V_{VCOM} = \left(\frac{R_2}{R_1+R_2}\right) \times V_{AVDD} \times \left(1 - \left(\frac{CODE+1}{128}\right)\left(\frac{R_1}{20 \times R_{SET}}\right)\right)$$

VCOM Amplifier

The buffer attached to V_{OUT} holds the VCOM voltage stable while providing the ability to source and sink 900mA into the backplane of a TFT-LCD panel. The buffer can directly drive the capacitive load of the TFT-LCD backplane without the need for a series resistor in most cases. The VCOM amplifier has current limiting on its output to protect its bond wires.

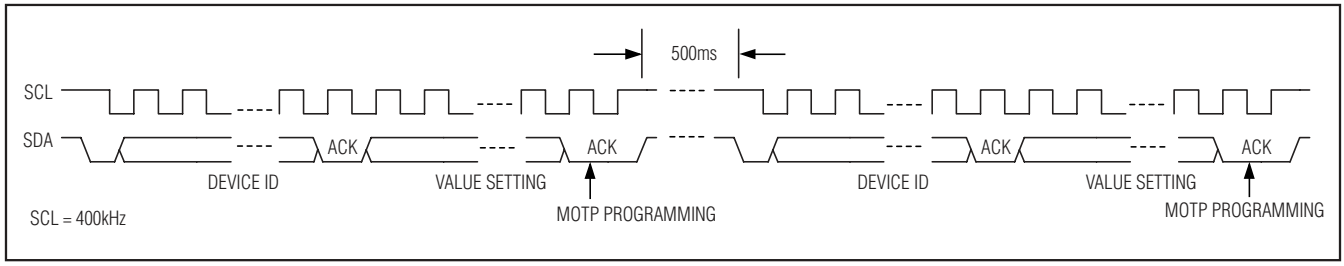


Figure 1. MOTP programming interval. Wait 500ms after issuing a write command to MOTP memory before starting another write command to MOTP memory.

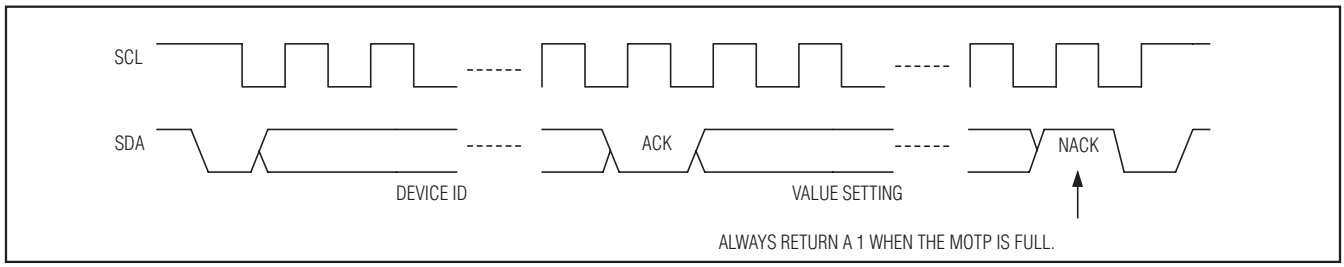


Figure 2. Example of a write command to MOTP memory after MOTP memory is full. The MAX9660 responds with a NACK.

Multiple One-Time Programmable Memory (MOTP) Programming

DAC codes can be written into MOTP memory up to 30 times because the MOTP memory is a bank of 30 one-time programmable registers. See the *Write Data Format* section for a description of how to use the I²C interface to write data into MOTP.

After an I²C write operation to MOTP memory, the MAX9660 requires a maximum of 500ms to burn the data into the MOTP register (see Figure 1). During this time, do not perform another write operation to MOTP memory. If a write operation to MOTP memory is attempted during this time, the MAX9660 responds with a not acknowledge (NACK).

The MAX9660 integrates MOTP memory that can be programmed 30 times. After 30 writes to MOTP memory, the MAX9660 responds with a not acknowledge (NACK) to all future write attempts (see Figure 2).

I²C Serial Interface

The MAX9660 features an I²C/SMBus™-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9660 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the MAX9660 by transmitting the proper slave address followed by the data word. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each word transmitted to the MAX9660 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX9660 transmits the proper slave address followed by a series of nine SCL pulses. The MAX9660 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on the SDA bus. SCL operates as only an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9660 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

SMBus is a trademark of Intel Corp.

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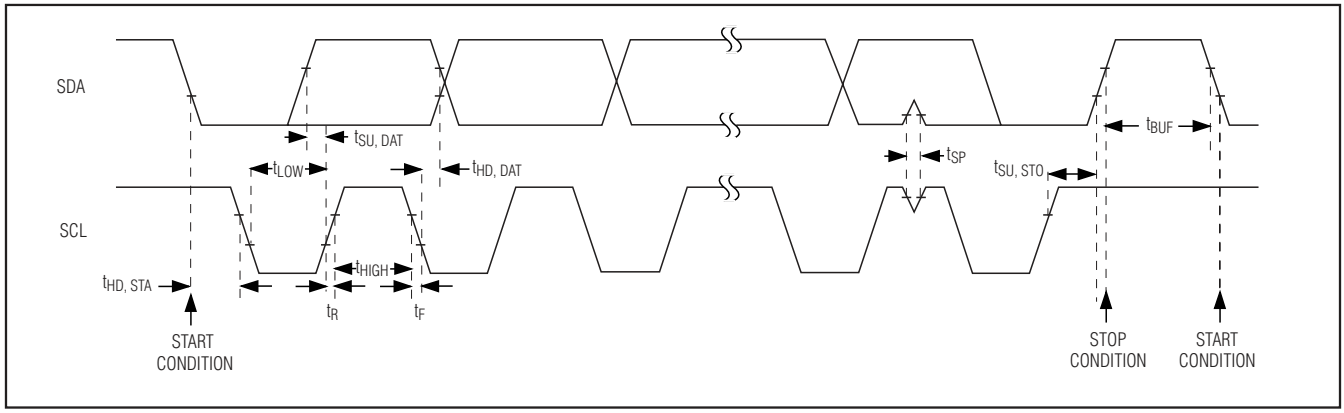

Figure 3. I²C Serial-Interface Timing Diagram

Table 1. Slave Address

B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS	READ ADDRESS
1	0	0	1	1	1	1	R/$\overline{W}$	0x9E	0x9F

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the MAX9660. The master terminates transmission, and frees the bus, by issuing a STOP condition.

Early STOP Conditions

The MAX9660 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write (R/$\overline{W}$) bit. Set the R/$\overline{W}$ bit to 1 to configure the MAX9660 to read mode. Set the R/$\overline{W}$ bit to 0 to configure the MAX9660 to write mode. The address is the first byte of information sent to the MAX9660 after the START condition. Table 1 shows the possible addresses for the MAX9660.

Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the MAX9660 uses to handshake receipt of each byte of data when in write mode (see Figure 5). The MAX9660 pulls down SDA during the entire master-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may retry communication. The master pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the MAX9660 is in read mode. An acknowledge bit is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge bit is sent when the master reads the final byte of data from the MAX9660, followed by a STOP condition.

Write Data Format

A write to the MAX9660 consists of transmitting a START condition, the slave address with the R/$\overline{W}$ bit set to 0, 7-bit data, M bit, and a STOP condition. Figure 6 illustrates the proper frame format for writing 7 bits of data to the MAX9660. The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write

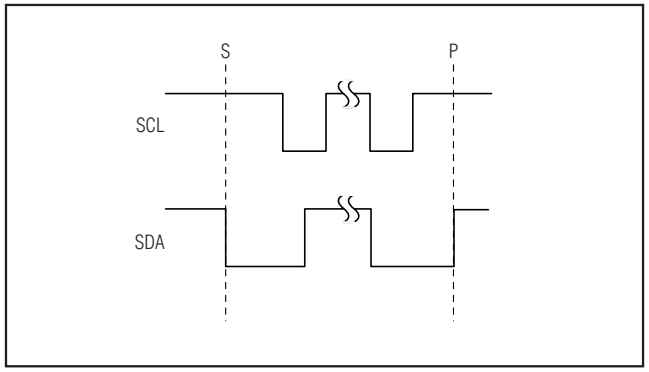

Figure 4. START and STOP Conditions

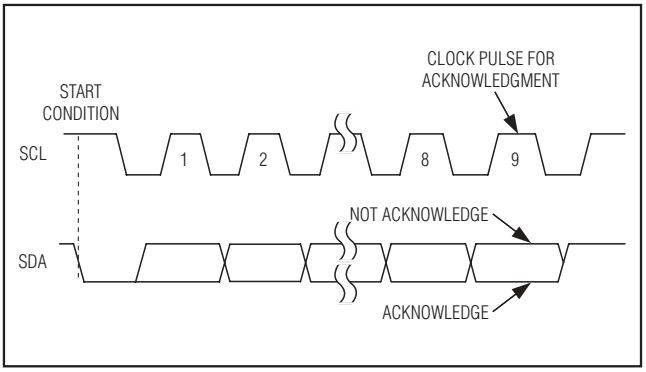

Figure 5. Acknowledge

Register Map

REG	B7	B6	B5	B4	B3	B3	B1	B0	FACTORY INITIALIZATION	R/$\overline{W}$
VCOM	d6	d5	d4	d3	d2	d1	d0	M	64	R/$\overline{W}$

Table 2. I2C Register

BITS	DESCRIPTION
B7:B1	7-bit DAC data
B0	Data location indicator (M bit). The M bit identifies the register for the data to be written to. M = 0, the data is written to the MOTP register. M = 1, the data is written to the DAC register.

data to the MAX9660. The MAX9660 acknowledges receipt of the address byte during the master-generated ninth SCL pulse. The second byte sent to the MAX9660 contains the 7-bit data that is written to the DAC latch or MOTP. The M bit after bit B1 identifies the register to be written to, as shown in Table 2. When M = 0, the MOTP is written to, and when M = 1, the DAC register is written to. An acknowledge pulse from the MAX9660 signals receipt of the VCOM data byte. The master signals the end of transmission by issuing a STOP condition.

Read Data Format

The master presets the address pointer by first sending the MAX9660's slave address with the R/$\overline{W}$ bit set to 1 after a START condition. The MAX9660 acknowledges receipt of its slave address and the register address by pulling SDA low during the ninth SCL clock pulse. The MAX9660 transmits the contents of the DAC register as 7-bit data and the eighth bit, M, is don't care. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). A STOP condition is issued after reading the data byte. The master acknowledges receipt of the read byte during the acknowledge clock pulse. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 7 illustrates the frame format for reading data from the MAX9660.

Applications Information

Power-Up and Power-Down Operation

During power-up, the digital supply must be powered up first. The analog supply should not be powered up until the digital supply has stabilized. During this time, the MOTP register value is loaded into the DAC register (0x40 is the factory-programmed default). Once AVDD is above approximately 7V, the VCOM amplifier has enough headroom and powers up proportionally with AVDD.

For power-down, AVDD must be powered down first to 0V, and then DVDD can safely be powered down.

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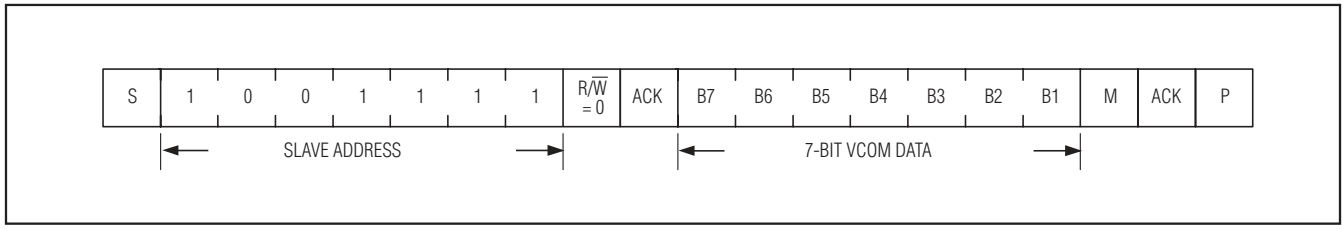


Figure 6. Write Operation to MOTP or DAC Register

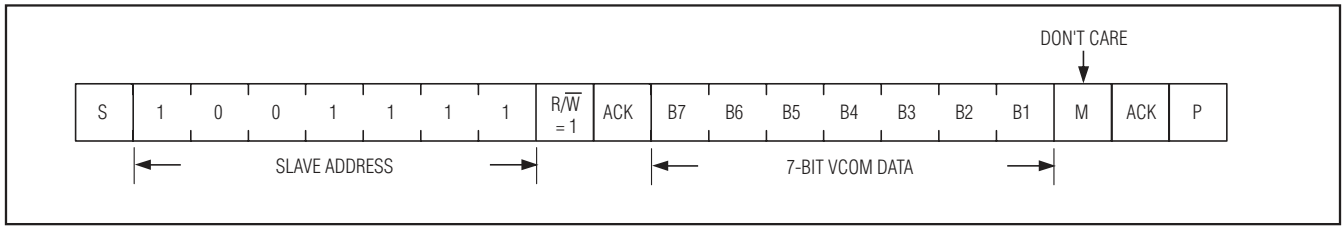


Figure 7. Read Operation to MOTP or DAC Register

Power Supplies and Bypass Capacitors

The MAX9660 operates from a single 8V to 20V analog supply (AVDD) and a 2.5V to 3.6V digital supply (DVDD). Bypass AVDD to GND with 0.1µF and 10µF capacitors in parallel. Use an extensive ground plane to ensure optimum performance. Bypass DVDD to GND with a 0.1µF capacitor. The 0.1µF bypass capacitors should be placed as close as possible to their respective pins.

Refer to the MAX9660 evaluation kit for a proven PCB layout.

Layout and Grounding

Exposed Pad

The exposed pad on the TDFN package is electrically connected to GND. Solder the exposed pad to a ground plane to provide a low thermal resistance to ground for heat dissipation. Do not route traces under these packages. The layout of the exposed pad should have multiple small through-holes over a single large through-hole as shown as Figure 8. Thermal resistance between top and ground layer can be reduced. In addition, the vias should be flooded with solder for best thermal performance.

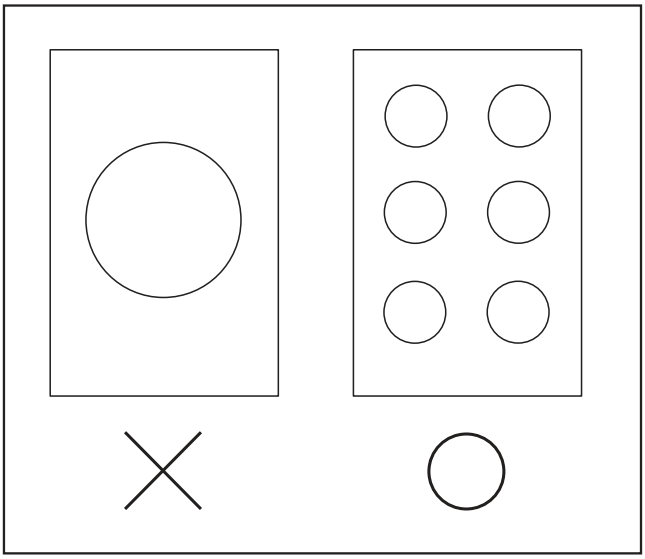
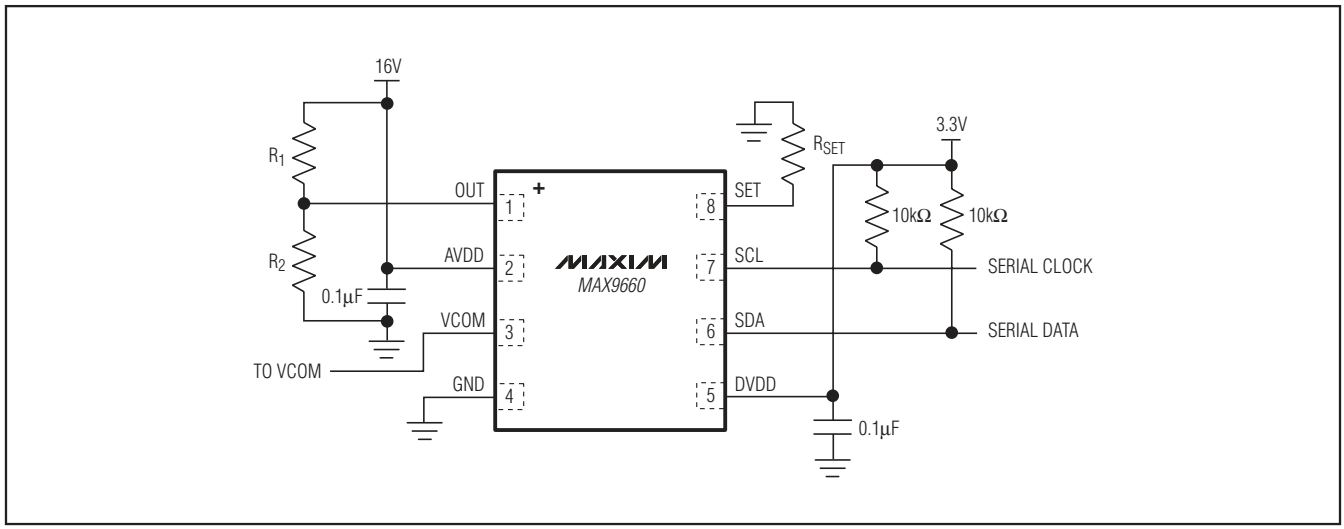


Figure 8. Multiple small through-holes are recommended over a single large through-hole in PCB layout.

7-Bit, Programmable VCOM Reference with 30x MOTP Memory

Typical Application Circuit



Chip Information

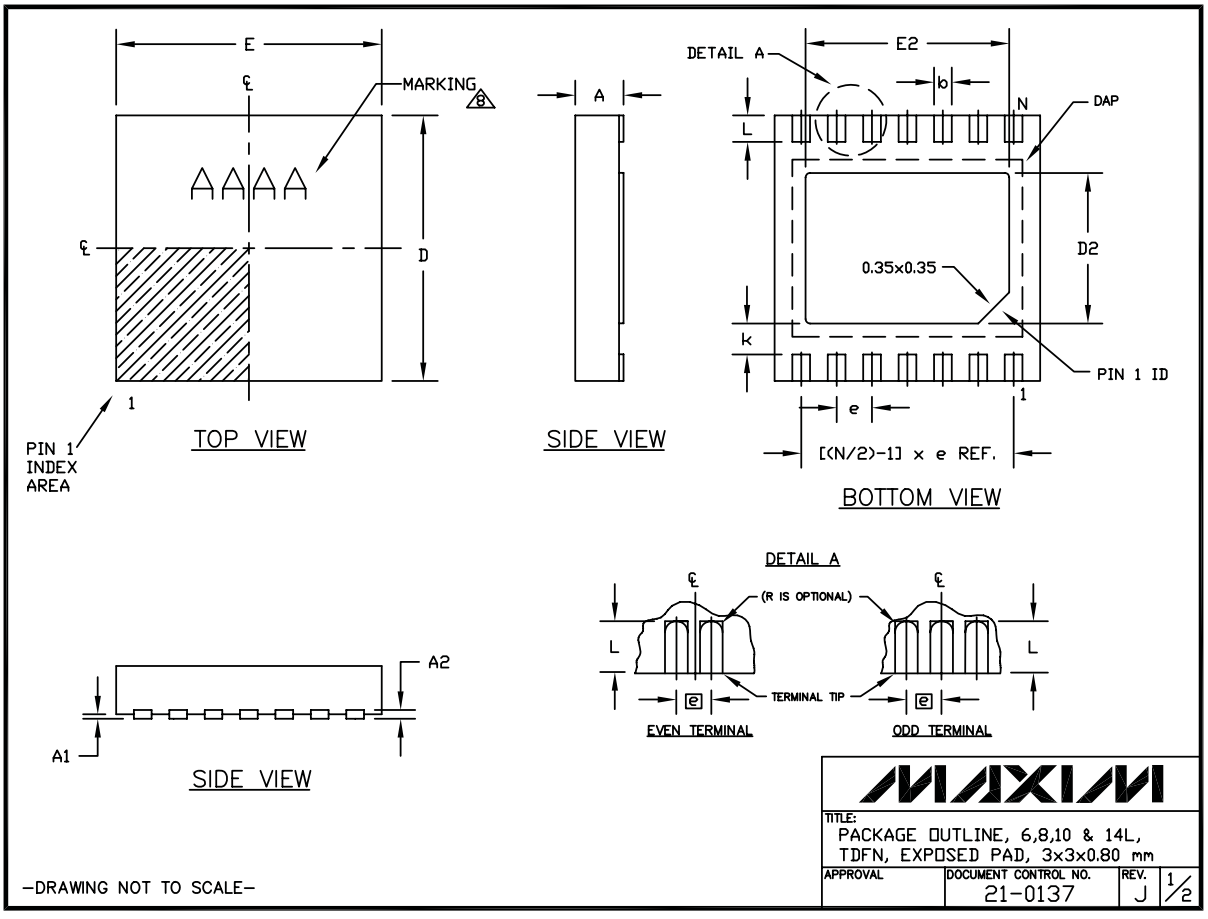
PROCESS: BiCMOS

7-Bit, Programmable VCOM Reference with 30x MOTP Memory

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 TDFN-EP	T833+2	21-0137



Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	J	2/2